

Quad 2-input NAND gate

BU4011B / BU4011BF / BU4011BFV

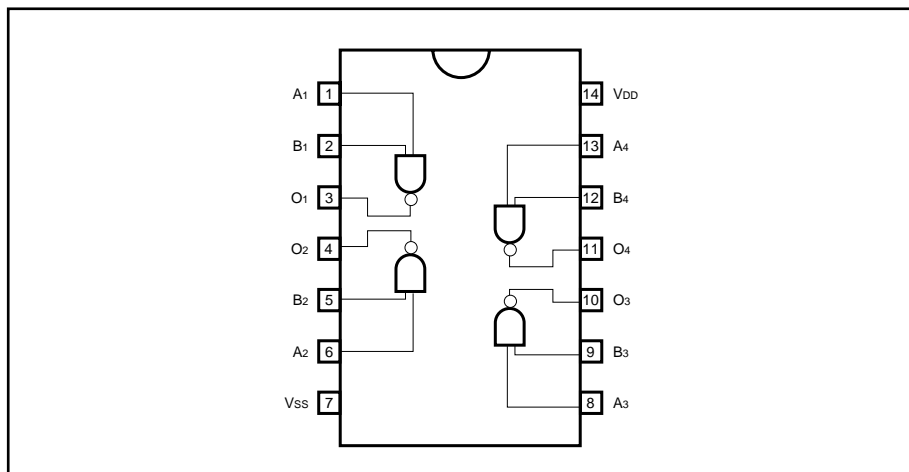
The BU4011B, BU4011BF, and BU4011BFV are dual-input positive logic NAND gates.

Four circuits are contained on a single chip. An inverter-based buffer has been added to the gate output, enabling improved input / output propagation characteristics, and an increased load capacitance minimizes fluctuation in propagation time.

●Features

- 1) Low power dissipation.
- 2) Wide range of operating power supply voltage.
- 3) High input impedance.
- 4) High fan-out.
- 5) Direct drive of 2 L-TTL inputs and 1 LS-TTL input.

●Block diagram



●Absolute maximum ratings ($V_{SS} = 0V$, $T_a = 25^\circ C$)

| Parameter | Symbol | Limits | Unit |
|-----------------------|-----------|---|------------|
| Power supply voltage | V_{DD} | - 0.3 ~ + 18 | V |
| Power dissipation | P_d | 1000 (DIP), 450 (SOP) 350 (SSOP-B14) | mW |
| Operating temperature | T_{opr} | - 40 ~ + 85 | $^\circ C$ |
| Storage temperature | T_{stg} | - 55 ~ + 150 | $^\circ C$ |
| Input voltage | V_{IN} | - 0.3 ~ $V_{DD} + 0.3$ | V |

●Electrical characteristics

DC characteristics (unless otherwise noted, $V_{SS} = 0V$, $T_a = 25^\circ C$)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | V _{DD} (V) | Conditions | Measurement circuit |
|----------------------------|-----------------|-------|------|------|------|---------------------|---|---------------------|
| | | | | | | | | |
| Input high-level voltage | V _{IH} | 3.5 | — | — | V | 5 | — | Fig. 1 |
| | | 7.0 | — | — | | 10 | | |
| | | 11.0 | — | — | | 15 | | |
| Input low-level voltage | V _{IL} | — | — | 1.5 | V | 5 | — | Fig. 1 |
| | | — | — | 3.0 | | 10 | | |
| | | — | — | 4.0 | | 15 | | |
| Input high-level current | I _{IH} | — | — | 0.3 | μA | 15 | V _{IH} = 15V | Fig. 1 |
| Input low-level current | I _{IL} | — | — | -0.3 | μA | 15 | V _{IL} = 0V | Fig. 1 |
| Output high-level voltage | V _{OH} | 4.95 | — | — | V | 5 | I _o = 0mA | Fig. 1 |
| | | 9.95 | — | — | | 10 | | |
| | | 14.95 | — | — | | 15 | | |
| Output low-level voltage | V _{OL} | — | — | 0.05 | V | 5 | I _o = 0mA | Fig. 1 |
| | | — | — | 0.05 | | 10 | | |
| | | — | — | 0.05 | | 15 | | |
| Output high-level current | I _{OH} | -0.16 | — | — | mA | 5 | V _{OH} = 4.6V | Fig. 1 |
| | | -0.4 | — | — | | 10 | V _{OH} = 9.5V | |
| | | -1.2 | — | — | | 15 | V _{OH} = 13.5V | |
| Output low-level current | I _{OL} | 0.44 | — | — | mA | 5 | V _{OL} = 0.4V | Fig. 1 |
| | | 1.1 | — | — | | 10 | V _{OL} = 0.5V | |
| | | 3.0 | — | — | | 15 | V _{OL} = 1.5V | |
| Static current dissipation | I _{DD} | — | — | 1 | μA | 5 | V _I = V _{DD} or GND | — |
| | | — | — | 2 | | 10 | | |
| | | — | — | 4 | | 15 | | |

Switching characteristics (unless otherwise noted, Ta = 25°C, Vss = 0V, CL = 50pF)

| Parameter | Symbol | Min. | Typ. | Max. | Unit. | VDD (V) | Conditions | Measurement circuit |
|-----------------------------------|------------------|------|------|------|-------|---------|------------|---------------------|
| | | | | | | 5 | | |
| Output rise time | t _{TLH} | — | 180 | 360 | ns | 5 | — | Fig. 2 |
| | | — | 90 | 180 | | 10 | | |
| | | — | 65 | 130 | | 15 | | |
| Output fall time | t _{THL} | — | 100 | 200 | ns | 5 | — | Fig. 2 |
| | | — | 50 | 100 | | 10 | | |
| | | — | 40 | 80 | | 15 | | |
| “L” to “H” Propagation delay time | t _{PLH} | — | 90 | 180 | ns | 5 | — | Fig. 2 |
| | | — | 50 | 100 | | 10 | | |
| | | — | 40 | 80 | | 15 | | |
| “H” to “L” Propagation delay time | t _{PHL} | — | 90 | 180 | ns | 5 | — | Fig. 2 |
| | | — | 50 | 100 | | 10 | | |
| | | — | 40 | 80 | | 15 | | |
| Input capacitance | C _{IN} | — | 5 | — | pF | — | — | — |

● Measurement circuits

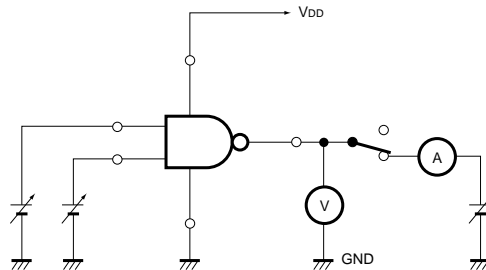


Fig. 1 DC characteristics

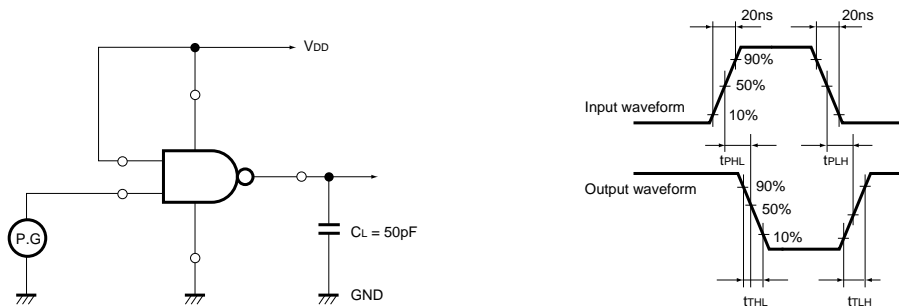


Fig. 2 Switching characteristics

●Electrical characteristic curve

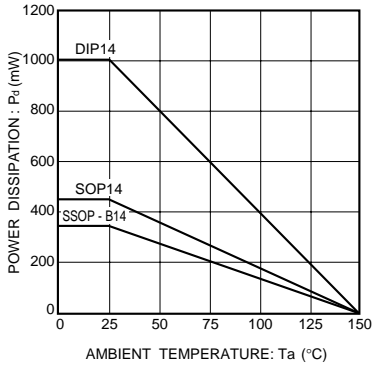
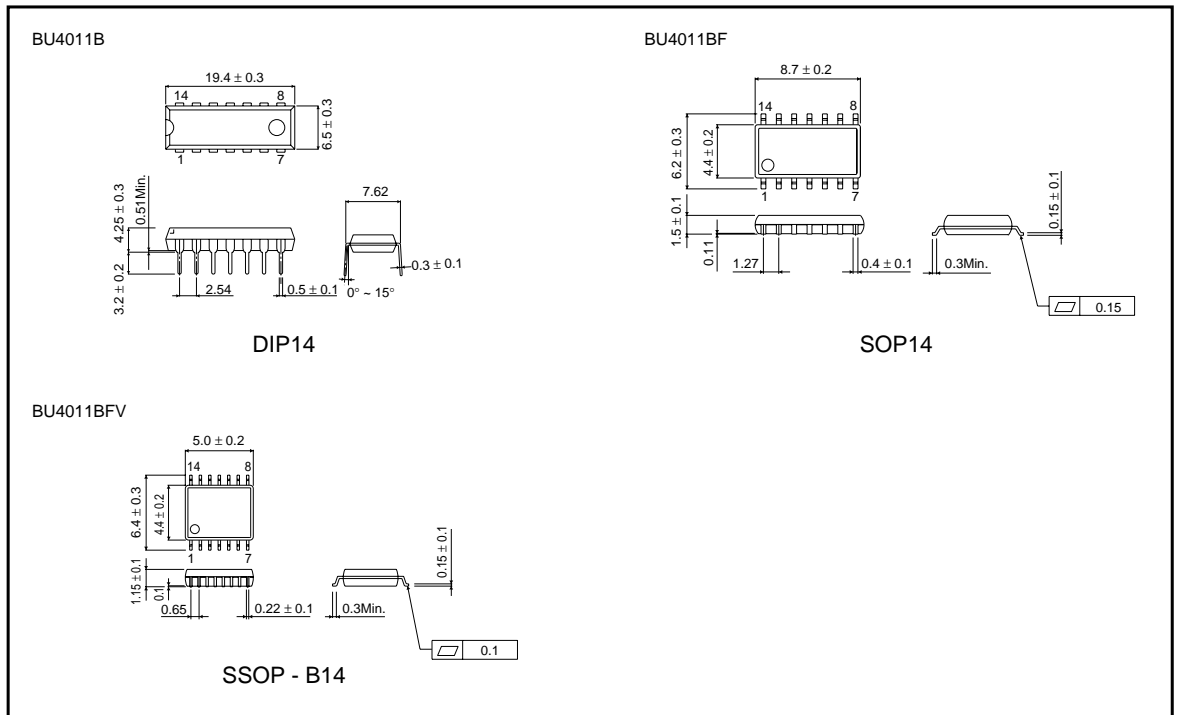


Fig. 3 Power dissipation vs. Ta

●External dimensions (Units: mm)



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