



SINGLE-INDUCTOR QUADRUPLE-OUTPUT TFT LCD POWER SUPPLY

FEATURES

- **Main Output, V_{MAIN}**
 - Adjustable Voltage, 3.0 V to 5.6 V/25 mA
 - Post-Regulated for Low Ripple (5mV_{PP})
 - ±0.8% Typical Accuracy
 - Efficiency up to 83%
- **Positive Output, V_{GH}**
 - Adjustable Voltage up to 20 V/2 mA
 - ±3% Typical Accuracy
- **Negative Output, V_{GL}**
 - Adjustable Voltage down to -18 V/2 mA
 - ±3% Typical Accuracy
- **Auxiliary 1.8 V/3.3 V Linear Regulator**

- **Automatic or Programmable Power Sequencing**
- **Complete 1 mm Component Profile Solution**
- **2.5 V to 5.5 V Input Voltage Range**
- **Output Short Circuit Protected**
- **16-Pin QFN Package (3 × 3 × 0,9 mm)**

APPLICATIONS

- **Small Form Factor a-Si and LTPS TFT LCD**
- **Cell Phones, Smart Phones**
- **PDAs, Pocket PCs**
- **Portable DVD**
- **Digital-Still Cameras, Camcorders**
- **Handheld Instruments**
- **Portable GPS**
- **Car Navigation Systems**

DESCRIPTION

The TPS6512x DC-DC converter supplies all three voltages required by amorphous-silicon (a-Si) and low-temperature poly-silicon (LTPS) TFT-LCD displays. The compact layout of the TPS6512x uses a single inductor to generate independently-regulated positive and negative outputs. A free-running variable peak current PWM control scheme time-multiplexes the inductor between outputs. This control architecture operates at a pseudo-fixed-frequency to provide fast response to line and load transients while maintaining a relatively constant switching frequency and high efficiency over a wide range of input and output voltages. Due to the high switching frequency capability of the device, inexpensive and ultra-thin 8.2 or 10 μ H inductors can be used.

The main output, V_{MAIN} , is post-regulated to provide a low-ripple source drive voltage for the LCD display. The auxiliary outputs generate a boosted output voltage, V_{GH} , up to 20 V, and a negative output voltage, V_{GL} , down to -18 V for the LCD gate drive. The device has internal current limiting for high reliability under fault conditions. Additionally, the device offers a fixed output linear regulator for the LCD logic circuitry.

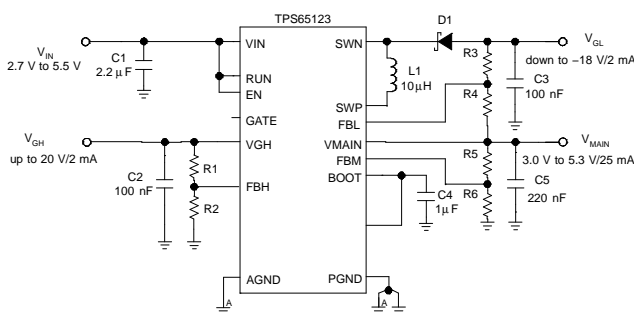


Figure 1. Typical Application

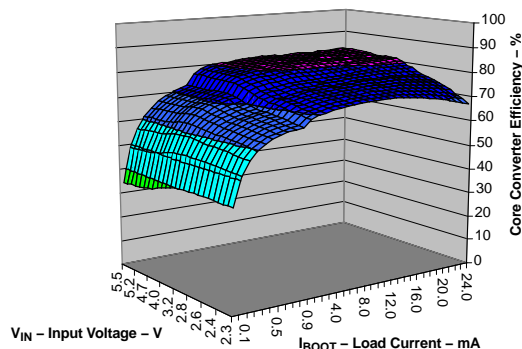


Figure 2. Core Converter Efficiency



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T _A	INTEGRATED LINEAR REGULATOR	POWER SEQUENCING	PACKAGE	PART NUMBER ⁽¹⁾	PACKAGE MARKING
-40 to 85°C	Fixed 3.3V output voltage	Automatic Power-Up/Down	3 × 3 QFN-16	TPS65120RGT	BKA
	Fixed 1.8V output voltage	Automatic Power-Up/Down	3 × 3 QFN-16	TPS65121RGT	BKB
	NO	Automatic Power-Up/Down	3 × 3 QFN-16	TPS65123RGT	BKC
	NO	Programmable Power-Up/Down	3 × 3 QFN-16	TPS65124RGT	BKD

(1) The xyz package is available in tape and reel. Add R suffix (xyzR) to order quantities of TBD parts. Add T suffix (xyzT) to order quantities of 250 parts.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		UNIT
Input voltage ⁽²⁾	V _{IN}	-0.3 V to +6 V
	SW _N	V _{IN} - 24 V to V _{IN} + 0.3 V
	SW _P	- 0.3 V to +23 V
Voltage ⁽²⁾	V _{GH}	- 0.3 V to +21 V
	V _{MAIN} , L _{DOIN} , L _{DOOUT} , EN _{VGL} , EN _{VGH}	- 0.3 V to +6 V
	BOOT	- 0.3 V to +6.2 V
Input voltage at GATE, EN, RUN ⁽²⁾		-0.3 V to V _{IN} + 0.3 V
Power dissipation		Internally limited
Operating temperature range		-40°C to 85°C
Maximum operating junction temperature, T _{J(max)}		135°C
Storage temperature range		65°C to 150°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.

DISSIPATION RATINGS⁽¹⁾

PACKAGE	R _{θJA}	DERATING FACTOR ABOVE T _A = 25°C
RGT	68°C/W	15mW/°C

(1) Maximum power dissipation is a function of T_{J(max)}, θ_{JA} and T_A. The maximum allowable power dissipation at any allowable ambient temperature is P_D = [T_{J(max)}-T_A]/ θ_{JA}.

ELECTRICAL CHARACTERISTICS
 $V_{IN} = 3.6\text{ V}$, $EN = RUN = V_{IN}$, $L = 10\ \mu\text{H}$, $T_A = -40^\circ\text{C}$ to 85°C , typical values are at $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CONVERTER STAGE						
V_{IN}	Input voltage for full load operation	$R_{L_MAIN} \geq 330\ \Omega$ at $V_{MAIN} = 5\text{ V}$, $R_{L_VGH} \geq 12\ \text{k}\Omega$ at $V_{GH} = 12\text{ V}$, $R_{L_VGL} \geq 12\ \text{k}\Omega$ at $V_{GL} = -12\text{ V}$, $V_{LDOIN} = \text{GND}$, $T_A = -40^\circ\text{C}$ to 85°C	2.7		5.5	V
	Minimum input voltage for start-up	$R_{L_MAIN} \geq 660\ \Omega$ at $V_{MAIN} = 5\text{ V}$, $R_{L_VGH} \geq 24\ \text{k}\Omega$ at $V_{GH} = 12\text{ V}$, $R_{L_VGL} \geq 24\ \text{k}\Omega$ at $V_{GL} = -12\text{ V}$, $V_{LDOIN} = \text{GND}$, $T_A = -20^\circ\text{C}$ to 85°C	2.5			V
f	Switching frequency	$R_{L_MAIN} = 250\ \Omega$ at $V_{MAIN} = 5\text{ V}$ $V_{LDOIN} = \text{ENVGH} = \text{ENVGL} = \text{GND}$		4.0		MHz
P_{GH}	Output power on V_{GH}	$V_{IN} \geq 2.7\text{ V}$		35		mW
		$V_{IN} \geq 2.5\text{ V}$		15		
P_{GL}	Output power on V_{GL}	$V_{IN} \geq 2.7\text{ V}$		35		mW
		$V_{IN} \geq 2.5\text{ V}$		15		
P_{TOT}	Total output power on $V_{BOOT} + V_{GH} + V_{GL}$	$V_{IN} \geq 2.5\text{ V}$		60		mW
		$V_{IN} \geq 2.7\text{ V}$		120		
		$V_{IN} \geq 3\text{ V}$		150		
		$V_{IN} \geq 4.5\text{ V}$		250		
η	Power efficiency	$V_{MAIN} = 5.0\text{ V}$, $I_{BOOT} = 20\text{ mA}$, $V_{GH} = 15\text{ V}$, $V_{GL} = -10\text{ V}$, $I_{GH} = I_{GL} = 100\ \mu\text{A}$, $V_{LDOIN} = \text{GND}$		83%		
I_{LIM}	P-MOS1 current limit	$2.7\text{ V} \leq V_{IN} \leq 5.5\text{ V}$		150	200	mA
$I_{START-UP}$	P-MOS1 start-up current limit	$2.7\text{ V} \leq V_{IN} \leq 5.5\text{ V}$		65		mA
$r_{DS(ON)}$	P-MOS1 switch on-resistance	$V_{IN} = V_{GS} = 3.6\text{ V}$		2.5	4.3	Ω
		$V_{IN} = V_{GS} = 2.5\text{ V}$		3.8	6.9	
	N-MOS1 switch on-resistance	$V_{BOOT} = V_{GS} = 3.7\text{ V}$		1.9	3.5	Ω
		$V_{BOOT} = V_{GS} = 5\text{ V}$		1.4	2.3	
	P-MOS1 leakage current	$V_{DS} = 6\text{ V}$, $T_A = 25^\circ\text{C}$		0.01		μA
	N-MOS1 leakage current			0.01		
	N-MOS2 + P-MOS2 forward voltage drop	$V_{GS} = V_{BOOT} = 5.5\text{ V}$, $V_{SWP} = 2\text{ V}$, $I_{BOOT} = I_D = 50\text{ mA}$		400	600	mV
	N-MOS3 + D1 forward voltage drop	$V_{GS} = V_{BOOT} = 5.5\text{ V}$, $V_{SWP} = 2\text{ V}$, $I_{GH} = I_D = 50\text{ mA}$		900	1100	mV
CONVERTER SUPPLY CURRENT						
I_Q	Quiescent current into V_{IN}	$I_{MAIN} = I_{GH} = I_{GL} = 0\text{ mA}$, $V_{GH} = +15\text{ V}$, $V_{GL} = -15\text{ V}$, $V_{MAIN} = 5\text{ V}$, $V_{FBH} = V_{FBM} = +1.5\text{ V}$, $V_{FBL} = -0.2\text{ V}$, $V_{BOOT} = 5.25\text{ V}$, $V_{LDOIN} = \text{GND}$, $EN = RUN = V_{IN}$, $T_A = 25^\circ\text{C}$		140	170	μA
	Quiescent current into V_{BOOT}			30	60	
	Quiescent current into V_{GH}			0.1	1	
I_{SD}	Shutdown current	$T_A = 25^\circ\text{C}$		0.1	1	μA

ELECTRICAL CHARACTERISTICS (continued)

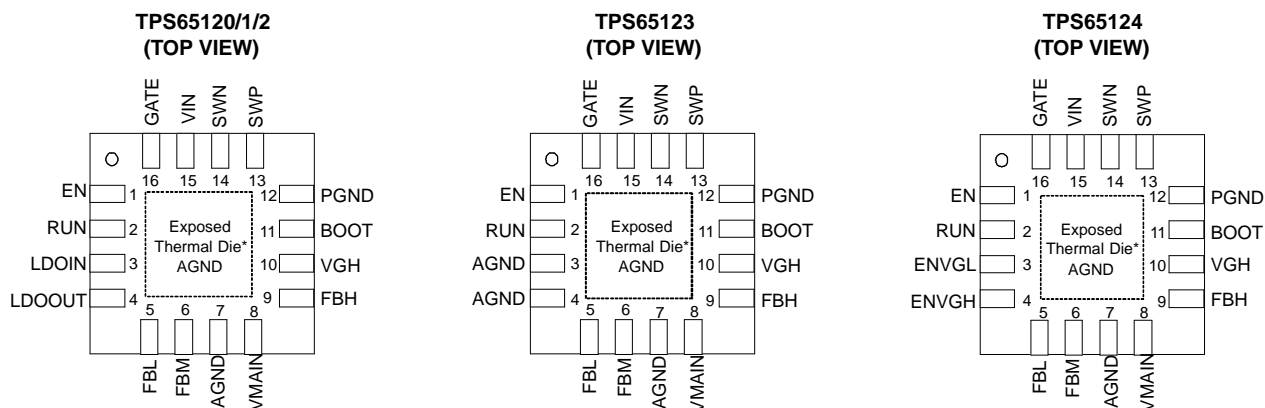
$V_{IN} = 3.6\text{ V}$, $EN = RUN = V_{IN}$, $L = 10\ \mu\text{H}$, $T_A = -40^\circ\text{C}$ to 85°C , typical values are at $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MAIN OUTPUT						
V_{MAIN}	Main output voltage range		3.0		5.6	V
I_{MAIN}	Maximum main output current	$V_{MAIN} \leq 5.3\text{ V}$	25			mA
		$V_{MAIN} \geq 5.3\text{ V}$	7.5			
V_{FBM}	Feedback regulation voltage	$2.7\text{ V} \leq V_{IN} \leq 5.5\text{ V}$, $100\ \mu\text{A} \leq I_{MAIN} \leq 25\text{ mA}$, $T_A = -20^\circ\text{C}$ to 50°C	1.203	1.213	1.223	V
		$2.7\text{ V} \leq V_{IN} \leq 5.5\text{ V}$, $0\text{ mA} \leq I_{MAIN} \leq 25\text{ mA}$	1.195	1.213	1.231	V
I_{FBM}	Feedback input bias current	$V_{FBM} = V_{REF}$		0.01	0.1	μA
	Load regulation	$I_{MAIN} = 0$ to 25 mA , $V_{MAIN} = 5\text{ V}$		0.006		%/mA
	Minimum dropout voltage	$I_{MAIN} = 10\text{ mA}$		130		mV
	Main output voltage ripple	$I_{MAIN} = 10\text{ mA}$		5		mV _{P-P}
I_{SC_MAIN}	Short-circuit current limit	$V_{BOOT} = 5.5\text{ V}$			50	mA
R_{DIS_VMAIN}	Discharge resistor for power-down sequence			10		k Ω
VGH OUTPUT						
V_{GH}	V_{GH} output voltage range		$V_{IN} + 0.5$		20	V
I_{GH}	Maximum DC output current				6	mA
	V_{GH} precharge resistor			1		k Ω
V_{FBH}	Feedback regulation voltage	$2.7\text{ V} \leq V_{IN} \leq 5.5\text{ V}$, $0\text{ mA} \leq I_{GH} \leq 2\text{ mA}$	1.177	1.213	1.249	V
I_{FBH}	Feedback input bias current	$V_{FBH} = 0\text{ V}$		0.01	0.1	μA
	Load regulation	$I_{GH} = 0$ to 2 mA , $V_{GH} = 15\text{ V}$		-0.11		%/mA
	Line regulation	$V_{IN} = 2.7\text{ V}$ to 5.5 V , $I_{GH} = 100\ \mu\text{A}$		0.01		%/V
	V_{GH} output voltage ripple	200 μA load, $V_{GH} = 15\text{ V}$, $C_{OUT} = 220\text{ nF}$, $C_{FF} = 10\text{ pF}$		20		mV
R_{DIS_VGH}	Discharge resistor for power-down sequence			10		k Ω
VGL OUTPUT						
V_{GL}	V_{GL} Output voltage range		-18		-2.5	V
I_{GL}	Maximum DC output current				6	mA
V_{FBL}	Feedback regulation voltage	$2.7\text{ V} \leq V_{IN} \leq 5.5\text{ V}$, $0\text{ mA} \leq I_{GL} \leq 2\text{ mA}$	-0.036	0	0.036	V
I_{FBL}	Feedback input bias current	$V_{FBL} = 0\text{ V}$		0.01	0.1	μA
	Load regulation	$I_{GL} = 0$ to 2 mA , $V_{GL} = -15\text{ V}$		0.13		%/mA
	Line regulation	$V_{IN} = 2.7\text{ V}$ to 5.5 V , $I_{GL} = 100\ \mu\text{A}$		0.1		%/V
	V_{GL} output voltage ripple	200 μA load, $V_{GL} = -15\text{ V}$, $C_{OUT} = 220\text{ nF}$		20		mV

ELECTRICAL CHARACTERISTICS (continued)
 $V_{IN} = 3.6\text{ V}$, $EN = RUN = V_{IN}$, $L = 10\ \mu\text{H}$, $T_A = -40^\circ\text{C}$ to 85°C , typical values are at $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LINEAR REGULATOR STAGE - AUXILIARY OUTPUT						
V_{LDOIN}	Input voltage range		2.5		5.8	V
V_{LDOOUT}	Output voltage range		1.8	$V_{LDOIN} - 0.5$		V
I_{LDOOUT}	Maximum output current		20			mA
I_{SC_LDO}	Short-circuit current limit	$V_{LDOOUT} = 0\text{ V}$			50	mA
	Minimum dropout voltage	$I_{LDOOUT} = 10\text{ mA}$			400	mV
	Total accuracy	$2.5\text{ V} \leq V_{LDOIN} \leq 5.5\text{ V}$, $0\text{ mA} \leq I_{LDOOUT} \leq 20\text{ mA}$			$\pm 3\%$	
	Load regulation	$I_{LDOOUT} = 0$ to 20 mA		0.006		%/mA
	Line regulation	$V_{LDOIN} = V_{LDOOUT} + 0.5\text{ V}$ (min 2.5 V) to 5.5 V , $I_{LDOOUT} = 20\text{ mA}$		0.013		%/V
I_{Q_LDO}	Linear regulator quiescent current	$V_{LDOIN} = V_{LDOOUT} + 0.4\text{ V}$ (min 2.5 V), $T_A = 25^\circ\text{C}$		11	20	μA
I_{SD_LDO}	Linear regulator shutdown current	GATE = VIN		0.2	1	μA
GATE DRIVER						
	Gate output pull-down resistance	$V_{GATE} < 500\text{ mV}$		100		k Ω
	Gate output pull-up resistance			100		k Ω
V_{IH}	High level input voltage		1.4			V
V_{IL}	Low level input voltage				0.4	V
UNDERVOLTAGE LOCKOUT						
V_{UVLO}	Undervoltage lockout threshold	V_{IN} falling		2.15	2.3	V
LOGIC SIGNALS EN, RUN, ENVGL, ENVGH						
V_{IH}	High level input voltage		1.4			V
V_{IL}	Low level input voltage				0.4	V
I_{LKG}	Logic input leakage current	ENVGL, ENVGH = V_{IN} or GND (TPS65124) EN, RUN = V_{IN}		0.01	0.1	μA
	EN, RUN pin pull-down resistance	EN, RUN $\leq 0.4\text{ v}$		100		k Ω

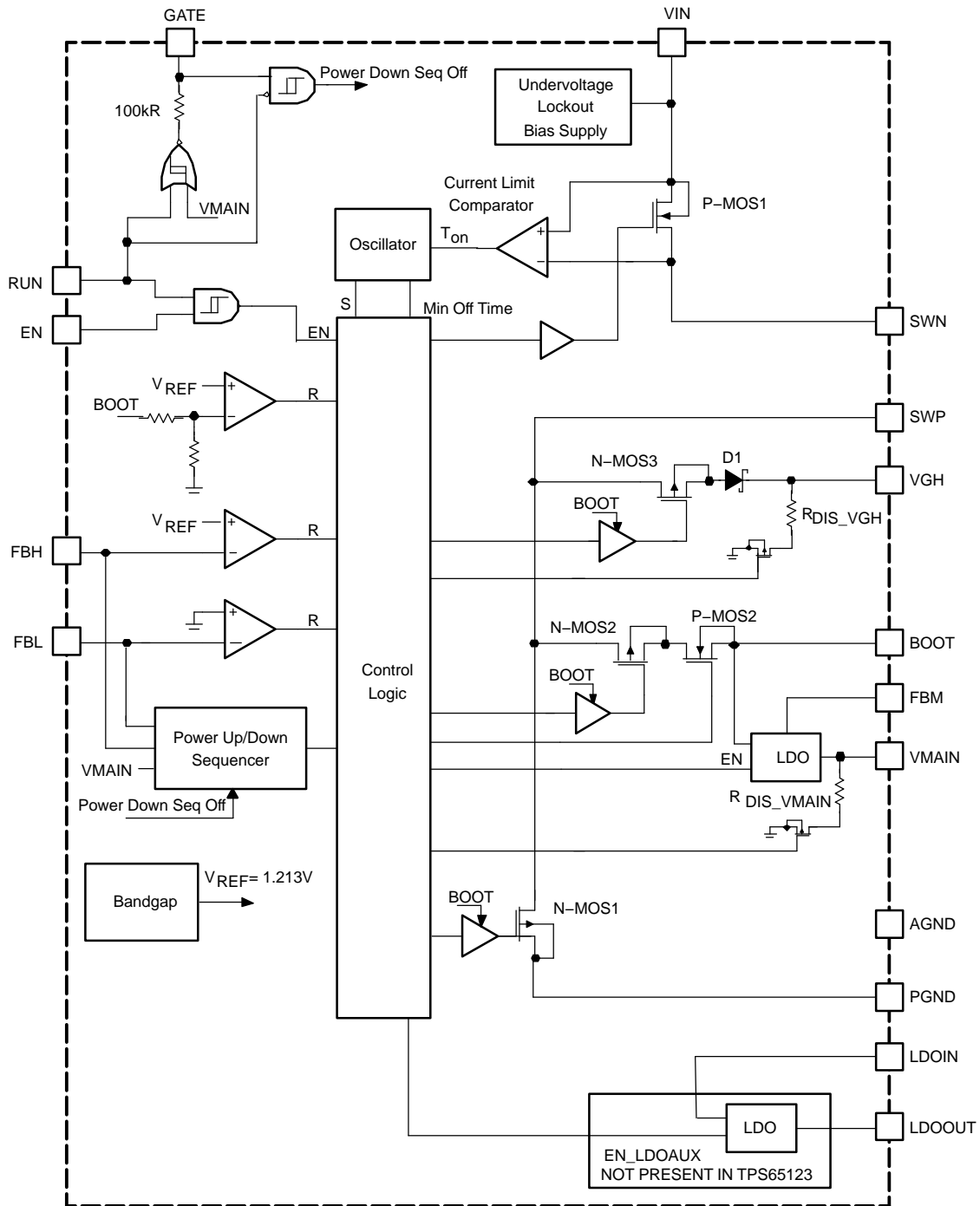
PIN ASSIGNMENTS



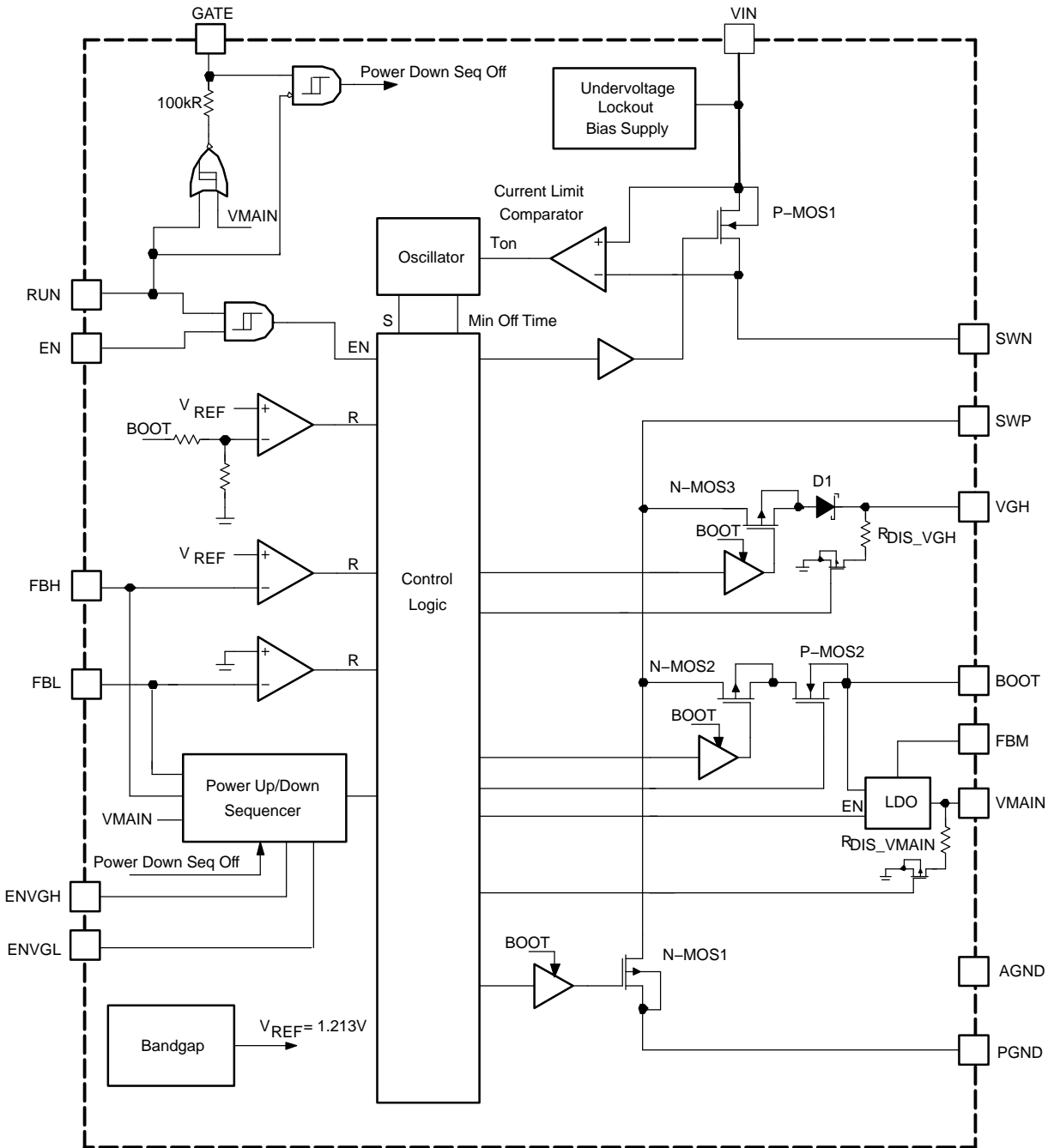
TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
VIN	15	I	This is the input voltage pin of the device.
GATE	16	I/O	This pin can either be the gate driver output to an external small P-Channel MOSFET (see application section), or an active high control input. Pulling GATE above the 1.4 V logic-high level and RUN to a logic-low level disables the integrated active power-down sequencing.
RUN	2	I	RUN controls the external P-Channel MOSFET. This pin must be terminated and not be left floating. Forcing this pin to a logic-high level turns on the external MOSFET switch.
EN	1	I	This is the enable pin of the multiple-output dc-to-dc converter. This pin must be terminated and not be left floating. A simultaneous logic-high level on EN and RUN enables the converter and a logic-low shuts down the device.
SWN	14	I/O	Connect the inductor to this pin. This pin is connected to the source of the high-side MOSFET switch.
SWP	13	I/O	Connect the inductor to this pin. This pin is connected to the drain of the low-side MOSFET switch.
PGND	12	O	Power ground. Connect to AGND underneath the IC.
VGH	10	O	Positive output
BOOT	11	O	Provides a bootstrapped supply for the rectifier MOSFET driver, enabling the gate of the MOSFET to be driven above the output voltage.
VMAIN	8	I	Main output
FBH	9	I	Feedback pin for the positive output voltage divider. Regulates to 1.213 V nominal.
FBL	5	I	Feedback pin for the negative output voltage divider. Regulates to 0 V nominal. Connect feedback resistor divider between VGL and main output.
FBM	6	I	Feedback pin for the main output voltage divider. Regulates to 1.213V nominal.
AGND	7, 3, 4		Analog ground. Connect to power ground (PGND) underneath IC. Pins 3 and 4 are only used for AGND in TPS65123.
LDOIN	3	I	Auxiliary linear regulator input. If this pin is connected to GND, the voltage regulator is disabled (TPS65120/1/2). The low-dropout series-pass regulator (LDO) is enabled according to the GATE signal timing.
LDOOUT	4	O	Auxiliary linear regulator output (TPS65120/1/2).
ENVGL	3	I	Enable pin for negative output (TPS65124). This pin should be terminated and not be left floating.
ENVGH	4	I	Enable pin for positive output (TPS65124). This pin should be terminated and not be left floating.

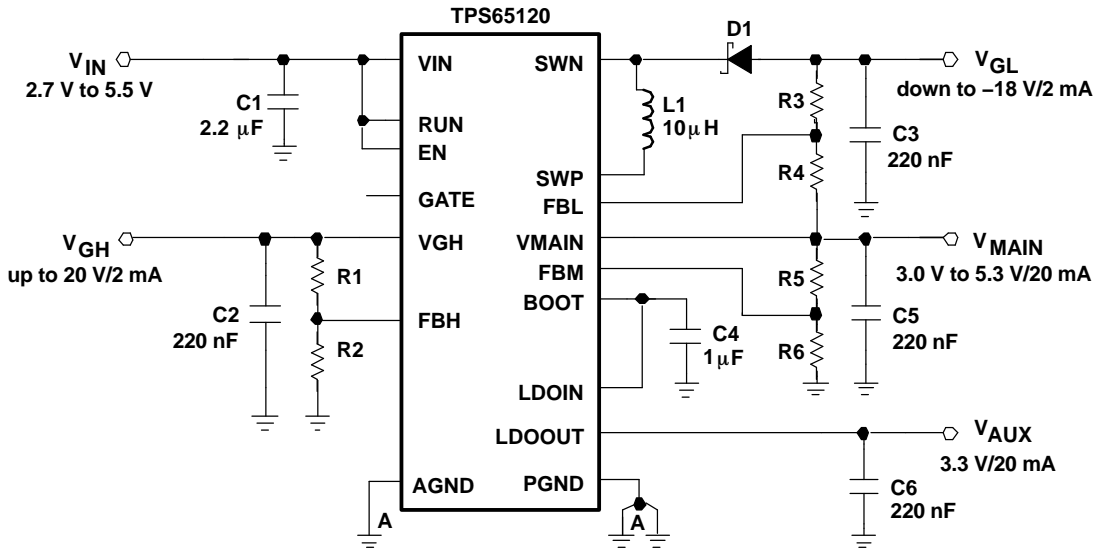
FUNCTIONAL BLOCK DIAGRAM - TPS65120/1/2/3



FUNCTIONAL BLOCK DIAGRAM - TPS65124



PARAMETER MEASUREMENT INFORMATION

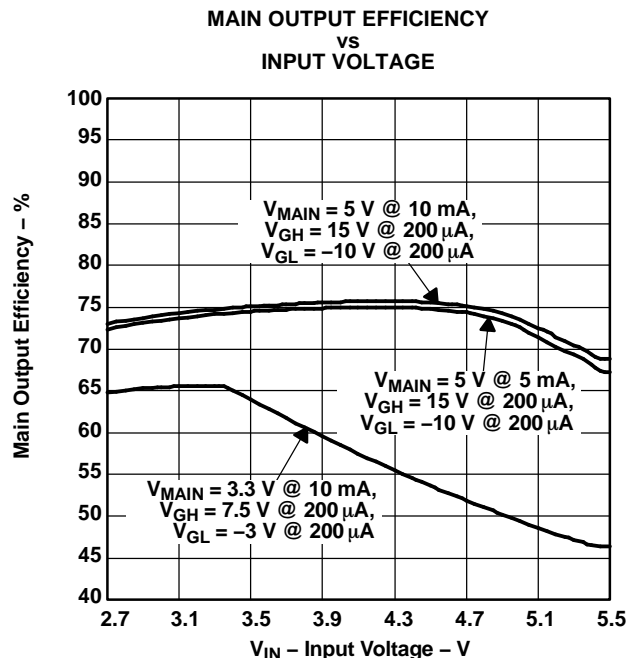
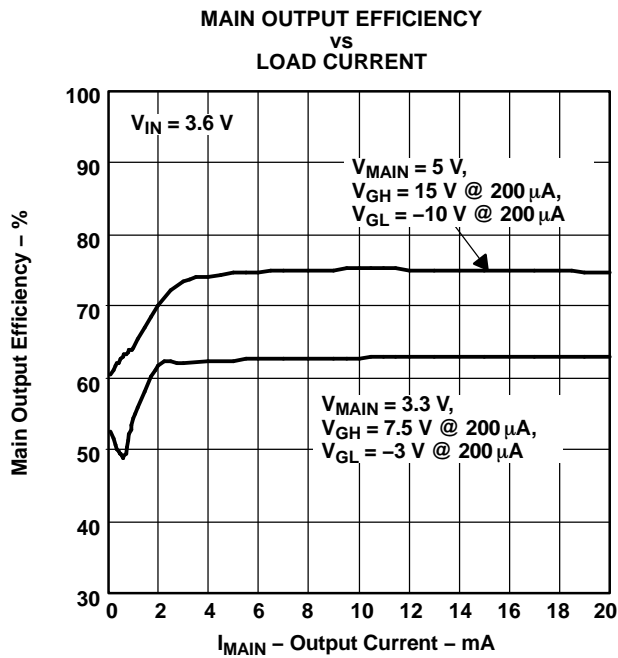
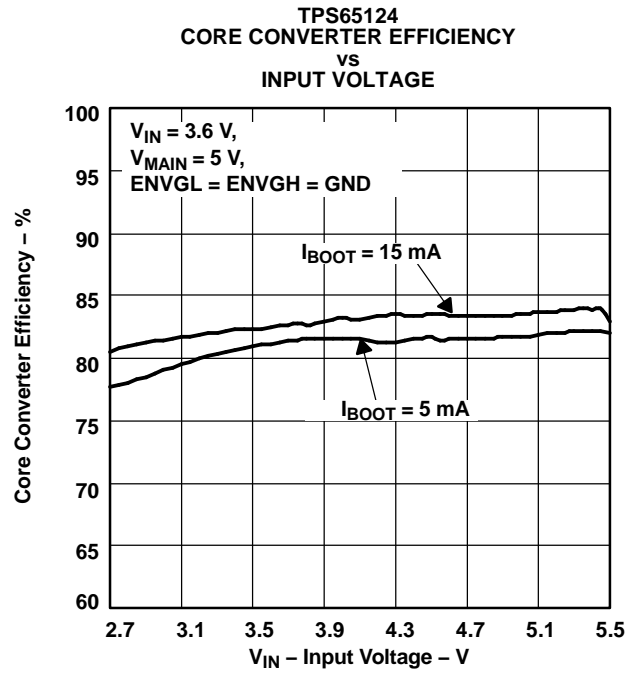
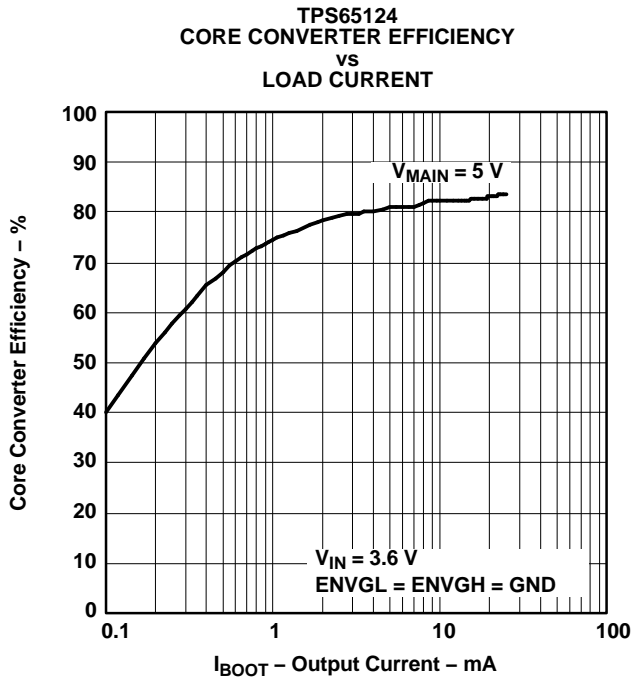


- List of Components:**
 U₁ = TPS6512x
 L₁ = EPCOS SIMID1812-C
 D₁ = ZETEX ZUMD54C
 C_x = X5R/X7R

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
η	Core converter efficiency	vs Load current	3
		vs Input voltage	4
	Main output efficiency	vs Load current	5
		vs Input voltage	6
V _{MAIN}	Output ripple voltage		7
	DC output voltage	vs Load current	8
	Load transient response		9
V _{GH} , V _{GL}	Positive, negative output ripple voltage		10, 11
V _{GH}	DC output voltage	vs Load current	12
V _{GL}	DC output voltage	vs Load current	13
f _s	Switching frequency	vs Load current	14
I _Q	No load quiescent current	vs Input voltage	15
	Power-Up Sequencing (TPS65120)		16
	Power-Down Sequencing (TPS65120)		17



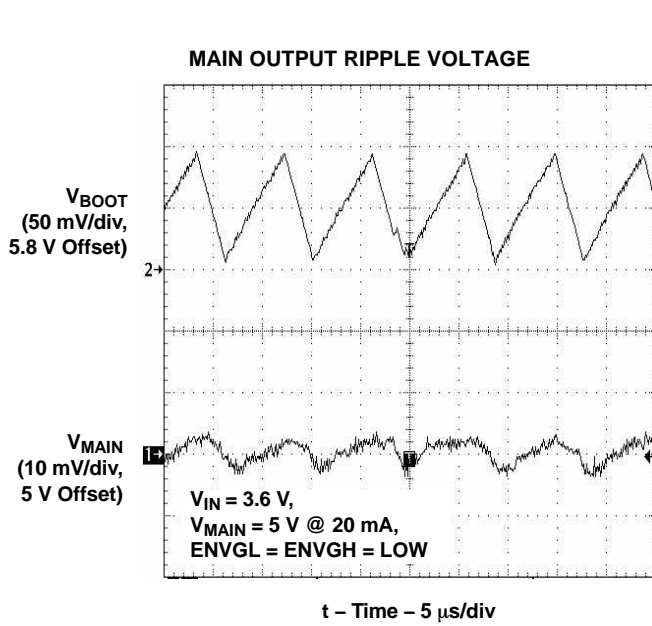


Figure 7.

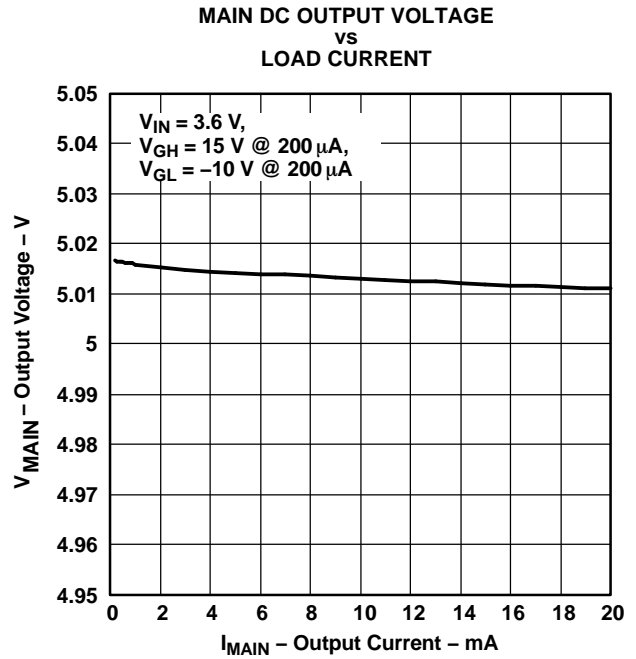


Figure 8.

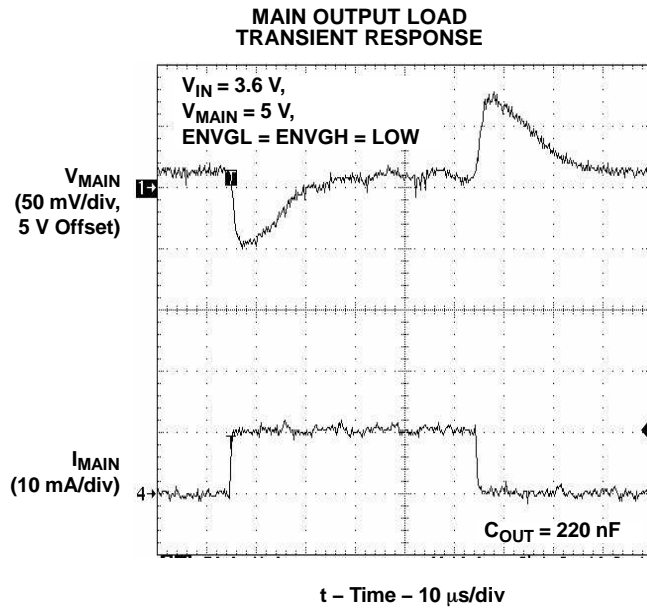


Figure 9.

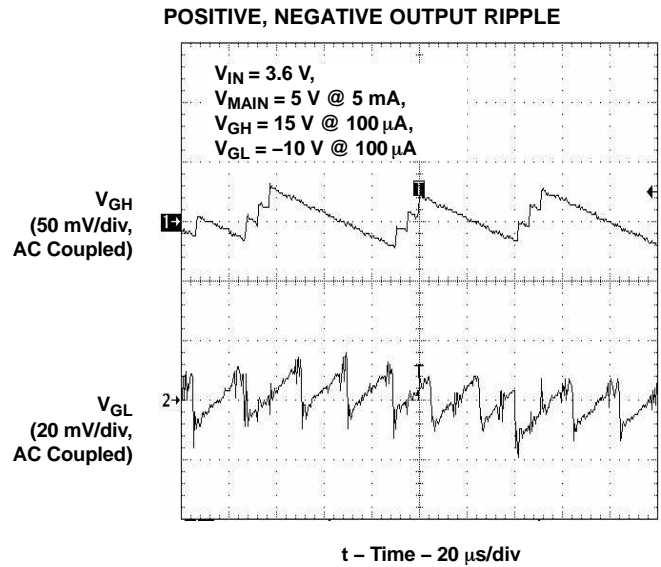


Figure 10.

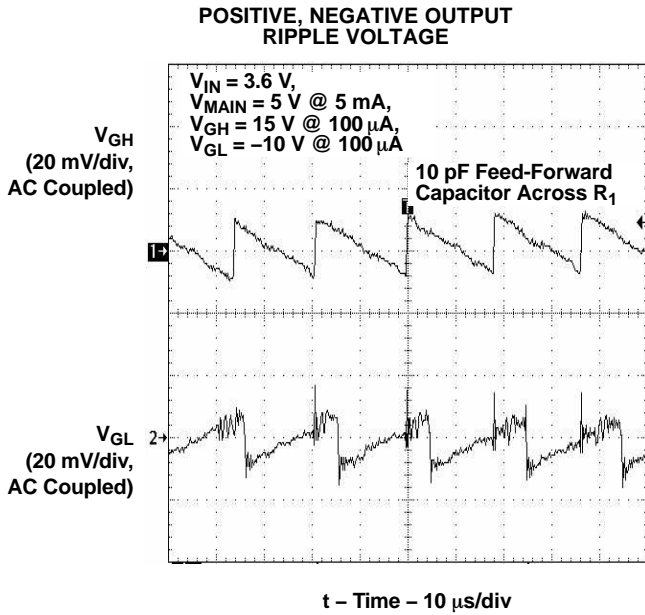


Figure 11.

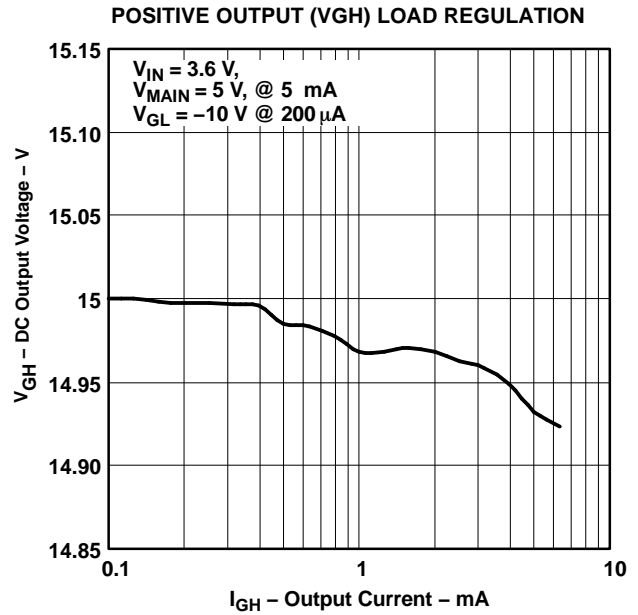


Figure 12.

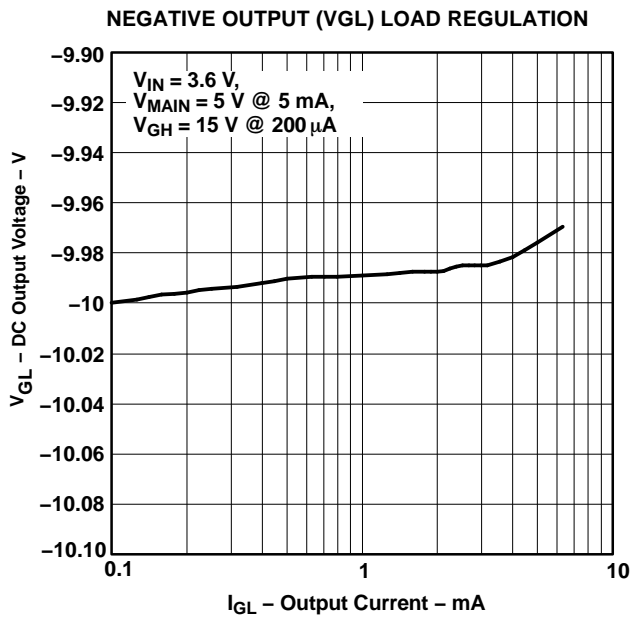


Figure 13.

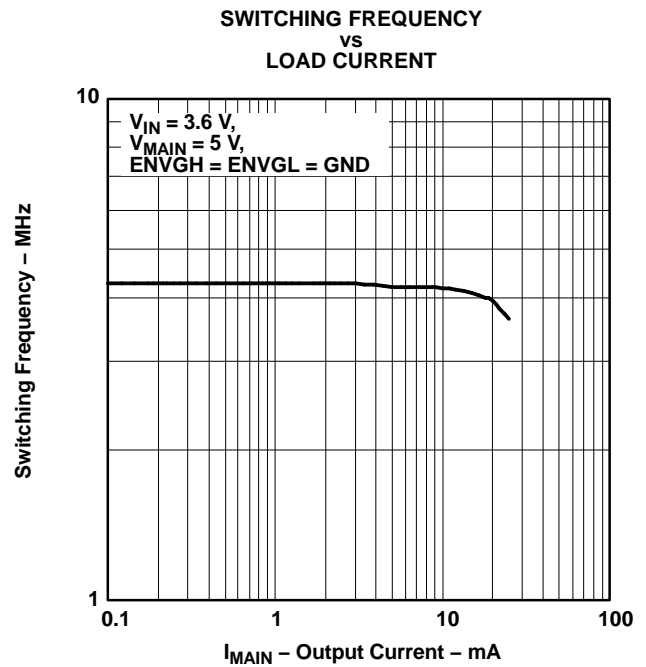


Figure 14.

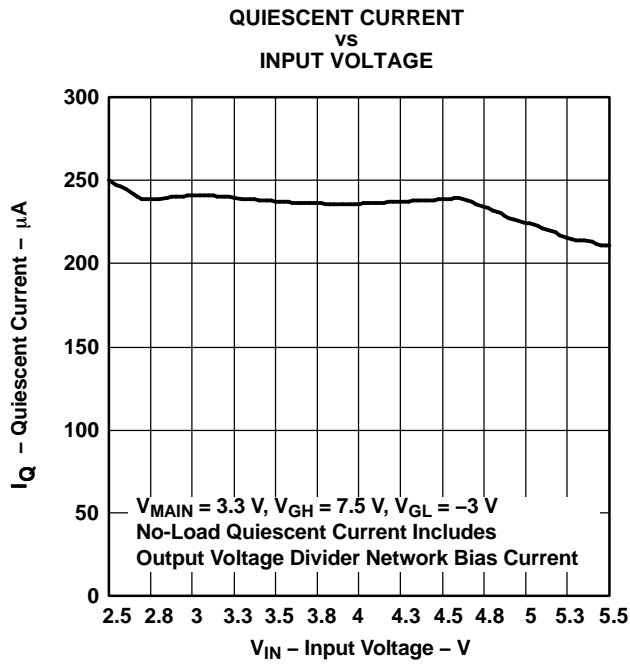


Figure 15.

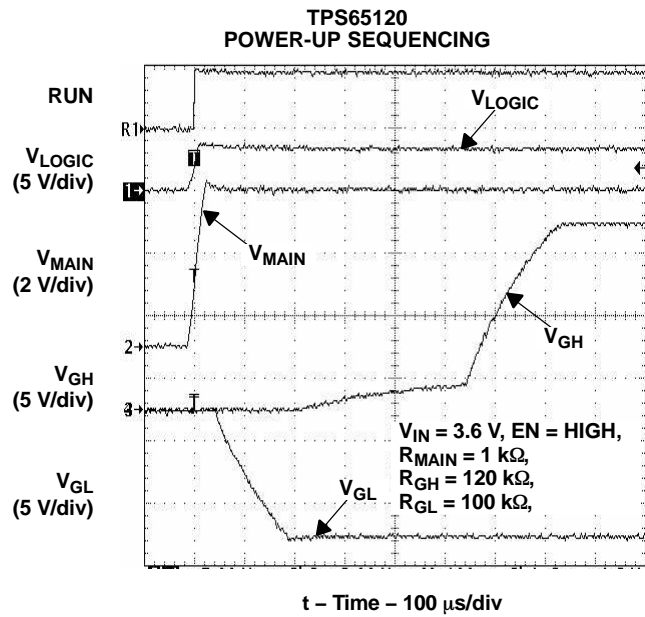


Figure 16.

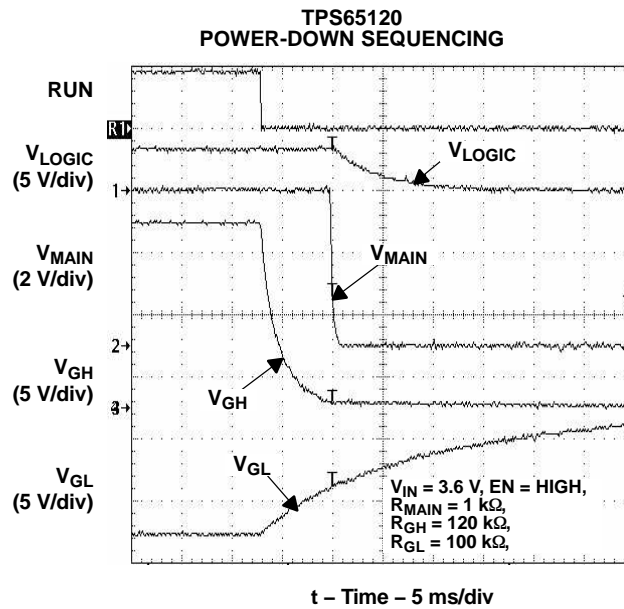


Figure 17.

DETAILED DESCRIPTION

The standard application circuit (Figure 1) of the TPS65120 is a complete power supply for TFT LCD displays. The circuit generates four independent supplies for the source driver (V_{MAIN}), the gate drivers (V_{GH} , V_{GL}) and a logic supply for the timing controller. The input voltage range is from 2.5 V to 5.5 V.

The TPS65120/1/2 contains a high-performance switching regulator and two low-dropout linear regulators (LDOs). One of the LDOs generates V_{MAIN} and the other powers the logic inside the panel. The TPS65123 includes only one linear regulator to provide the main output with low ripple voltage and can be set from 3.0 V to 5.3 V with an external resistor voltage divider. The TPS65124 integrates programmable power sequencing for highest flexibility.

OPERATION

The TPS6512x generates both positive and negative supply voltages using a single inductor. It alternates between acting as a step-up converter and an inverting converter on a cycle-by-cycle basis. All output voltages are independently regulated.

A free-running, variable-peak-current PWM control scheme is used to time-multiplex the inductor between BOOT, V_{GH} , and V_{GL} outputs. This inherently-stable control architecture operates at a pseudo fixed frequency, providing fast response to line and load transients while maintaining a relatively constant switching frequency and high efficiency over a wide range of input and output voltages.

During the first cycle of operation, internal switches N-MOS1 and P-MOS1 are turned on. SWN connects to VIN, SWP pulls to ground and the inductor current rises. Once the inductor current reaches the DC current limit (I_{LIM}) of 150 mA (typ) the internal control logic can either turn off N-MOS1 or P-MOS1 to service the requesting output. Depending on the required output power, the converter starts another cycle or enters a pulse-skipping modulation scheme to increase efficiency under light loads. The current into the SWN pin measures the inductor current. The TPS6512x controls the inductor current to regulate BOOT, V_{GH} , and V_{GL} output voltages.

To achieve low ripple voltage and high accuracy, the main output (V_{MAIN}) is post-regulated by an integrated LDO. This LDO regulator regulates energy from the BOOT output down to 5.3 V (max). To achieve the highest efficiency, the BOOT voltage is regulated to minimize the dropout voltage across the LDO to approximately $V_{MAIN} + 0.5$ V.

In addition, the VMAIN, VGH, VGL outputs are monitored for fault conditions that last longer than the fault-timer period of 100 μ s (typ). The device goes into a latched shutdown state in case of a fault condition.

Soft Start

The TPS6512x has an internal soft-start circuit that limits the inrush current during startup. This prevents possible voltage drops of the input voltage in case the battery or a high impedance power source is connected to the input of the device.

The device powers up by precharging the BOOT output capacitor to VIN. During the precharge phase, the current through the rectifying switch N-MOS2 is limited. This also limits the output current under short-circuit conditions on the BOOT output. To ensure proper startup of the device, the BOOT output must be left unloaded during the precharge phase.

After the precharge phase, the converter operates with an $I_{START-UP}$ current limit of 65 mA (typ), then increases gradually to the full current limit of 150 mA (typ).

Undervoltage Lockout

To ensure that the input voltage is high enough for reliable operation, the TPS6512x includes an under-voltage lockout (UVLO) circuit. The UVLO threshold at the VIN pin is 2.15 V (typ) falling and 2.25 V (typ) rising. The 100 mV (typ) hysteresis prevents supply transients from causing restarts.

Once the input voltage exceeds the UVLO rising threshold, the controller can enable the reference voltage and precharges BOOT. When the input voltage falls below the UVLO falling threshold, the controller turns off the reference and all the regulator outputs, and pulls GATE high with an internal 100 k Ω resistor to turn off P1 (Figure 18).

DETAILED DESCRIPTION (continued)

Enable and Power Sequencing (TPS65120/1/2/3)

To correctly power up most TFT panels, the gate-drive supplies must be sequenced such that the negative supply (V_{GL}) powers up before the positive supply (V_{GH}). The TPS65120/1/2/3 controls this sequence through an enable pin.

Once RUN is high, the TPS65120/1/2/3 turns on the external P-channel MOSFET P1 (see Figure 18) by pulling GATE low. GATE is pulled down with a 100 k Ω resistor. The DC/DC converter then starts, enabling the BOOT output.

Pulling the enable pin (EN) high enables the MAIN output. When the output voltage V_{MAIN} has reached 90% of its nominal value, the negative output enables. V_{GH} is delayed until the negative voltage has reached 90% of its nominal value.

Pulling the RUN pin low shuts down the device. Power-down sequencing starts by switching off V_{GH} and V_{GL} .

The V_{GH} output capacitor is actively discharged by an internal resistor while V_{GL} is only discharged by its feedback voltage divider. The required time to discharge the output capacitor at V_{GL} output depends on the load current. Once V_{FBL} has reached 1.2 V (typ) the main output is turned off followed by the output voltage V_{LOGIC} . This sequence is shown in Figure 19.

When no power sequencing is required on the digital supply voltage (V_{LOGIC}), tie EN and RUN signals together and GATE can be connected to a logic-high level to disable the power-down sequencer. Each output turns off depending upon load current and output capacitance.

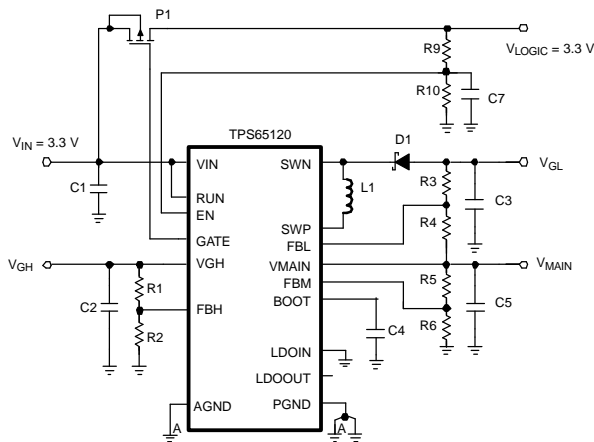


Figure 18. Power Sequencing on Digital Supply Voltage, V_{LOGIC}

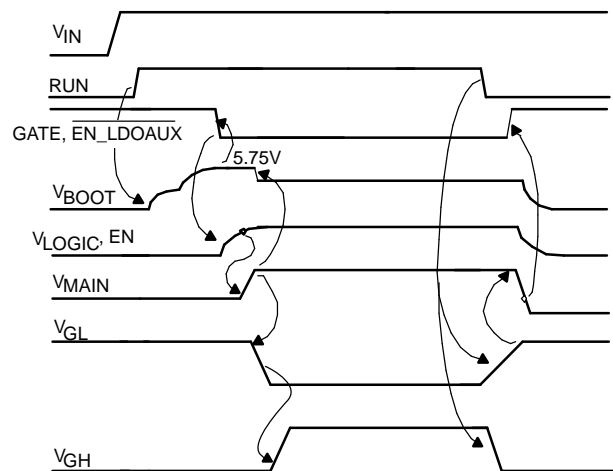


Figure 19. TPS65120/1/2/3 Power Sequence

DETAILED DESCRIPTION (continued)

Enable and Power Sequencing (TPS65124)

The TPS65124 controls the power sequencing of V_{LOGIC} , V_{MAIN} , V_{GH} and V_{GL} with four separate enable pins. These pins must be terminated and not be left floating to prevent instability.

Once RUN is pulled high and the input voltage on VIN exceeds the rising input UVLO threshold, the reference is turned on and the external P-channel MOSFET P1 (see Figure 20) is switched on by pulling GATE low. The GATE is pulled down with a 100 kΩ resistor. The DC/DC converter then starts up, enabling the BOOT output.

Pulling enable pin high (EN) powers on the MAIN output. This power sequencing must occur before the gate voltages are enabled. Conversely V_{GL} and V_{GH} output voltages must be turned off by pulling ENVGL and ENVGH inputs to ground before the MAIN output is switch off.

To clamp the V_{GL} output near zero when the MAIN output is still on, an external diode (D2) can be used. In some applications this diode may already be implemented in the display.

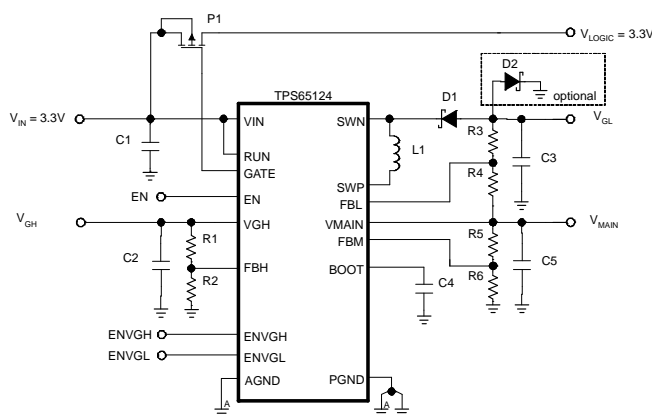


Figure 20. Power Sequencing on Digital Supply Voltage, V_{LOGIC}

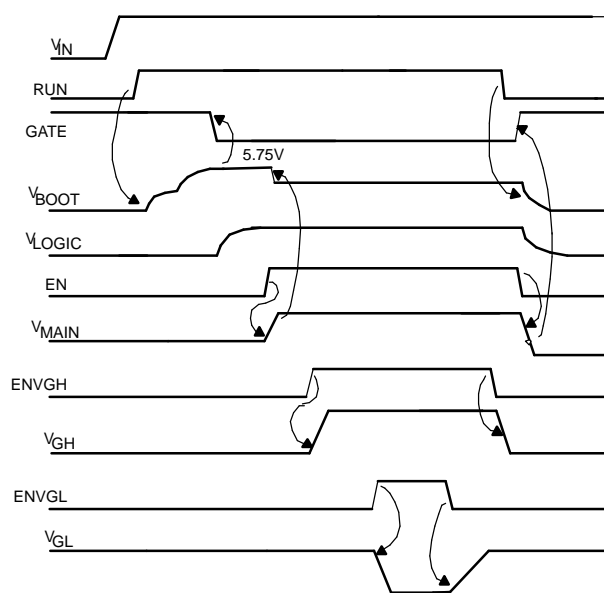


Figure 21. TPS65124 Programmable Power Sequence

Fault Protection

All TPS6512x outputs are protected against a short circuit to ground. During steady-state operation, if the output V_{MAIN} , V_{GH} or V_{GL} falls below its fault detection threshold the device simultaneously turns off all three outputs. Once V_{MAIN} comes down to 700 mV typ, the GATE output is pulled to V_{IN} , the auxiliary LDO (TPS65120/1/2) is disabled and the device enters a shutdown state.

The auxiliary LDO present in TPS65120/1/2 has an integrated current foldback circuit for reliable short-circuit protection.

The device can be enabled again by toggling the enable pins (RUN, EN) below 0.4 V or by cycling the input voltage below the UVLO falling threshold (2.15 V typ).

APPLICATION INFORMATION

OUTPUT POWER CAPABILITY

The first step in the design procedure is to calculate the maximum output current for each output under certain input and output voltage conditions. The TPS6512x uses time-multiplex operation to share the inductive storage element between BOOT, VGH and VGL outputs. To avoid complex calculations it is recommended to use the specified output-power data from the electrical characteristics table to determine the maximum output-power capability.

The following example shows how to proceed for given requirements:

- Input Voltage = 3.0 V
- MAIN Output = 5.0 V @ 10 mA
- VGH output = 12 V @ 500 μ A
- VGL output = -12 V @ 300 μ A

1. Calculate Maximum Output Power on VGH Output

$$P_{GH} = V_{GH} \times I_{GH}$$

2. Calculate Maximum Output Power on VGL Output

$$P_{GL} = |V_{GL}| \times I_{GL}$$

3. Calculate Maximum Output Power on BOOT Output

$$P_{BOOT} = P_{MAIN} \times \eta_{LDO_MAIN} \approx \frac{V_{MAIN}^2}{V_{MAIN} + 0.5} \times I_{MAIN} \quad \text{for } V_{IN} < V_{MAIN} + 0.5$$

$$P_{BOOT} = P_{MAIN} \times \eta_{LDO_MAIN} \approx \frac{V_{MAIN}^2}{V_{IN}} \times I_{MAIN} \quad \text{for } V_{IN} > V_{MAIN}$$

4. Maximum Output Power Verification

The electrical characteristics table states that for $V_{IN} > 3.0$ V, the maximum power on VGH and VGL outputs must be lower than 35 mW each. Furthermore, the total output power ($P_{BOOT} + P_{GH} + P_{GL}$) must be lower than 150 mW.

In our design example, $P_{GH} = 6$ mW, $P_{GL} = 3.6$ mW, and $P_{BOOT} = 55$ mW. Since these numbers are well below the specified values, we can conclude that TPS6512x can reasonably power such a display.

SETTING THE OUTPUT VOLTAGE

The output voltages are defined as shown in Figure 22.

$$V_{MAIN} = V_{FBM} \times \frac{R5 + R6}{R6}$$

with an internal reference voltage V_{FBM} typical = 1.213V.

$$V_{GH} = V_{FBH} \times \frac{R1 + R2}{R2}$$

with an internal reference voltage V_{FBH} typical = 1.213V.

$$|V_{GL}| = V_{MAIN} \times \frac{R3}{R4}$$

To minimize the operating quiescent current, set R2, R4 and R6 in the range 100 k Ω to 300 k Ω . Great care should be taken to route the FBx lines away from noise sources such as the inductor or the SWN and SWP lines.

A feed-forward capacitor across the upper feedback resistor (R1, R3) on VGH and VGL outputs can be used to provide more overdrive for the error comparator. This feed-forward capacitor helps to reduce the output ripple voltage. A good starting value is 10 pF.

DIODE SELECTION

To achieve high efficiency, use a Schottky diode. The voltage rating must be higher than the input voltage plus the absolute value of the negative output. The current rating of the diode must meet the converter peak inductor-current rating when servicing the VGL output. The main parameter affecting the efficiency of the converter is the forward voltage and the reverse leakage current of the diode, both should be as low as possible.

The following diodes from different suppliers listed in Table 2 have been used with the TPS6512x converter.

Table 2. List of Diodes

MANUFACTURER	REFERENCE	REVERSE VOLTAGE
ROHM	RB521G-30	30 V
VISHAY	BAT54-HT3	30 V
ZETEX	ZUMD54	30 V

CAPACITOR SELECTION

The TPS65120 converter requires six capacitors. The input capacitor is primarily a function of the board layout. In designs with long traces, for good input filtering, we recommend a ceramic input capacitor (X5R/X7R type) of at least 1 μF placed as close as possible to the converter.

To operate properly, the TPS6512x requires a bootstrap capacitor of 1 μF (or larger) on the BOOT output. Additionally the minimum BOOT capacitance must be larger than two times the capacitor value connected to the MAIN and AUXILIARY LDO outputs (in case LDO AUX is connected to the BOOT output).

The TPS6512x peak-current control scheme is inherently stable. The filtering capacitors on VGH and VGL outputs are basically determined as a function of the required current and permissible ripple voltage. For small form-factor TFT-LCD applications, typical values in the range of 100 nF to 1 μF are usually required. A good starting point is 220 nF. For high output power on VGH and VGL outputs, the capacitance may need to approach 2 μF .

For stable operation, TPS6512x requires a 220-nF ceramic capacitor on the MAIN and AUXILIARY LDO outputs. Larger capacitor values can be used to achieve lower output-voltage noise without sacrificing stability.

In general, ceramic X5R types are strongly recommended for their low ESR and ESL and capacitance-versus-bias-voltage stability. Be certain that the capacitors used are rated for the maximum voltage with adequate safety margin.

LAYOUT CONSIDERATIONS

As for all switching power supplies, the layout is an important step in the design. If the layout is not carefully done, the regulator could become unstable, displaying double or missing pulses as well as EMI problems. Therefore, use wide, short traces for the main current paths. Route these traces first.

Place the input capacitor as close as possible to the IC pins as well as the inductor and output capacitors. Place the inductor and diode as close as possible to the switch pins to minimize noise coupling into other circuits.

Use a common ground node for power ground and a different one for control ground (AGND) to minimize the effects of ground noise. Connect these ground nodes together (star point) at any place close to one of the ground pins of the IC and make sure that small-signal components returning to the AGND pin do not share the switching-current paths.

Feedback pins and divider networks are high-impedance nodes and should therefore be routed away from the inductor and shielded with a ground plane or trace to minimize noise coupling into the control loop.

APPLICATION EXAMPLES

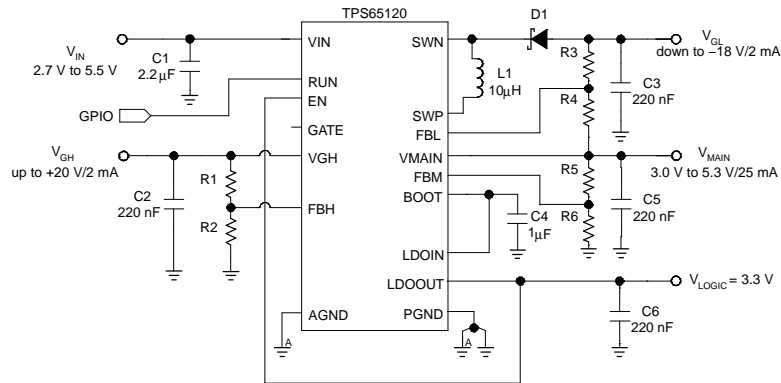
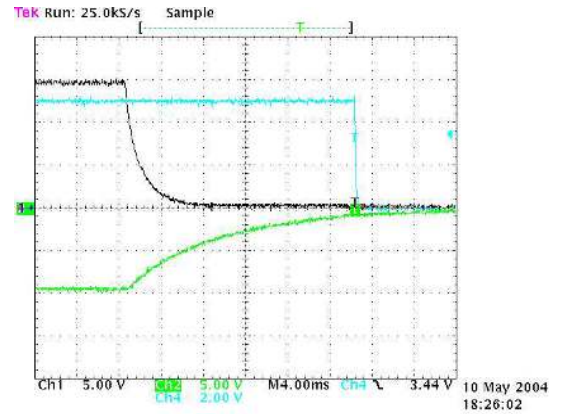
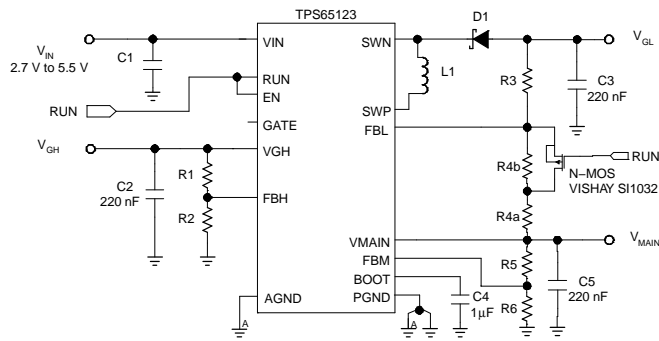


Figure 23. Complete TFT-LCD Power Supply from 1 cell Li-Ion

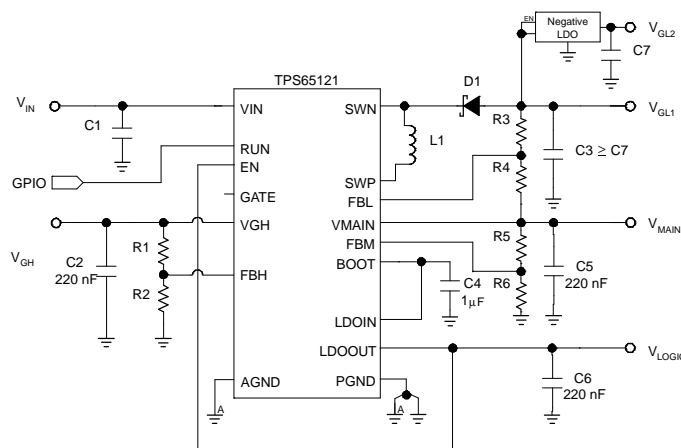


$$|V_{GL}| = V_{MAIN} \times \frac{R_3}{R_{4a}}$$

$$R_{4b} = R_3 \left(\frac{1.2 - V_{MAIN}}{V_{GL_OFFThreshold} - 1.2} \right) - R_{4a}$$

$V_{MAIN} = 5.0\text{ V}$, $V_{GH} = 15\text{ V}$, $V_{GL} = -10\text{ V}$
 $R_3 = 540\text{ k}\Omega$, $R_{4a} = 270\text{ k}\Omega$, $R_{4b} = 680\text{ k}\Omega$

Figure 24. $V_{GL} \rightarrow V_{MAIN}$ Power Down-Sequencing Threshold Shifting



Negative LDO = TPS723xx series

Figure 25. Additional Negative Gate Driver Voltage

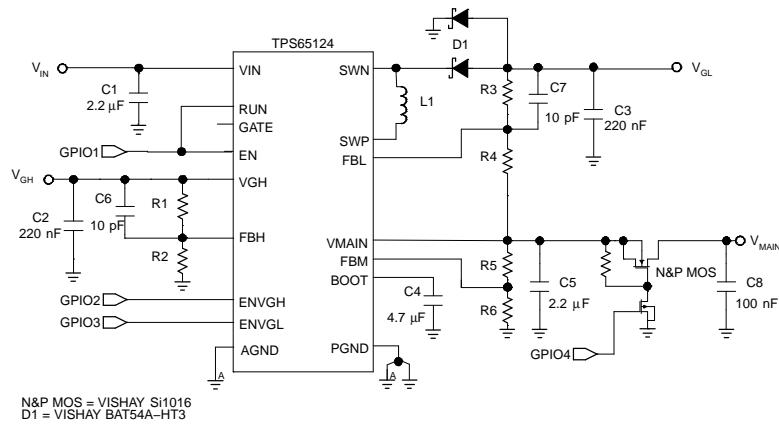


Figure 26. Fully Programmable Sequencing Featuring Very Low Gate Ripple Voltage

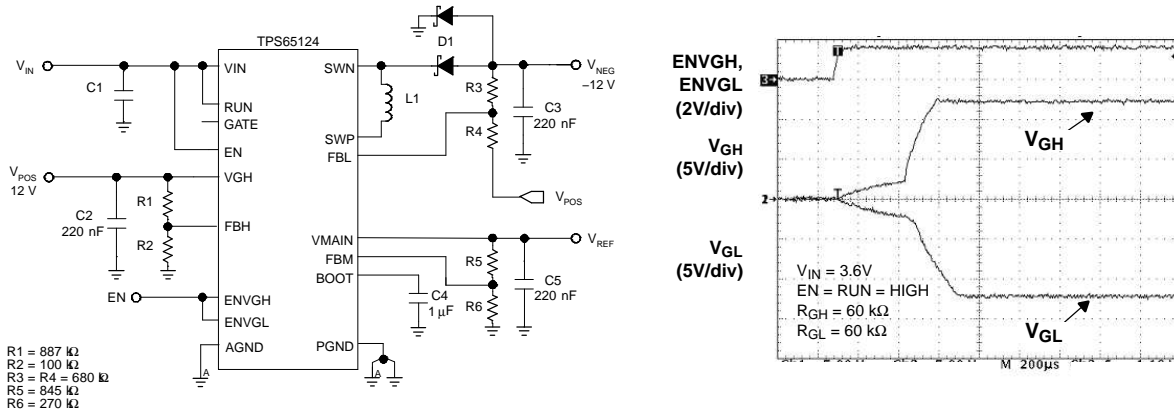


Figure 27. Dual Output Tracking Regulator with High Accuracy Reference Voltage

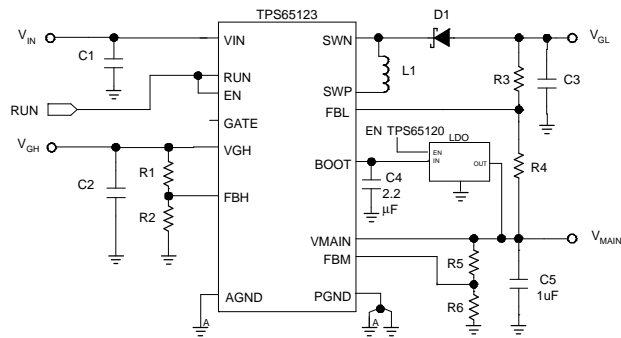


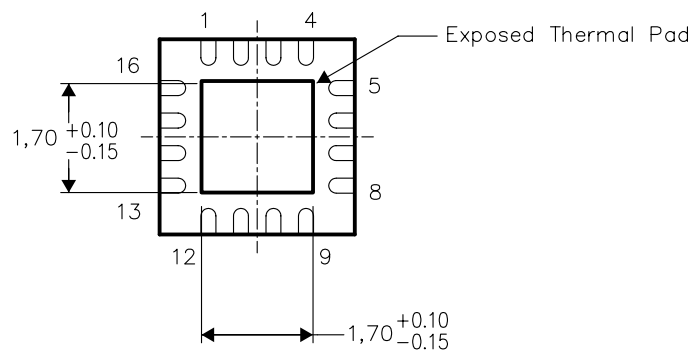
Figure 28. Boosting Main Output Current, $I_{MAIN} > 25mA$

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground plane or special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65120RGTR	ACTIVE	VQFN	RGT	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BKA	Samples
TPS65120RGTT	ACTIVE	VQFN	RGT	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BKA	Samples
TPS65121RGTR	ACTIVE	VQFN	RGT	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BKB	Samples
TPS65123RGTR	ACTIVE	VQFN	RGT	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BKC	Samples
TPS65123RGTT	ACTIVE	VQFN	RGT	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BKC	Samples
TPS65124RGTR	ACTIVE	VQFN	RGT	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BKD	Samples
TPS65124RGTT	ACTIVE	VQFN	RGT	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BKD	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

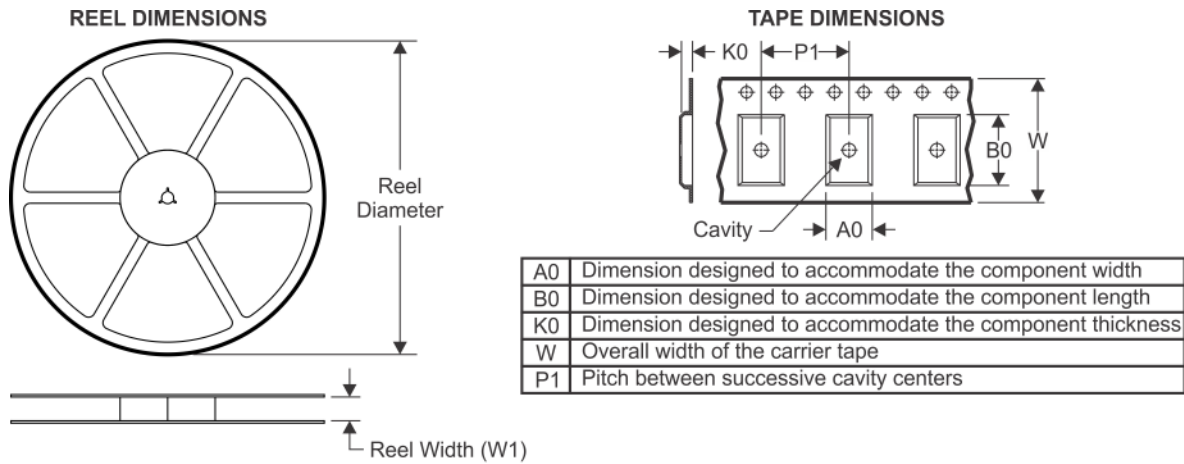
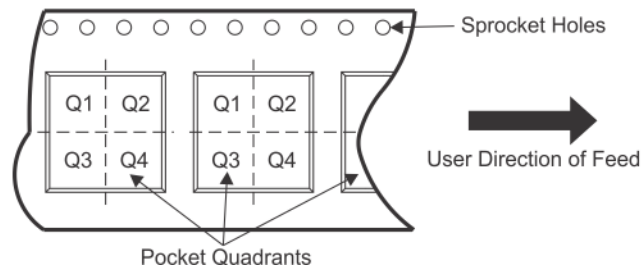
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65121RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS65123RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS65124RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

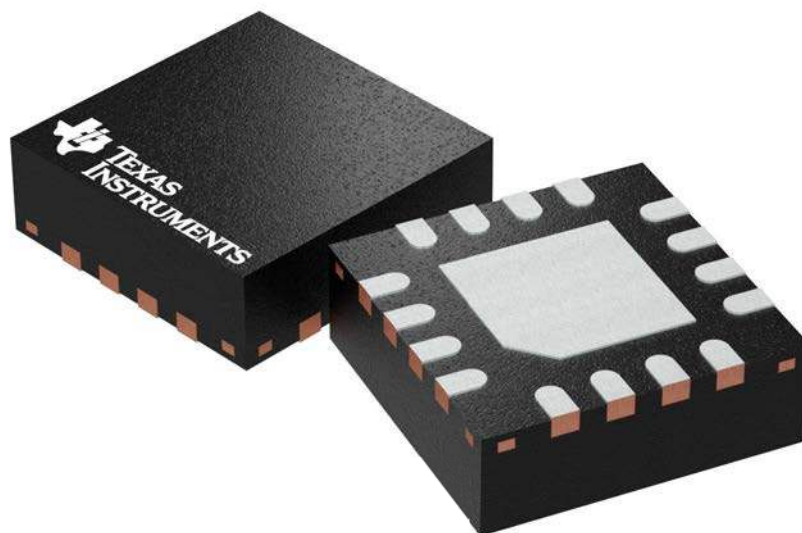
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65121RGTR	VQFN	RGT	16	3000	350.0	350.0	43.0
TPS65123RGTR	VQFN	RGT	16	3000	350.0	350.0	43.0
TPS65124RGTR	VQFN	RGT	16	3000	350.0	350.0	43.0

RGT 16

GENERIC PACKAGE VIEW

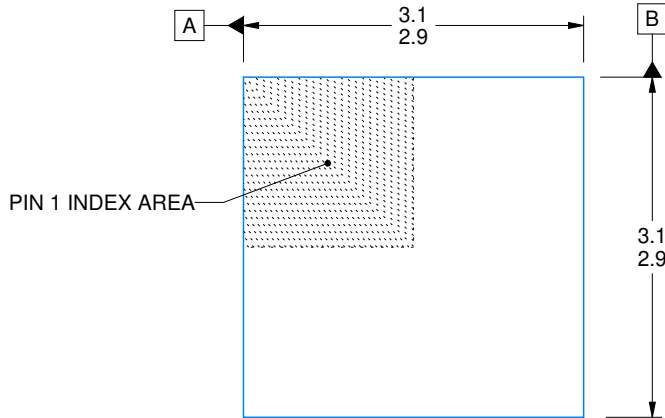
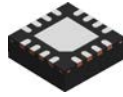
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

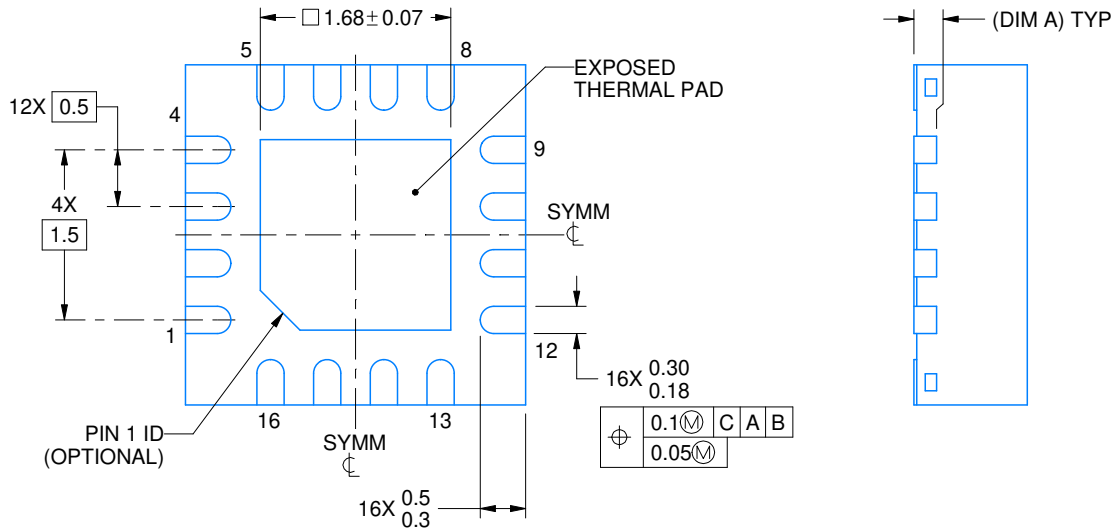
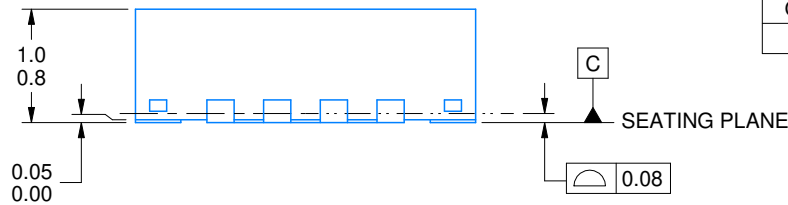


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203495/1



SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2



4222419/D 04/2022

NOTES:

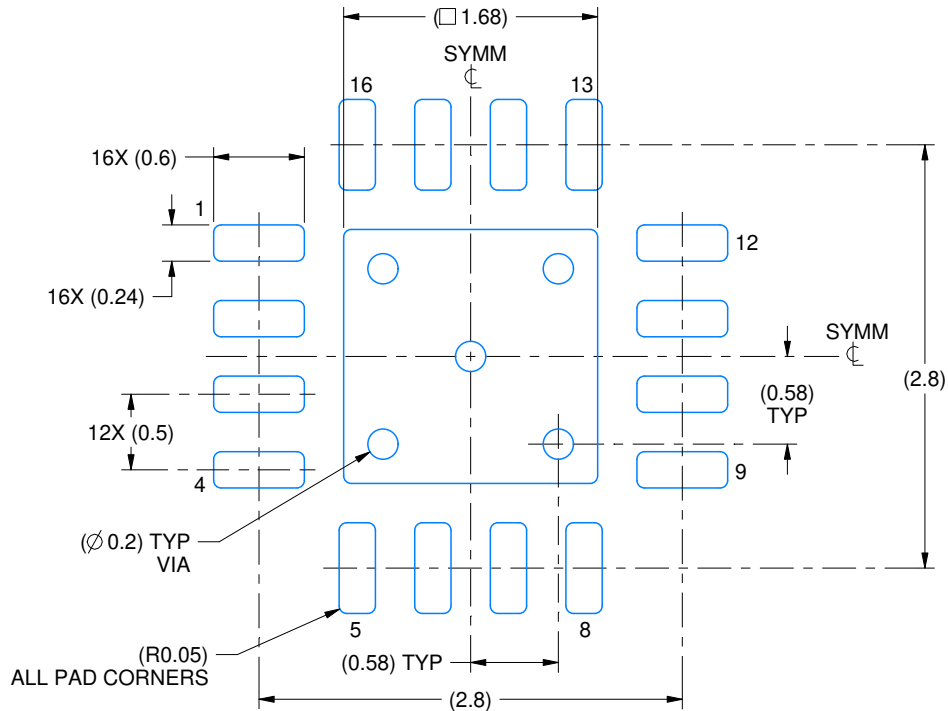
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

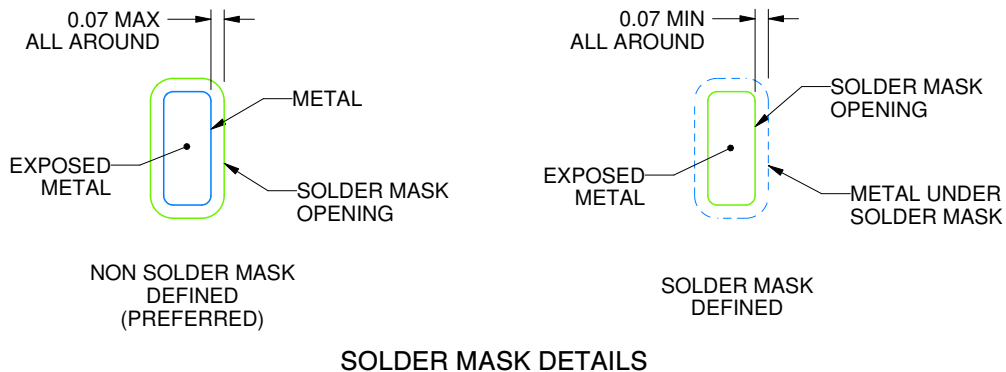
RGT0016C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4222419/D 04/2022

NOTES: (continued)

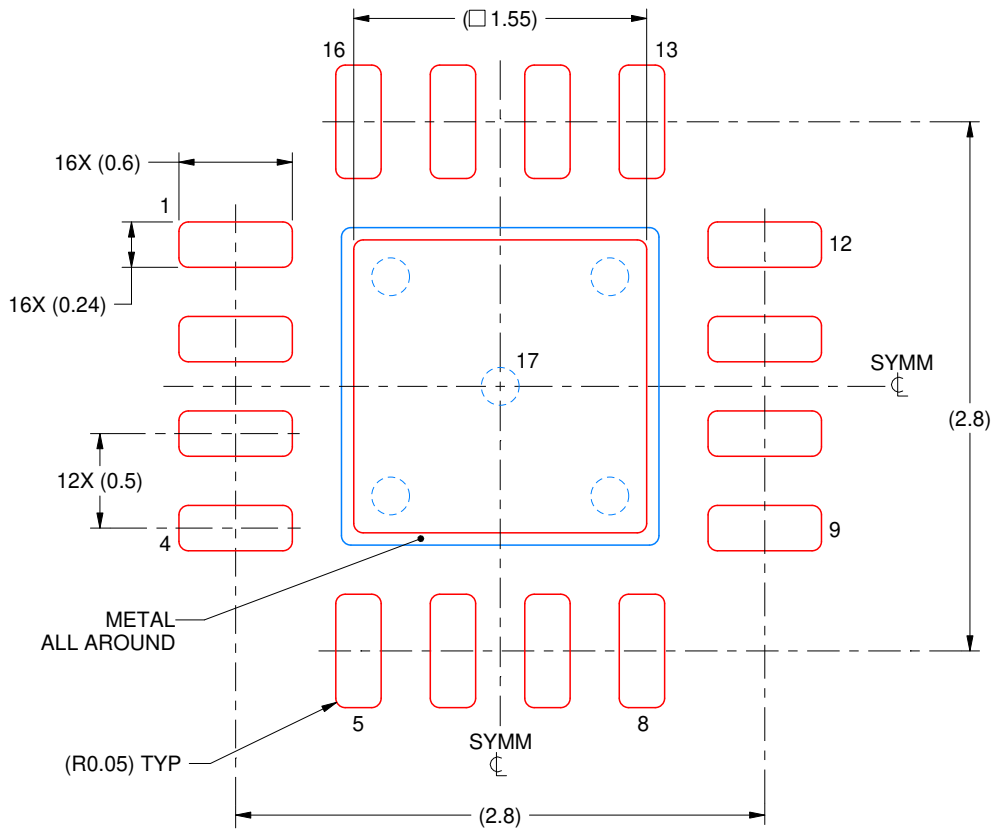
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGT0016C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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