

# HA1630S04/05/06 Series

Ultra-Small Low Voltage Operation CMOS Single Operational Amplifier

R03DS0082EJ0200  
Rev.2.00  
Jan 10, 2014

## Description

The HA1630S04/05/06 are high slew rate single CMOS Operational Amplifiers realizing low voltage operation, low input offset voltage and low supply current. In addition to a low operating voltage from 1.8V, these device output can achieve full swing output voltage capability extending to either supply. Available in an ultra-small CMPAK-5 package that occupies only 1/8 the area of the SOP-8 package.

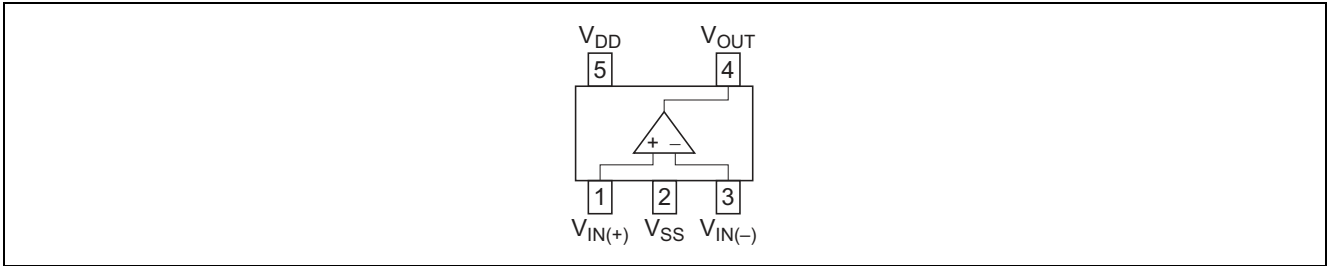
## Features

- Low power and single supply operation  $V_{DD} = 1.8$  to  $5.5$  V
- Low input offset voltage  $V_{IO} = 4.0$  mV Max
- Low supply current  $I_{DD} = 200$   $\mu$ A Typ (HA1630S04)  
 $I_{DD} = 400$   $\mu$ A Typ (HA1630S05)  
 $I_{DD} = 800$   $\mu$ A Typ (HA1630S06)
- High slew rate SR = 2 V/ $\mu$ s Typ (HA1630S04)  
SR = 4 V/ $\mu$ s Typ (HA1630S05)  
SR = 8 V/ $\mu$ s Typ (HA1630S06)
- Maximum output voltage  $V_{OH} = 2.9$  V Min (at  $V_{DD} = 3.0$  V)
- Low input bias current  $I_{IB} = 1$  pA Typ

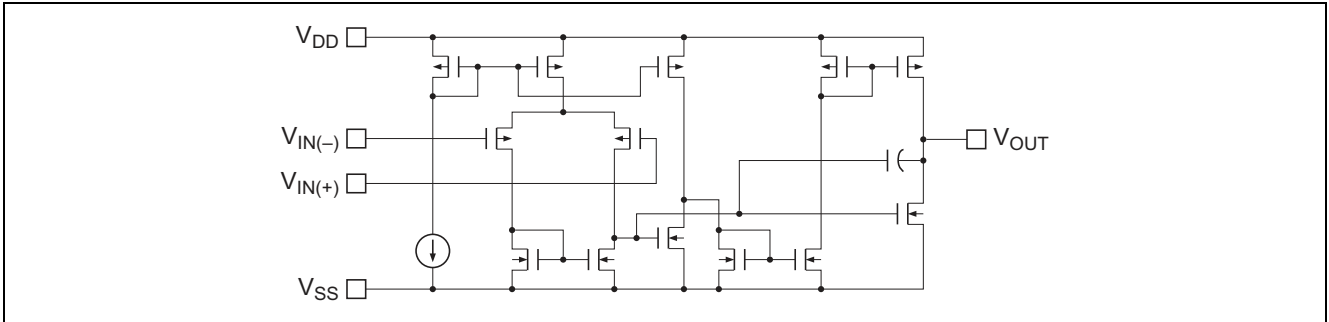
## Ordering Information

Type No.	Package Name	Package Code
HA1630S04CM	CMPAK-5	PTSP0005ZC-A
HA1630S04LP	MPAK-5	PLSP0005ZB-A
HA1630S05CM	CMPAK-5	PTSP0005ZC-A
HA1630S05LP	MPAK-5	PLSP0005ZB-A
HA1630S06CM	CMPAK-5	PTSP0005ZC-A
HA1630S06LP	MPAK-5	PLSP0005ZB-A

## Pin Arrangement



## Equivalent Circuit



## Absolute Maximum Ratings

(Ta = 25°C)

Items	Symbol	Ratings	Unit	Note
Supply voltage	V <sub>DD</sub>	7	V	
Differential input voltage	V <sub>IN(diff)</sub>	-V <sub>DD</sub> to +V <sub>DD</sub>	V	
Input voltage	V <sub>IN</sub>	-0.3 to +V <sub>DD</sub>	V	1
Power dissipation	P <sub>T</sub>	200	mW	
Operating temp. Range	Topr	-40 to +85	°C	
Storage temp. Range	Tstg	-55 to +125	°C	

Note: 1. Do not apply Input Voltage exceeding V<sub>DD</sub> or 7 V.

## Electrical Characteristics

(V<sub>DD</sub> = 3.0 V, Ta = 25°C)

Items	Symbol	Min	Typ	Max	Unit	Test Condition
Input offset voltage	V <sub>IO</sub>	—	—	4.0	mV	V <sub>in</sub> = 1.5 V
Input offset current	I <sub>IO</sub>	—	(1.0)	—	pA	V <sub>in</sub> = 1.5 V
Input bias current	I <sub>IB</sub>	—	(1.0)	—	pA	V <sub>in</sub> = 1.5 V
Output high voltage	V <sub>OH</sub>	2.9	—	—	V	R <sub>L</sub> = 100 kΩ
Output source current	I <sub>O SOURCE</sub>	100	200	—	μA	V <sub>OH</sub> = 2.5 V (HA1630S04)
		200	400	—		V <sub>OH</sub> = 2.5 V (HA1630S05)
		400	800	—		V <sub>OH</sub> = 2.5 V (HA1630S06)
Output low voltage	V <sub>OL</sub>	—	—	0.1	V	R <sub>L</sub> = 100 kΩ
Output sink current	I <sub>O SINK</sub>	—	(5.0)	—	mA	V <sub>OL</sub> = 0.5 V (HA1630S04)
		—	(6.0)	—		V <sub>OL</sub> = 0.5 V (HA1630S05)
		—	(6.5)	—		V <sub>OL</sub> = 0.5 V (HA1630S06)
Common mode input voltage range	V <sub>CM</sub>	-0.05 to 2.1	—	—	V	(HA1630S04, HA1630S05)
		0 to 1.9	—	—		(HA1630S06)
Slew rate	SR	—	(2.0)	—	V/μs	C <sub>L</sub> = 20 pF (HA1630S04)
		—	(4.0)	—		C <sub>L</sub> = 20 pF (HA1630S05)
		—	(8.0)	—		C <sub>L</sub> = 20 pF (HA1630S06)
Voltage gain	A <sub>V</sub>	60	90	—	dB	
Gain bandwidth product	BW	—	(2.1)	—	MHz	C <sub>L</sub> = 20 pF (HA1630S04)
		—	(3.3)	—		C <sub>L</sub> = 20 pF (HA1630S05)
		—	(3.6)	—		C <sub>L</sub> = 20 pF (HA1630S06)
Power supply rejection ratio	PSRR	50	70	—	dB	
Common mode rejection ratio	CMRR	50	70	—	dB	
Supply current	I <sub>DD</sub>	—	200	400	μA	R <sub>L</sub> = ∞ (HA1630S04)
		—	400	800		R <sub>L</sub> = ∞ (HA1630S05)
		—	800	1700		R <sub>L</sub> = ∞ (HA1630S06)

Notes: 1. In the case of continuous current flow, use a sink current of under 4 mA.

2. ( ) : Design specification

## Table of Graphs

Electrical Characteristics			HA1630S04 Figure	HA1630S05 Figure	HA1630S06 Figure	Test Circuit
Supply current	$I_{DD}$	vs Supply voltage	1-1	2-1	3-1	2
		vs Ambient temperature	1-2	2-2	3-2	
Output high voltage	$V_{OH}$	vs Output source current	1-3	2-3	3-3	4
		vs Supply voltage	1-4	2-4	3-4	
Output source current	$I_{O\ SOURCE}$	vs Ambient temperature	1-5	2-5	3-5	6
Output low voltage	$V_{OL}$	vs Output sink current	1-6	2-6	3-6	5
Output sink current	$I_{O\ SINK}$	vs Ambient temperature	1-7	2-7	3-7	6
Input offset voltage	$V_{IO}$	Distribution	1-8	2-8	3-8	1
		vs Supply voltage	1-9	2-9	3-9	
		vs Ambient temperature	1-10	2-10	3-10	
Common mode input voltage range	$V_{CM}$	vs Ambient temperature	1-11	2-11	3-11	7
Power supply rejection ratio	PSRR	vs Frequency	1-12	2-12	3-12	1
Common mode rejection ratio	CMRR	vs Frequency	1-13	2-13	3-13	7
Voltage gain & phase angle	$A_V$	vs Frequency	1-14	2-14	3-14	10
Input bias current	$I_{IB}$	vs Ambient temperature	1-15	2-15	3-15	3
		vs Input voltage	1-16	2-16	3-16	
Slew Rate (rising)	SRr	vs Ambient temperature	1-17	2-17	3-17	9
Slew Rate (falling)	SRf	vs Ambient temperature	1-18	2-18	3-18	
Slew rate		Large signal transient response	1-19	2-19	3-19	
		Small signal transient response	1-20	2-20	3-20	
Total harmonic distortion + noise	(0 dB)	vs. Output voltage p-p	1-21	2-21	3-21	8
	(40 dB)	vs. Output voltage p-p	1-22	2-22	3-22	
Maximum p-p output voltage		vs Frequency	1-23	2-23	3-23	
Voltage noise density		vs Frequency	1-24	2-24	3-24	

### Main Characteristics (HA1630S04)

Figure 1-1. HA1630S04  
Supply Current vs. Supply Voltage

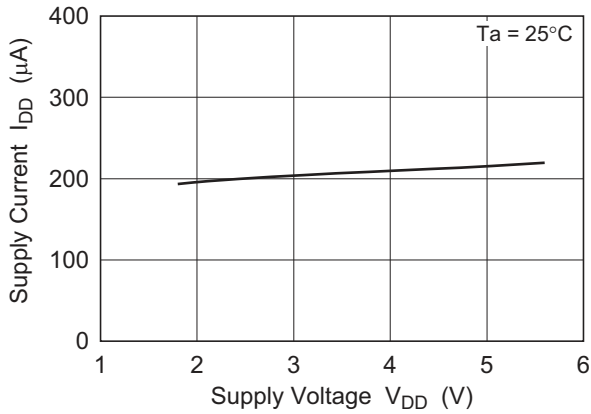


Figure 1-2. HA1630S04  
Supply Current vs. Ambient Temperature

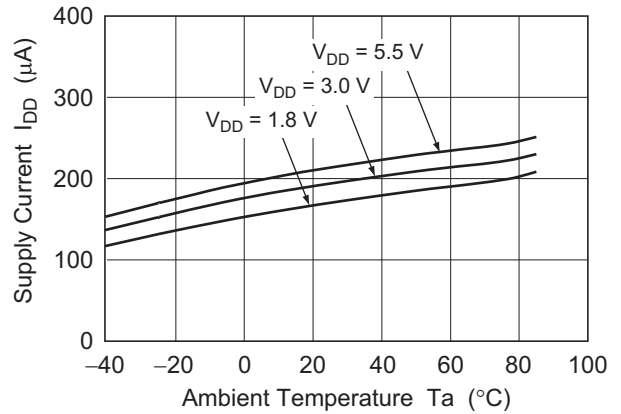


Figure 1-3. HA1630S04  
Output High Voltage vs. Output Source Current

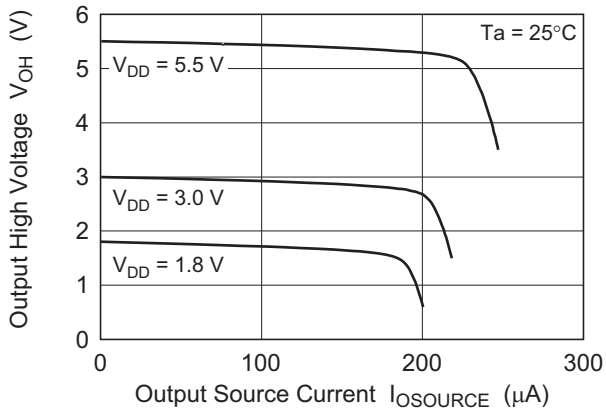


Figure 1-4. HA1630S04  
Output High Voltage vs. Supply Voltage

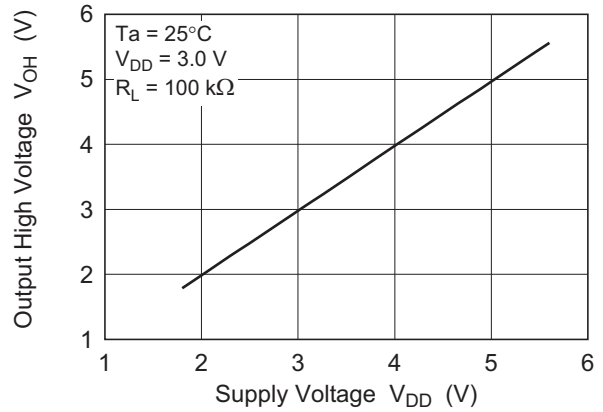
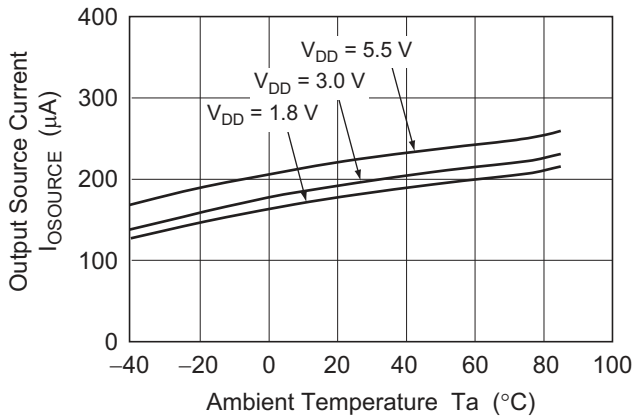


Figure 1-5. HA1630S04  
Output Source Current vs. Ambient Temperature



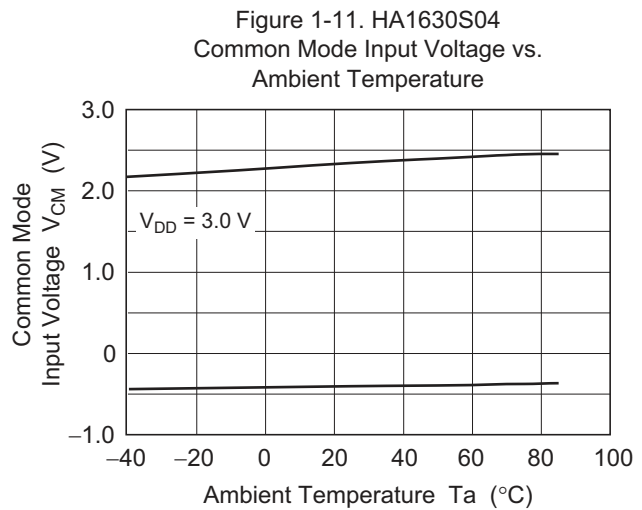
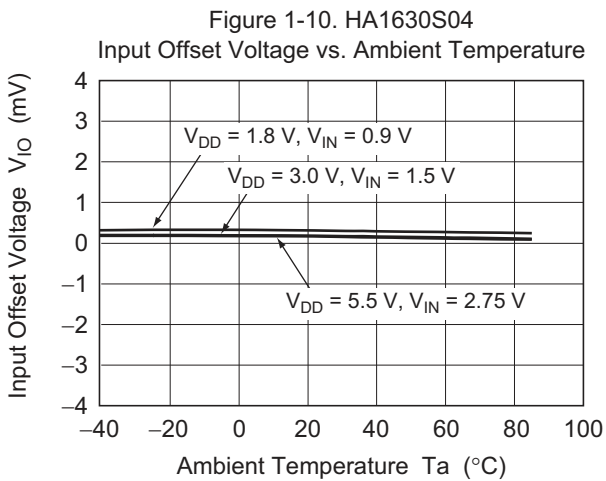
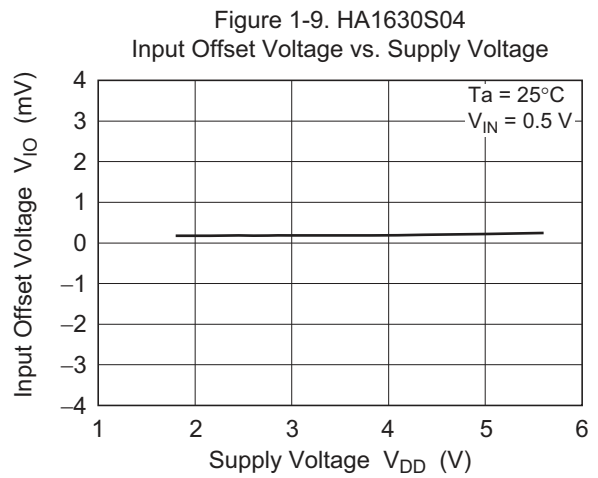
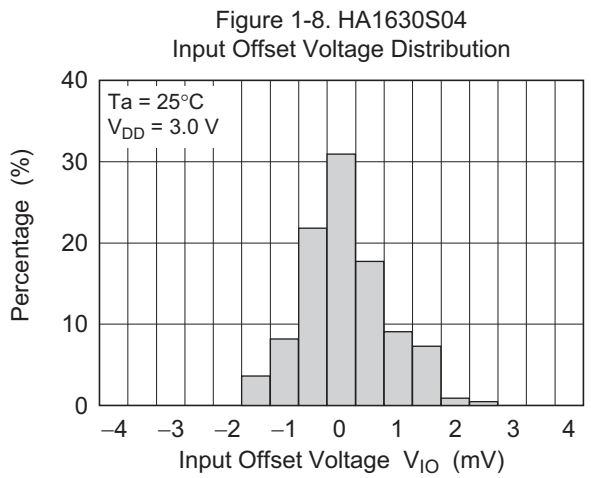
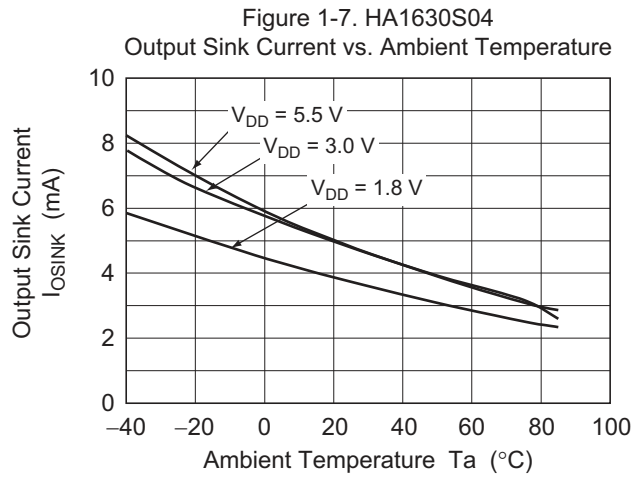
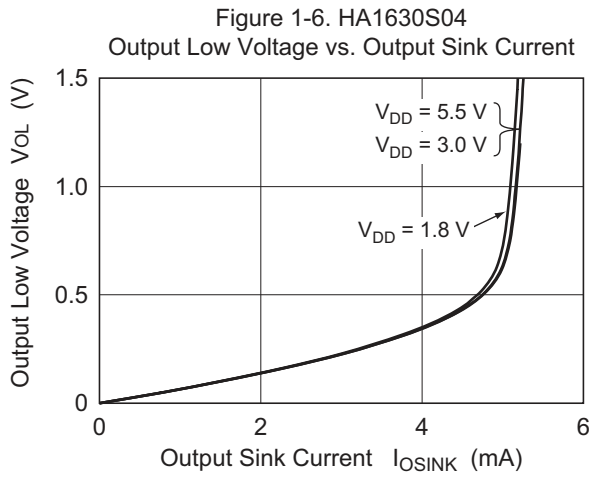


Figure 1-12. HA1630S04  
Power Supply Rejection Ratio vs. Frequency

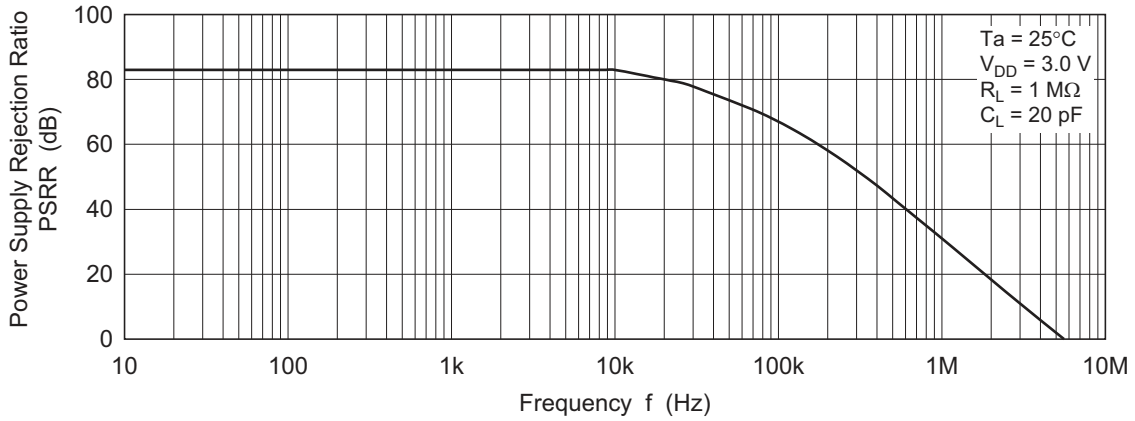


Figure 1-13. HA1630S04  
Common Mode Rejection Ratio vs. Frequency

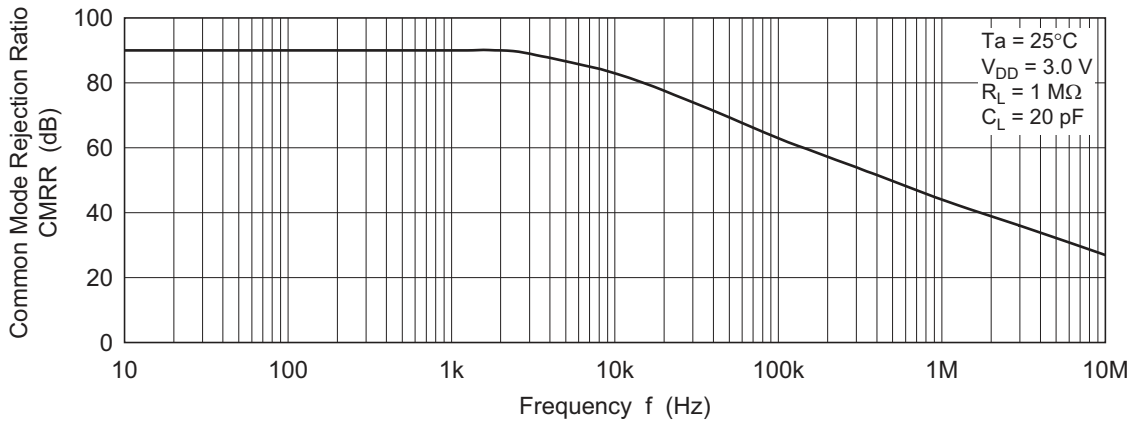
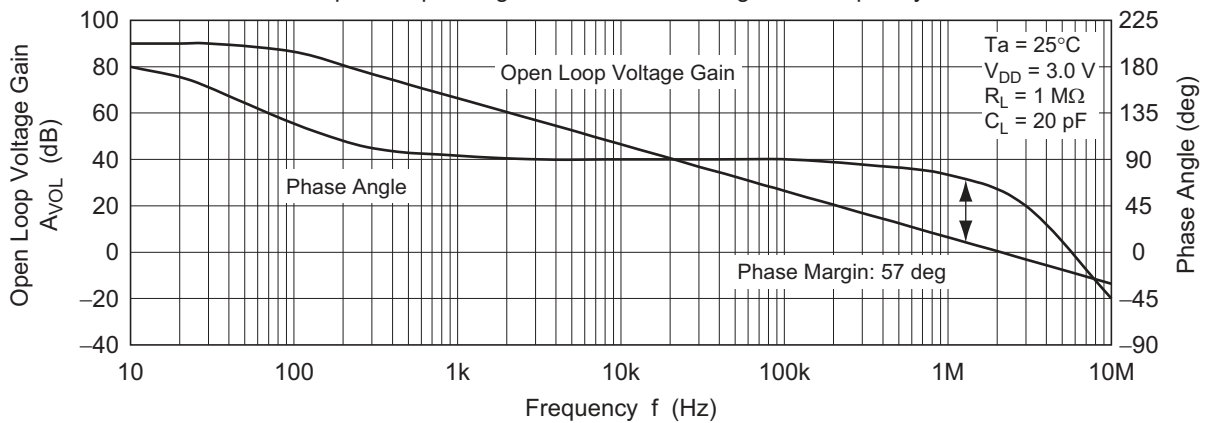


Figure 1-14. HA1630S04  
Open Loop Voltage Gain and Phase Angle vs. Frequency



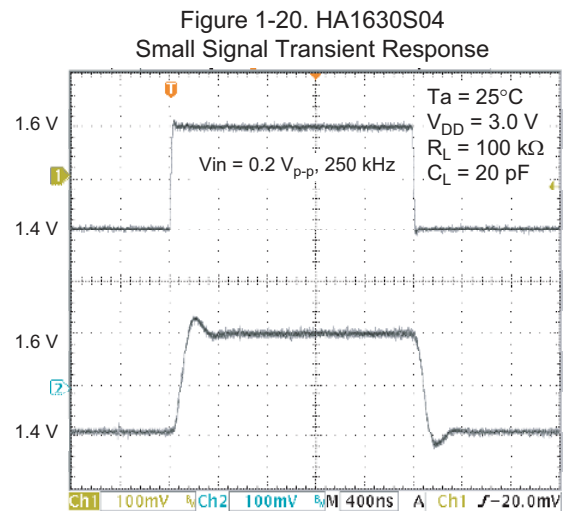
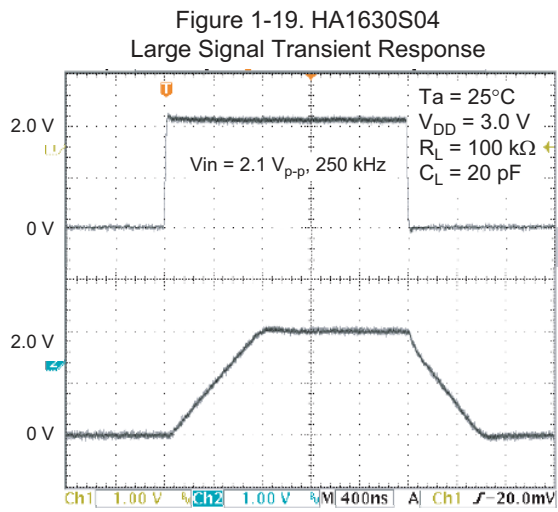
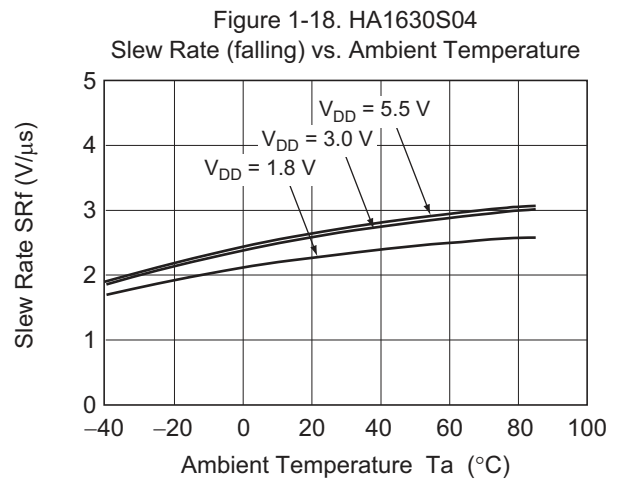
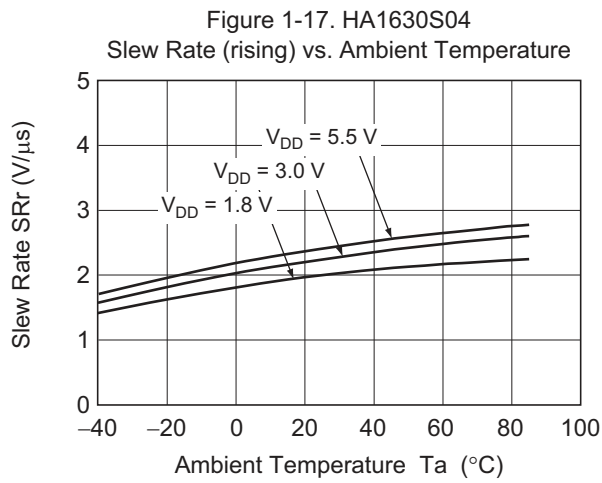
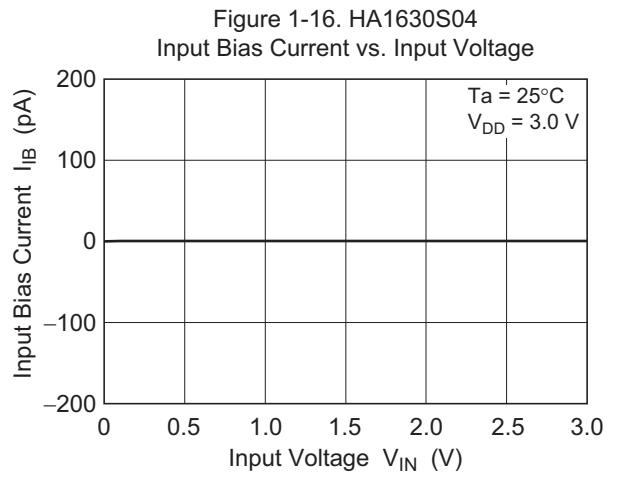
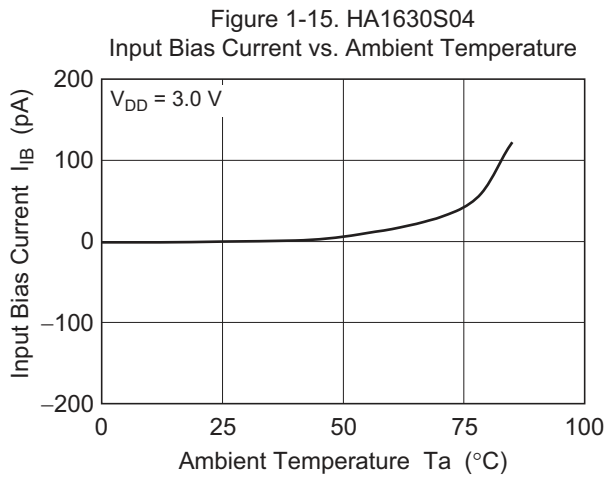




Figure 1-21. HA1630S04  
Total Harmonic Distortion + Noise vs.  
Output Voltage p-p

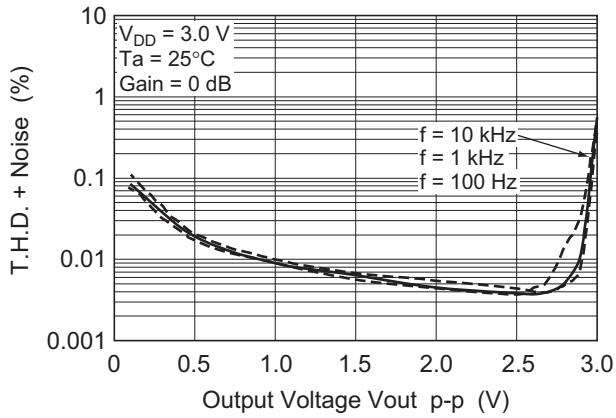


Figure 1-22. HA1630S04  
Total Harmonic Distortion + Noise vs.  
Output Voltage p-p

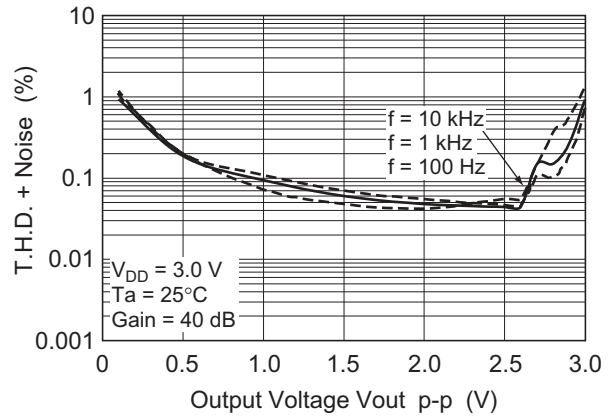


Figure 1-23. HA1630S04  
Voltage Output p-p vs. Frequency

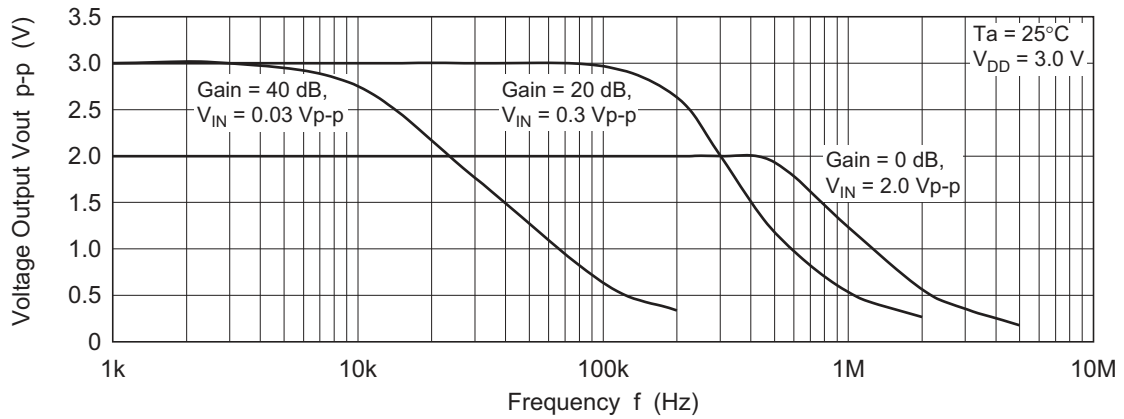
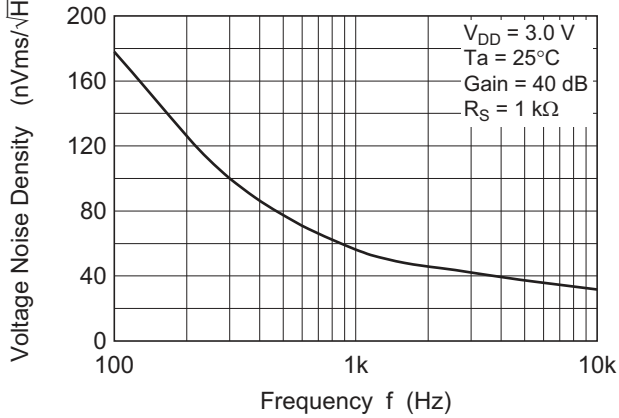
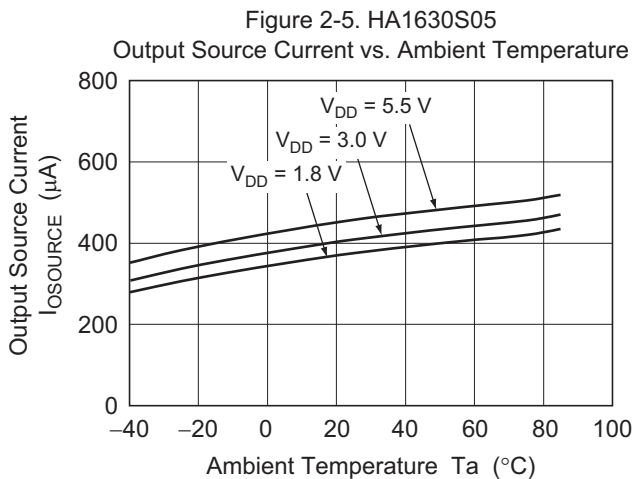
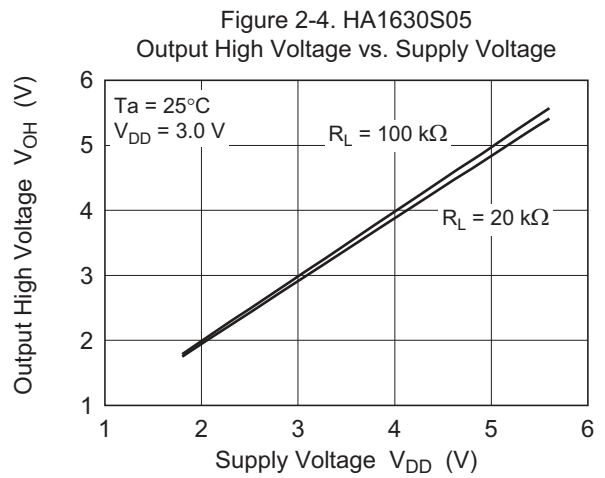
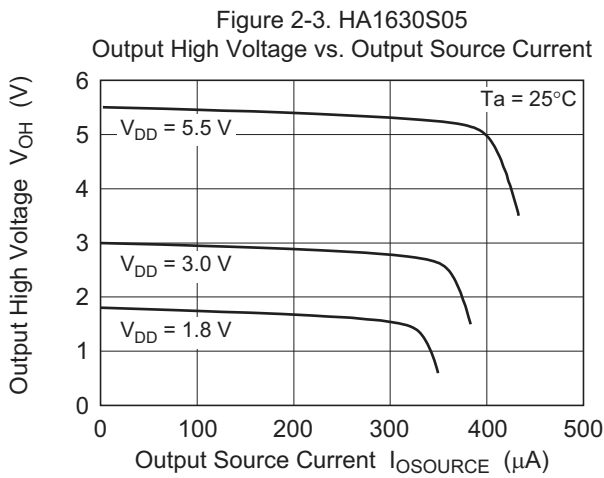
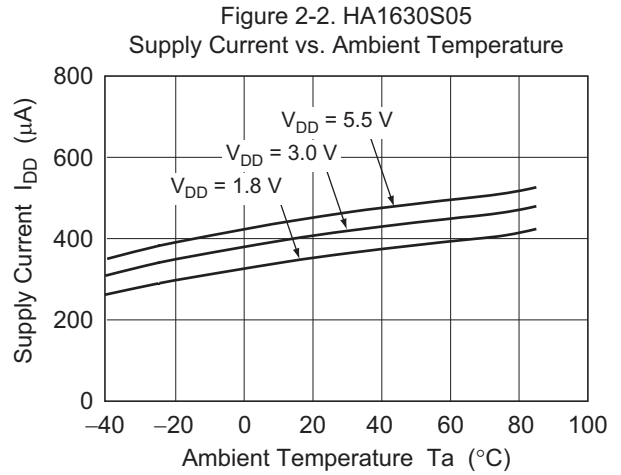
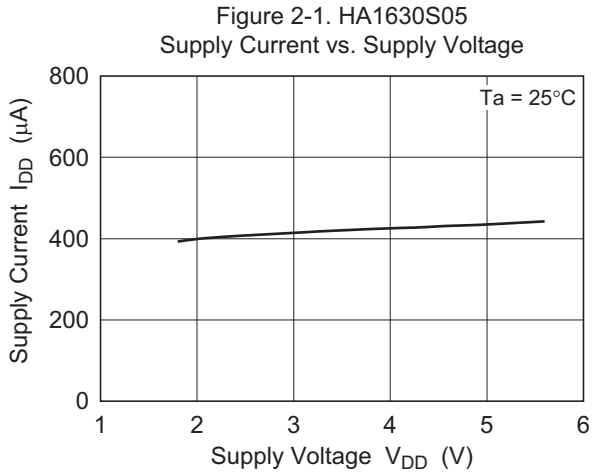


Figure 1-24. HA1630S04  
Voltage Noise Density vs. Frequency



Main Characteristics (HA1630S05)



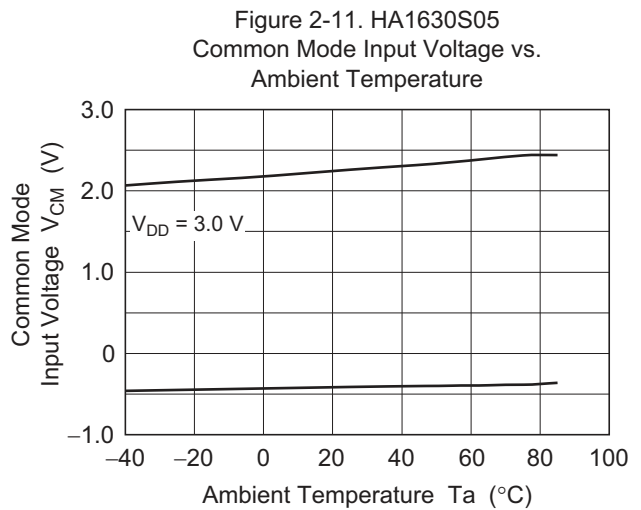
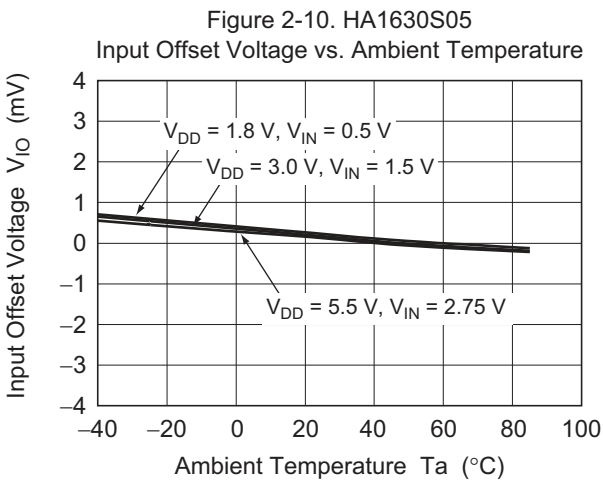
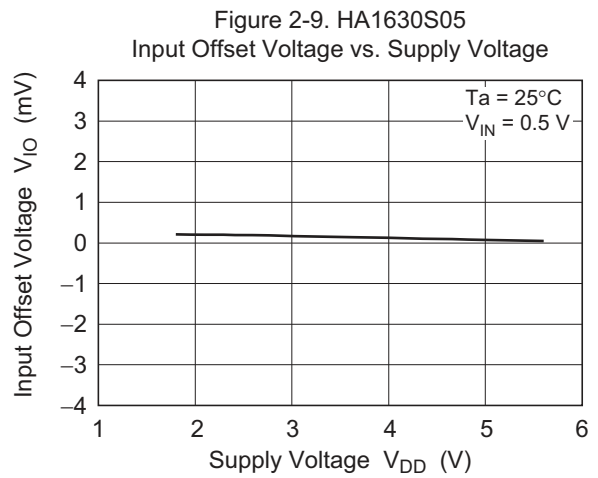
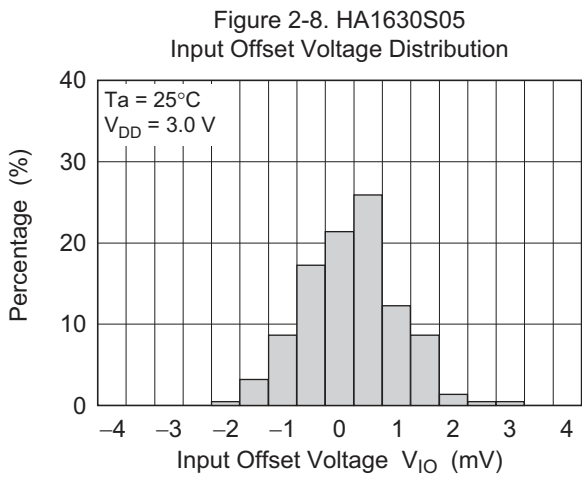
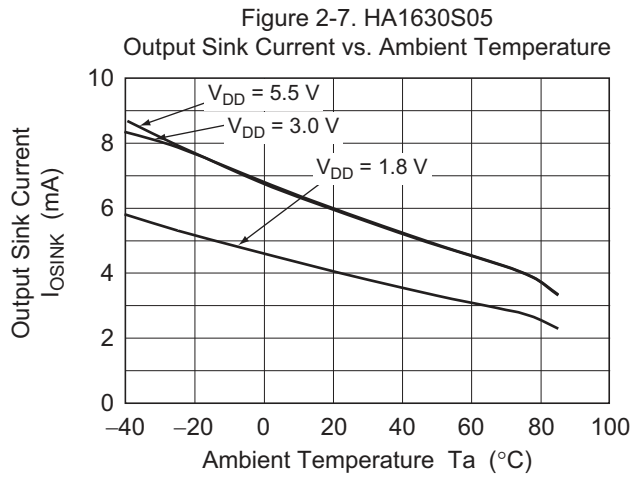
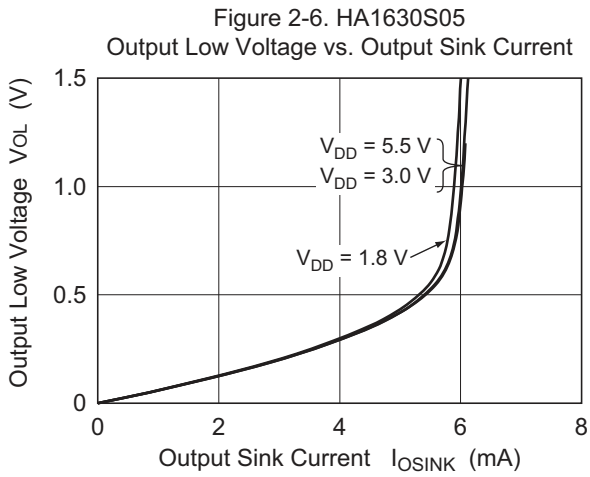


Figure 2-12. HA1630S05  
Power Supply Rejection Ratio vs. Frequency

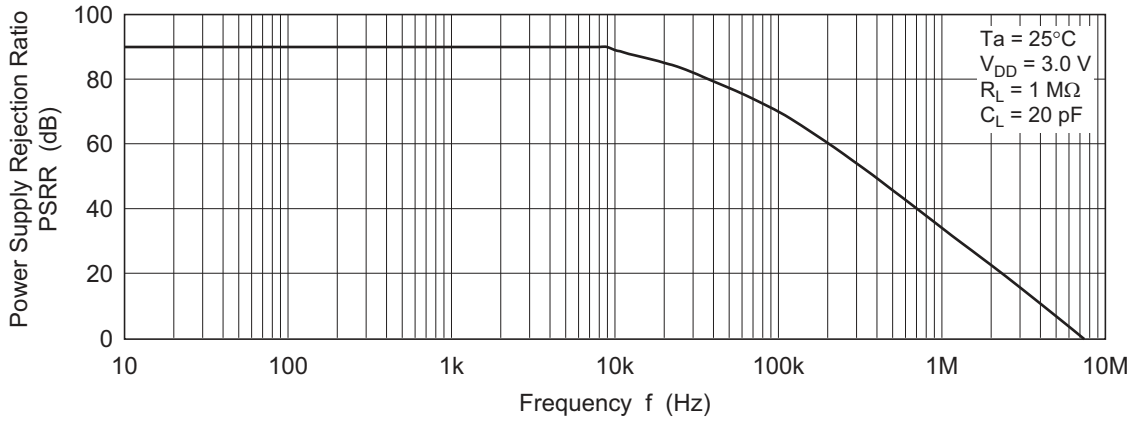


Figure 2-13. HA1630S05  
Common Mode Rejection Ratio vs. Frequency

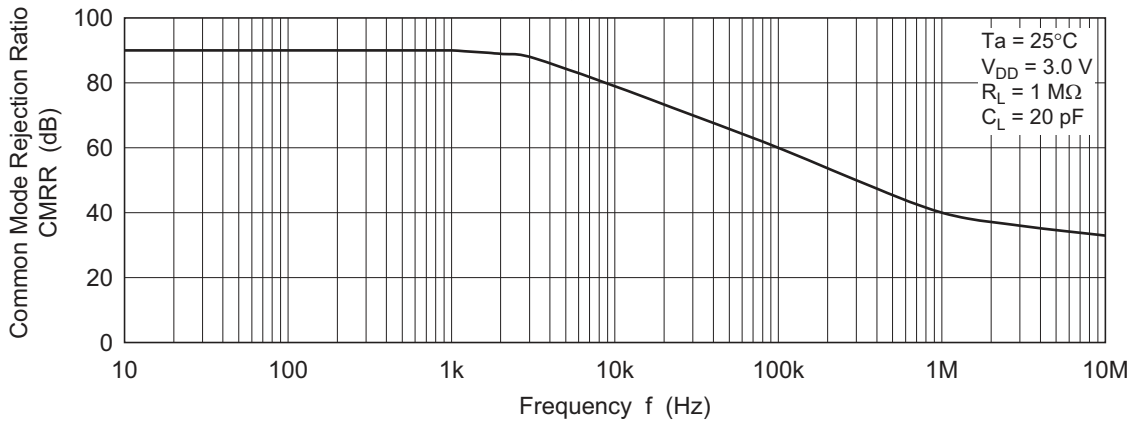
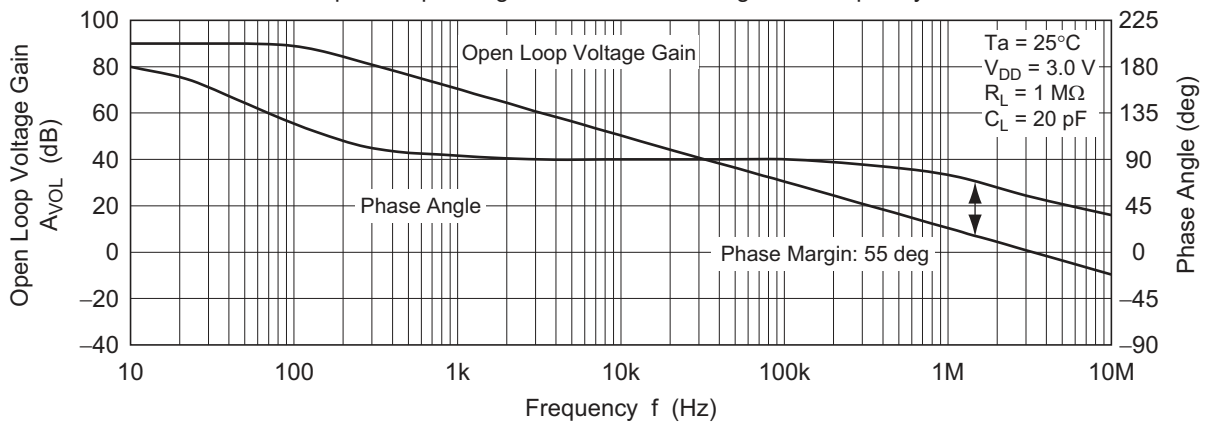


Figure 2-14. HA1630S05  
Open Loop Voltage Gain and Phase Angle vs. Frequency



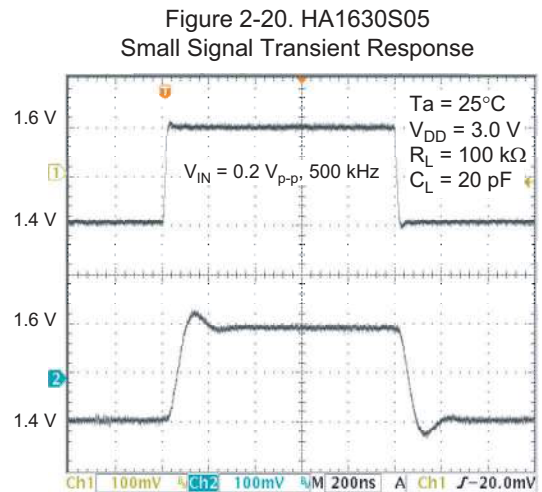
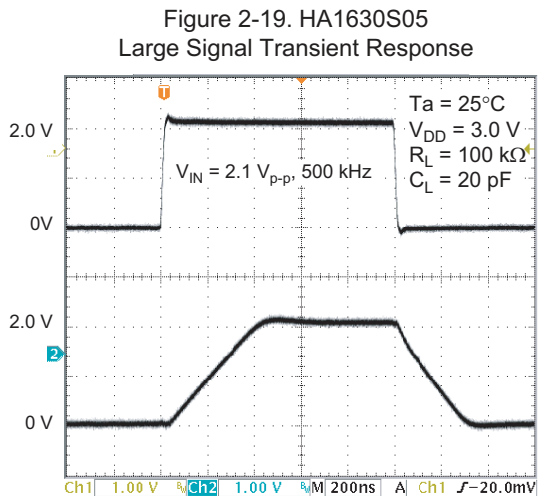
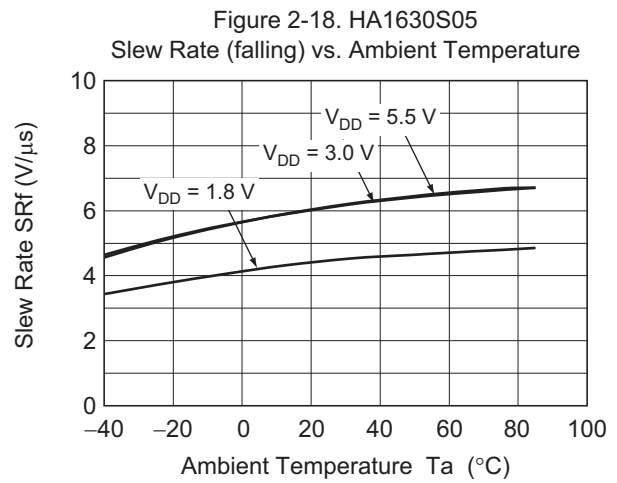
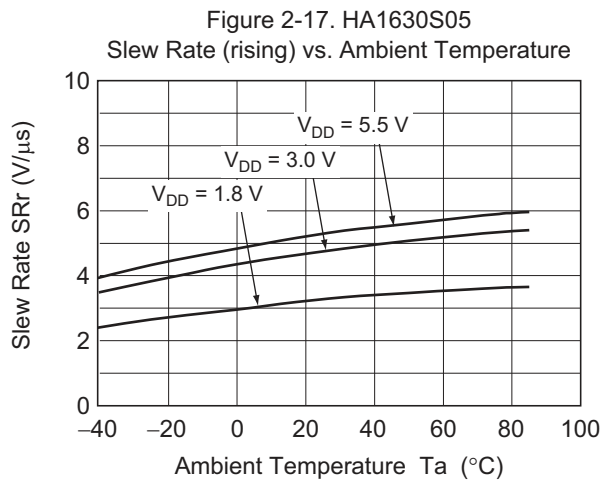
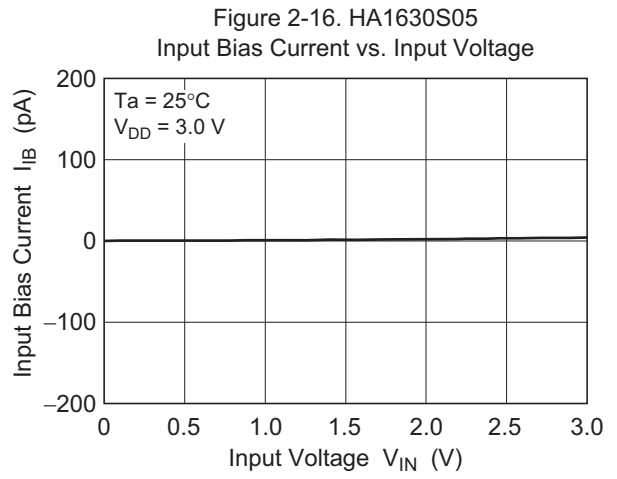
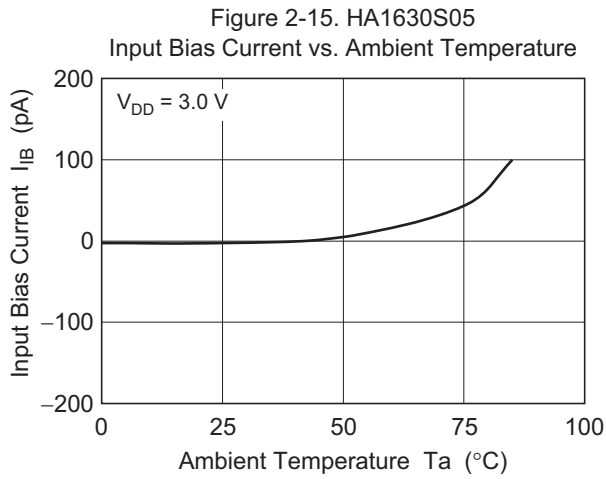


Figure 2-21. HA1630S05  
Total Harmonic Distortion + Noise vs.  
Output Voltage p-p

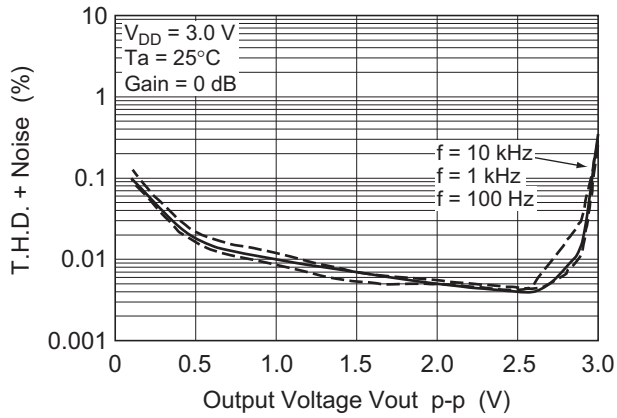


Figure 2-22. HA1630S05  
Total Harmonic Distortion + Noise vs.  
Output Voltage p-p

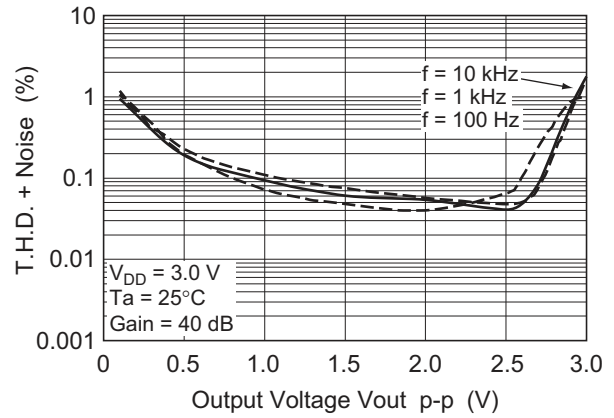


Figure 2-23. HA1630S05  
Voltage Output p-p vs. Frequency

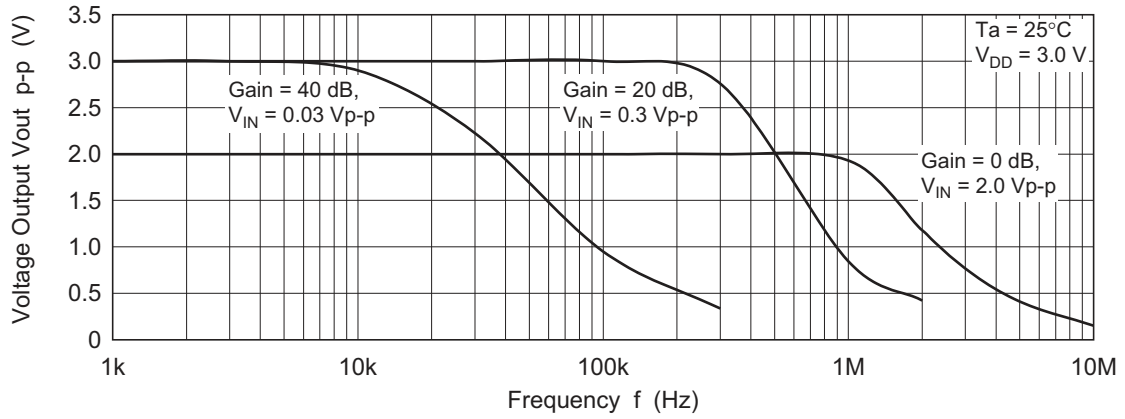
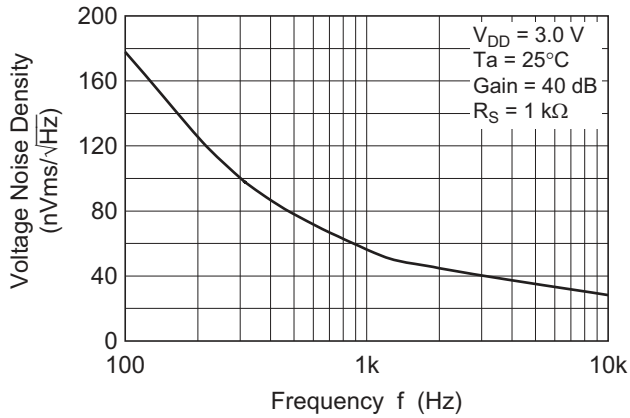
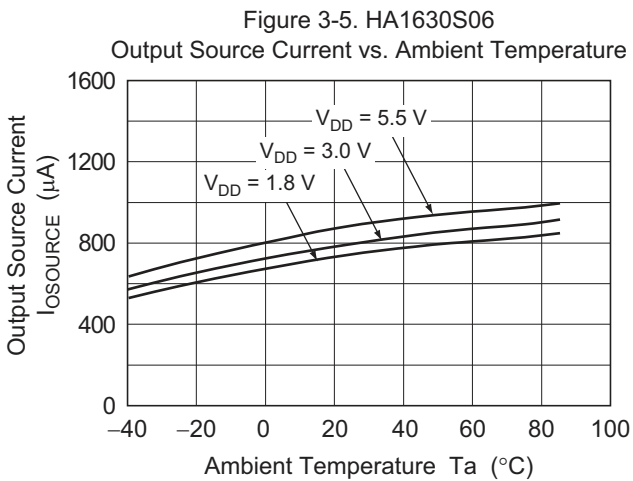
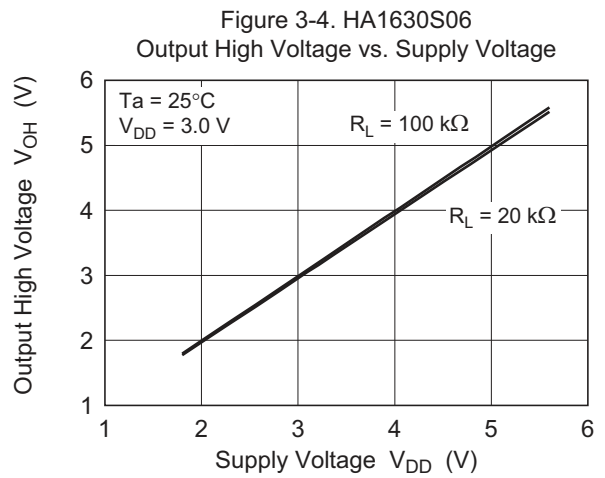
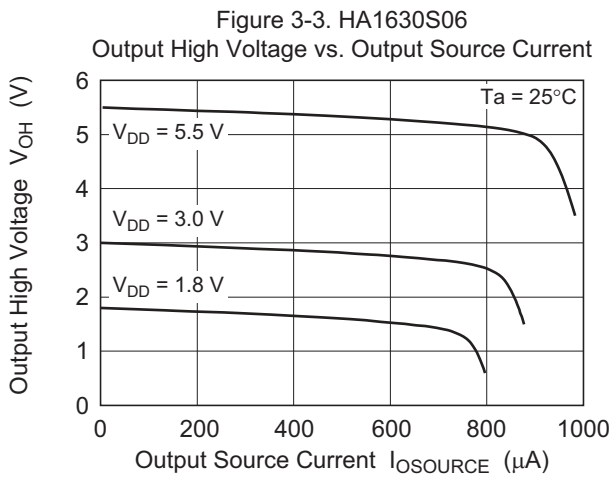
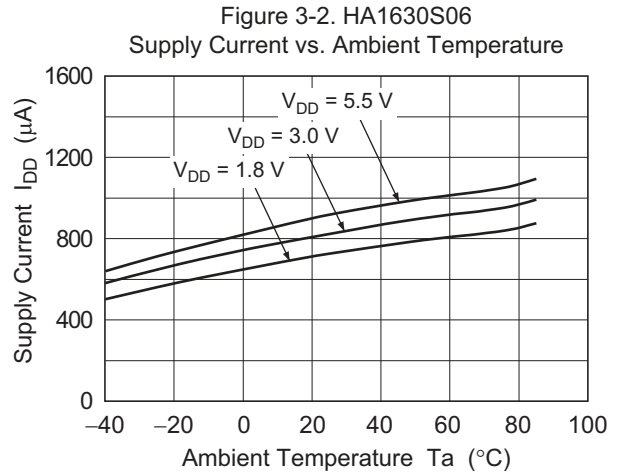
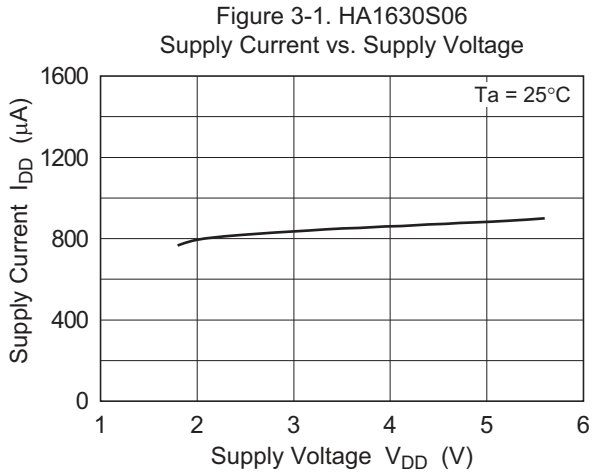


Figure 2-24. HA1630S05  
Voltage Noise Density vs. Frequency



Main Characteristics (HA1630S06)



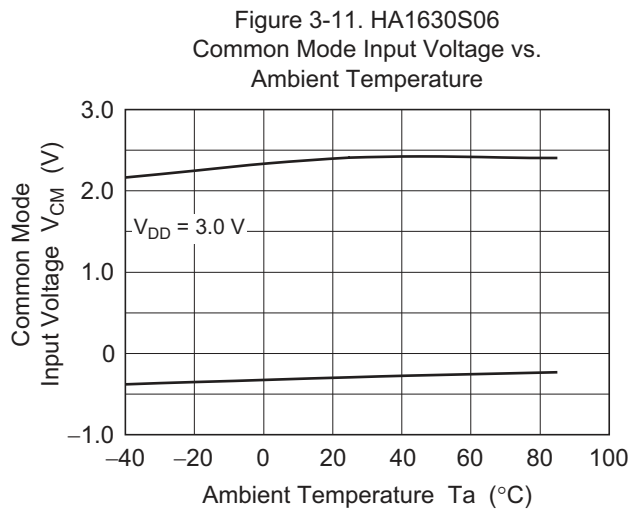
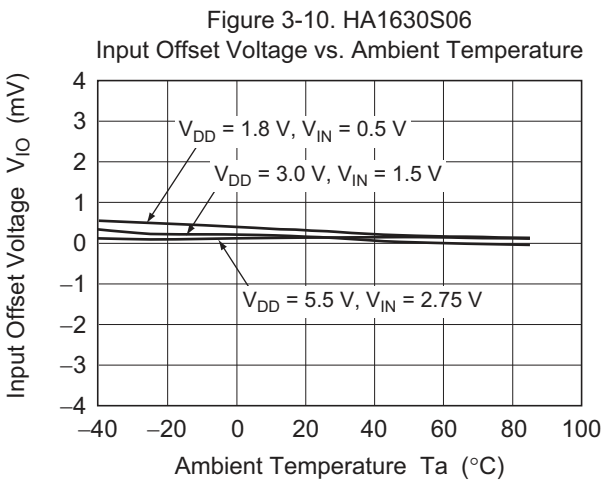
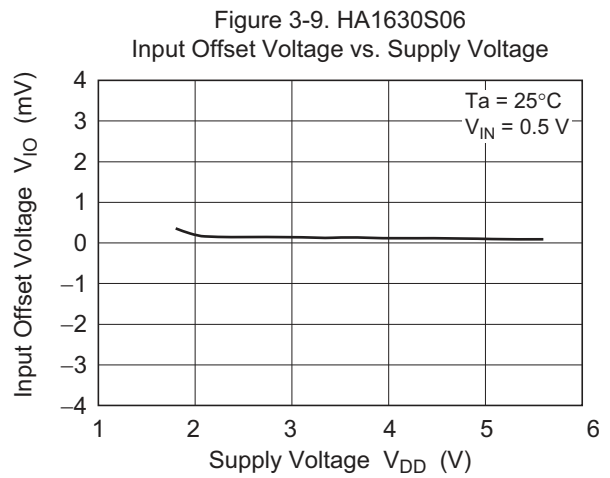
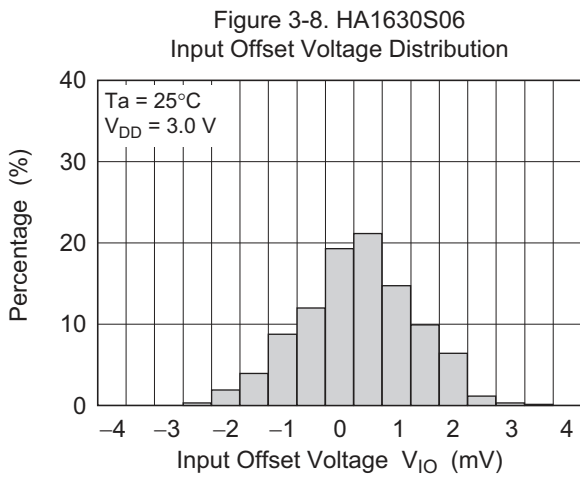
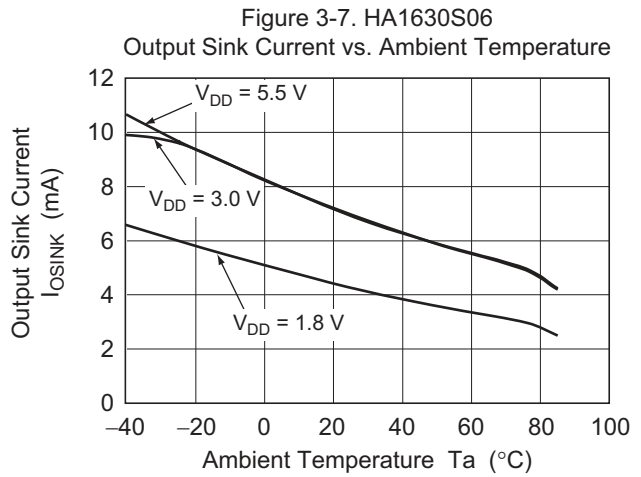
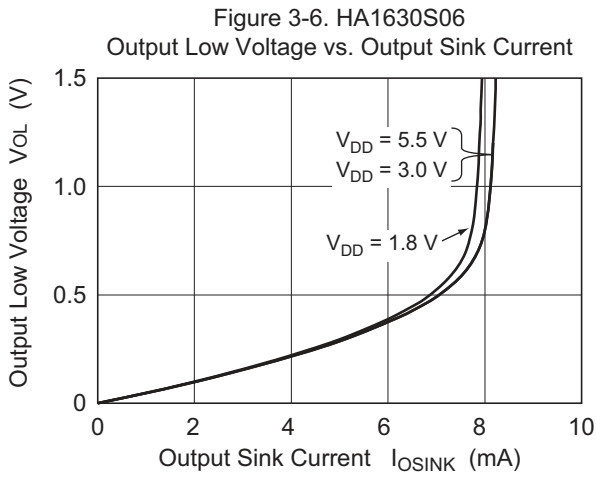




Figure 3-12. HA1630S06  
Power Supply Rejection Ratio vs. Frequency

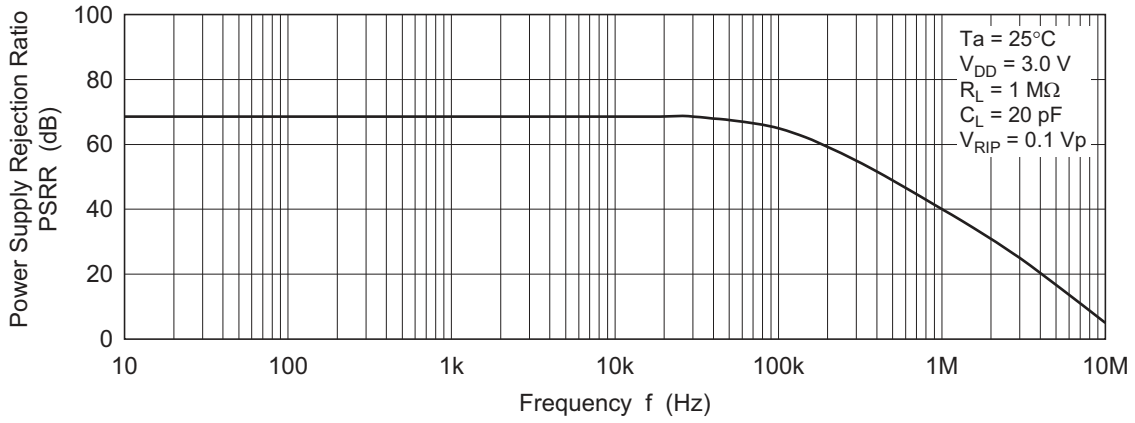


Figure 3-13. HA1630S06  
Common Mode Rejection Ratio vs. Frequency

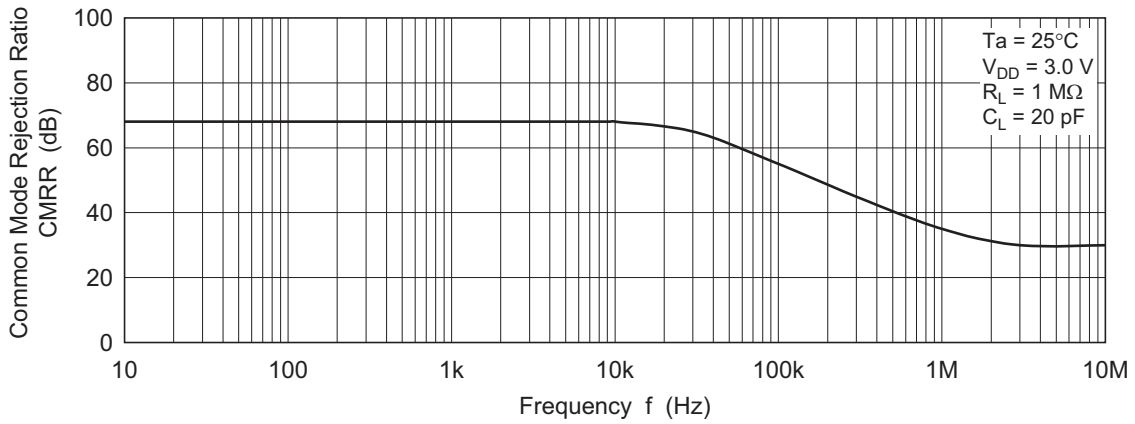
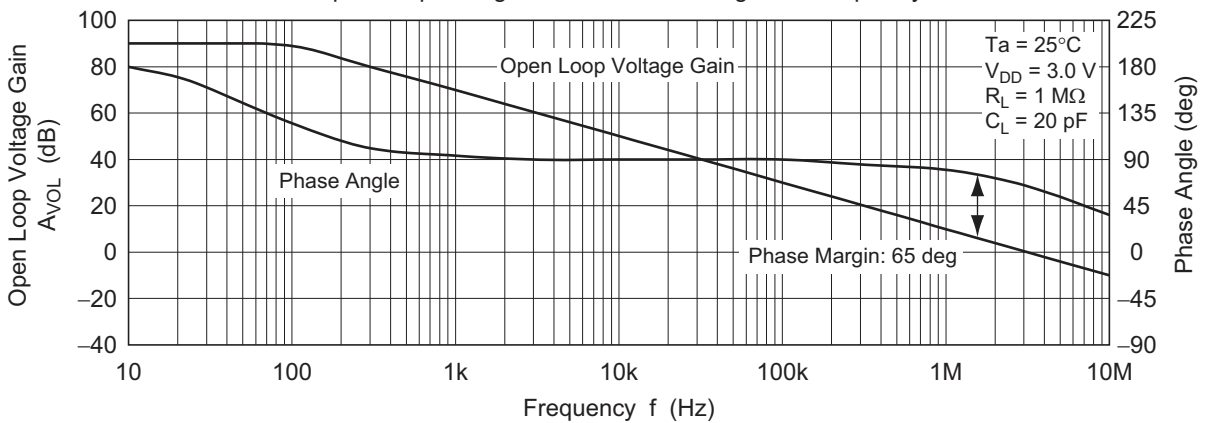


Figure 3-14. HA1630S06  
Open Loop Voltage Gain and Phase Angle vs. Frequency



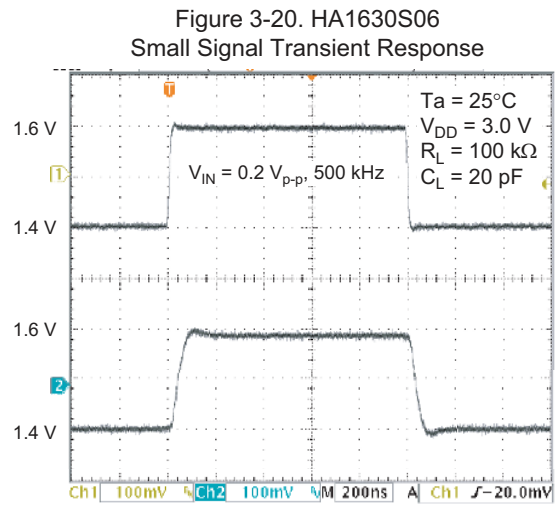
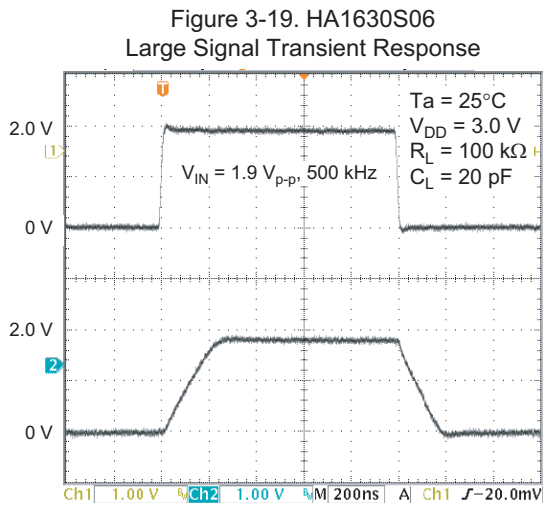
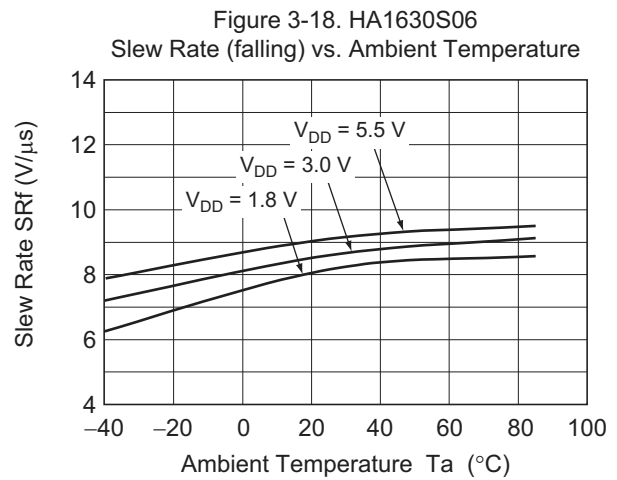
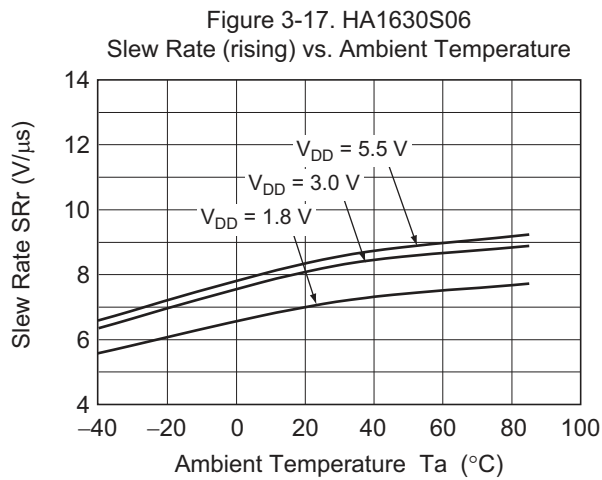
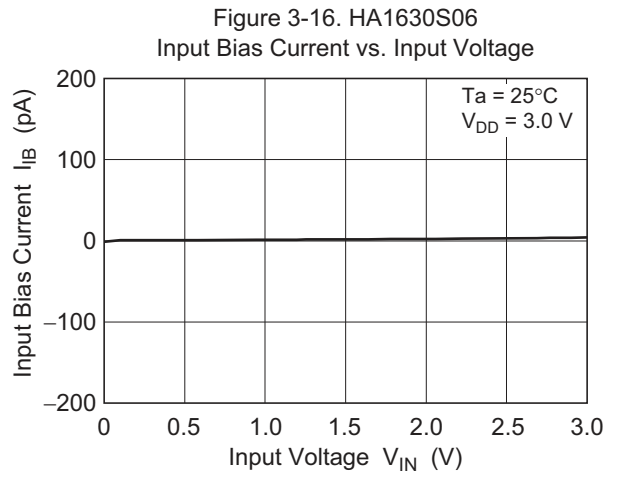
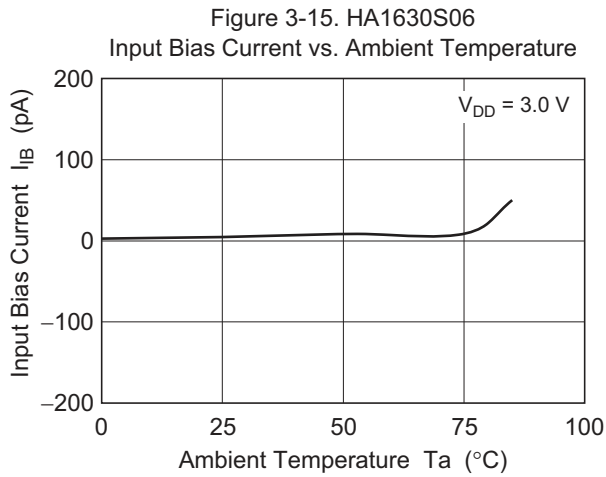


Figure 3-21. HA1630S06  
Total Harmonic Distortion + Noise vs.  
Output Voltage p-p

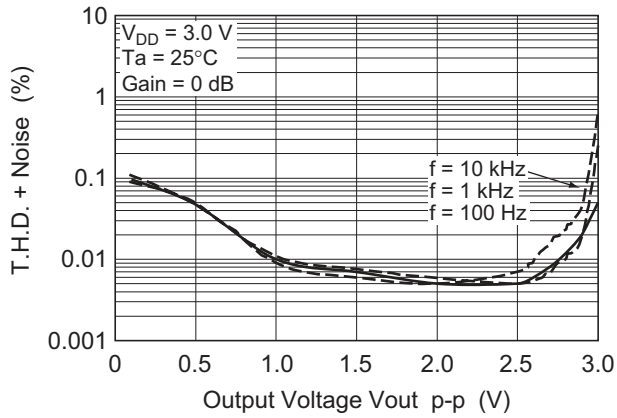


Figure 3-22. HA1630S06  
Total Harmonic Distortion + Noise vs.  
Output Voltage p-p

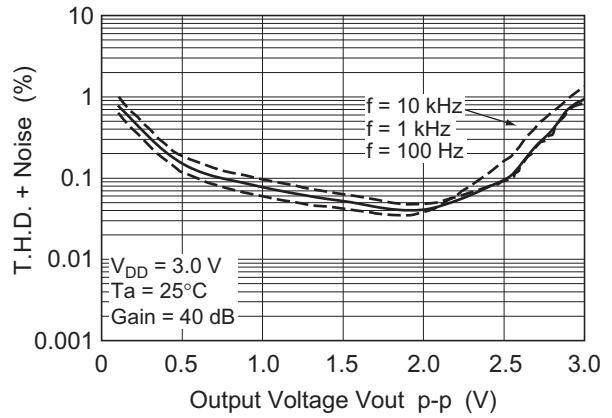


Figure 3-23. HA1630S06  
Voltage Output p-p vs. Frequency

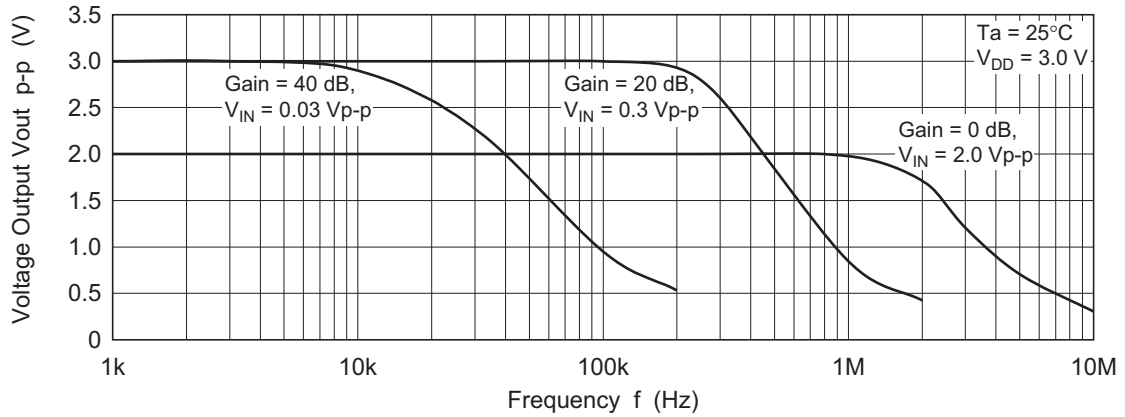
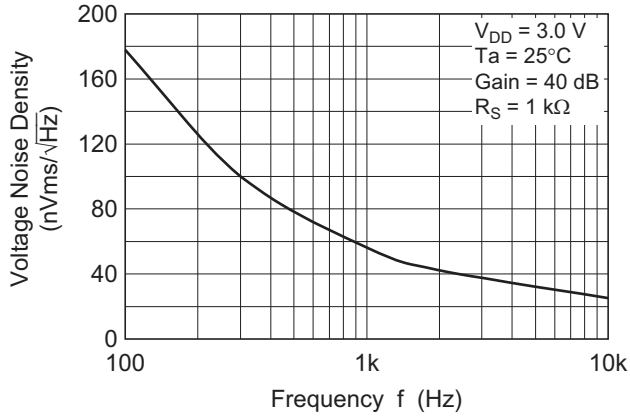
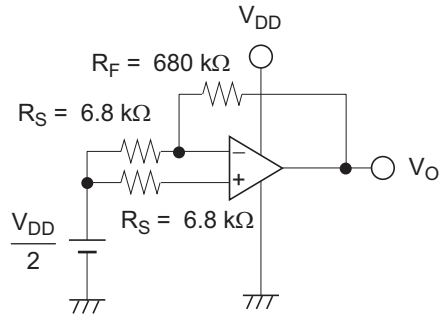


Figure 3-24. HA1630S06  
Voltage Noise Density vs. Frequency



**Test Circuits**

1. Power Supply Rejection Ratio, PSRR & Voltage Offset,  $V_{IO}$



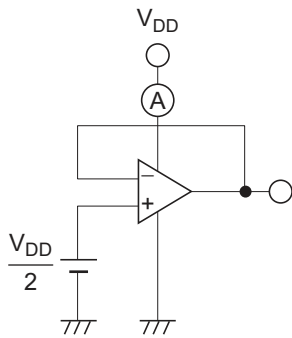
$$V_{IO} = \left( V_O - \frac{V_{DD}}{2} \right) \times \frac{R_S}{R_S + R_F}$$

PSRR

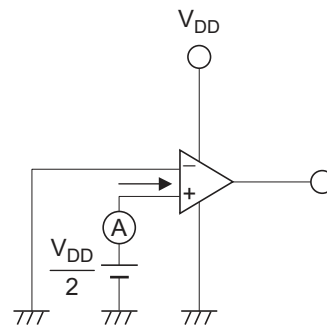
$$PSRR = -20 \log \left( \left| \frac{V_{DD1} - V_{DD2}}{V_{O1} - V_{O2}} \right| \times \frac{R_S}{R_S + R_F} \right)$$

Measure  $V_O$  corresponding to  $V_{DD1} = 2.95 \text{ V}$  and  $V_{DD2} = 3.05 \text{ V}$

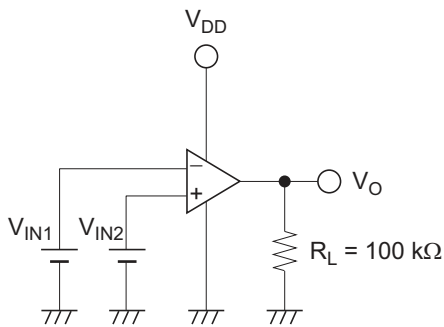
2. Supply Current,  $I_{DD}$



3. Input Bias Current,  $I_B$

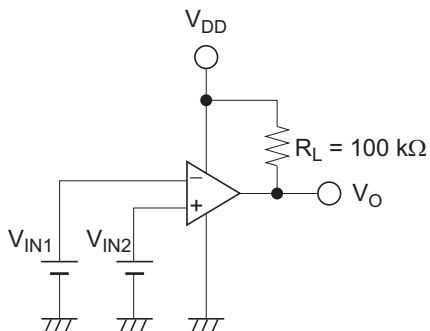


4. Output High Voltage,  $V_{OH}$



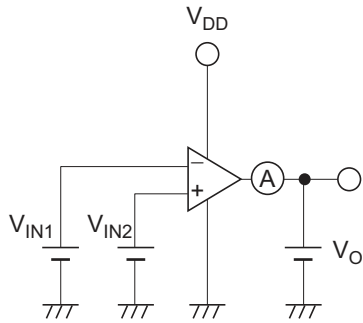
$$\begin{aligned} V_{OH} \\ V_{IN1} &= V_{DD} / 2 - 0.05 \text{ V} \\ V_{IN2} &= V_{DD} / 2 + 0.05 \text{ V} \end{aligned}$$

5. Output Low Voltage,  $V_{OL}$



$$\begin{aligned} V_{OL} \\ V_{IN1} &= V_{DD} / 2 + 0.05 \text{ V} \\ V_{IN2} &= V_{DD} / 2 - 0.05 \text{ V} \end{aligned}$$

6. Output Source Current,  $I_{OSOURCE}$  & Output Sink Current,  $I_{OSINK}$



$I_{OSOURCE}$

$$V_O = V_{DD} - 0.5 \text{ V}$$

$$V_{IN1} = V_{DD} / 2 - 0.05 \text{ V}$$

$$V_{IN2} = V_{DD} / 2 + 0.05 \text{ V}$$

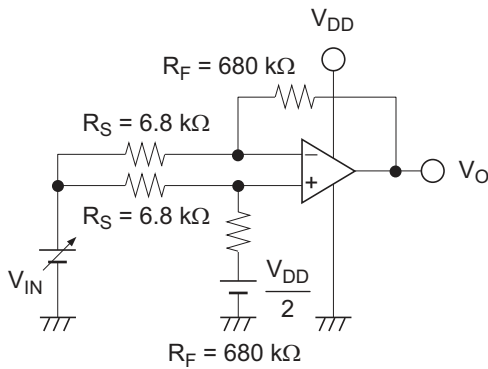
$I_{OSINK}$

$$V_O = + 0.5 \text{ V}$$

$$V_{IN1} = V_{DD} / 2 + 0.05 \text{ V}$$

$$V_{IN2} = V_{DD} / 2 - 0.05 \text{ V}$$

7. Common Mode Input Voltage,  $V_{CM}$  & Common Mode Rejection Ratio, CMRR

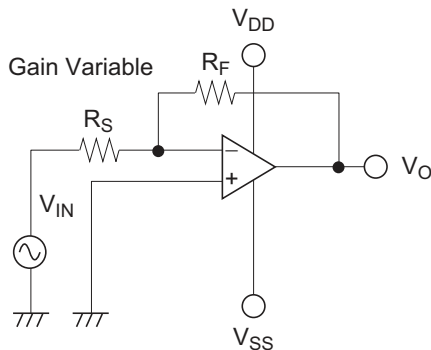


CMRR

$$CMRR = -20 \log \left( \left| \frac{V_{IN1} - V_{IN2}}{V_{O1} - V_{O2}} \right| \times \frac{R_S}{R_S + R_F} \right)$$

Measure  $V_O$  corresponding to  $V_{IN1} = 1.45 \text{ V}$  and  $V_{IN2} = 1.55 \text{ V}$

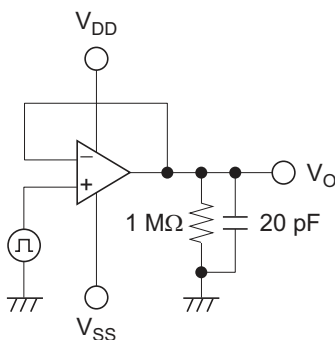
8. Total Harmonic Distortion, THD



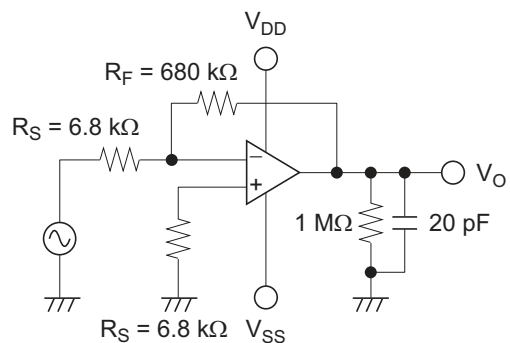
THD

Gain Variable  
 $R_F / R_S = 20 \log (100 \text{ k}\Omega / 1 \text{ k}\Omega) = 40 \text{ dB}$   
 $R_F / R_S = 20 \log (100 \text{ k}\Omega / 100 \text{ k}\Omega) = 0 \text{ dB}$   
 freq = 100 Hz, 1 kHz, 10 kHz  
 30 kHz LPF ON

9. Slew Rate, SR

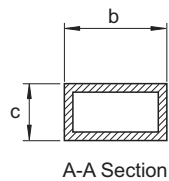
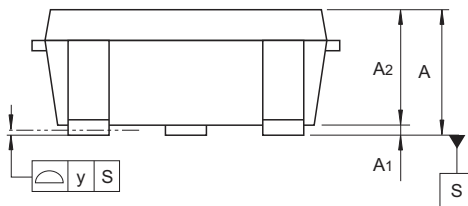
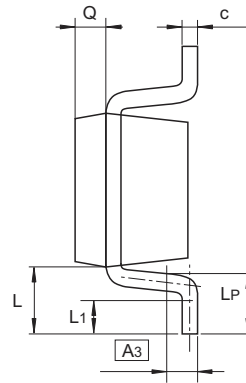
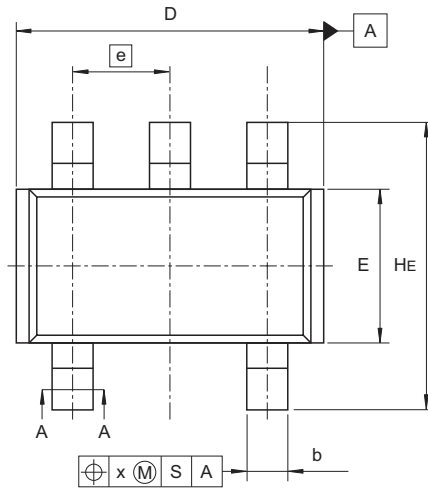


10. Gain,  $A_V$  & Phase, GBW



### Package Dimensions

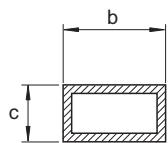
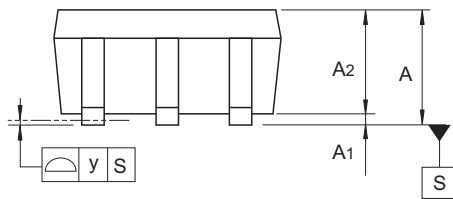
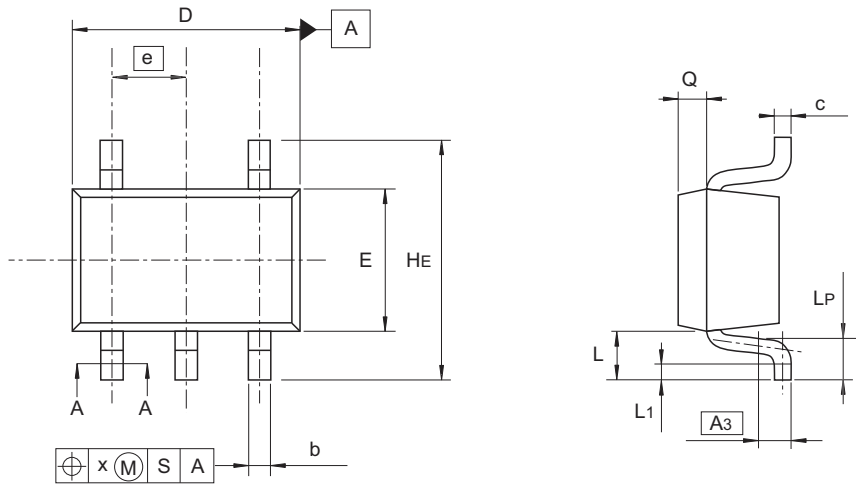
JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
SC-74A	PLSP0005ZB-A	MPAK-5 / MPAK-5V	0.015



Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
A	1.0	—	1.4
A <sub>1</sub>	0	—	0.1
A <sub>2</sub>	1.0	1.1	1.3
A <sub>3</sub>	—	0.25	—
b	0.35	0.4	0.5
c	0.11	0.16	0.26
D	2.8	2.95	3.1
E	1.5	1.6	1.8
e	—	0.95	—
H <sub>E</sub>	2.5	2.8	3.0
L	0.3	—	0.7
L <sub>1</sub>	0.1	—	0.5
L <sub>P</sub>	0.2	—	0.6
x	—	—	0.05
y	—	—	0.05
Q	—	0.3	—

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JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
SC-88A	PTSP0005ZC-A	CMPAK-5 / CMPAK-5V	0.006



A-A Section

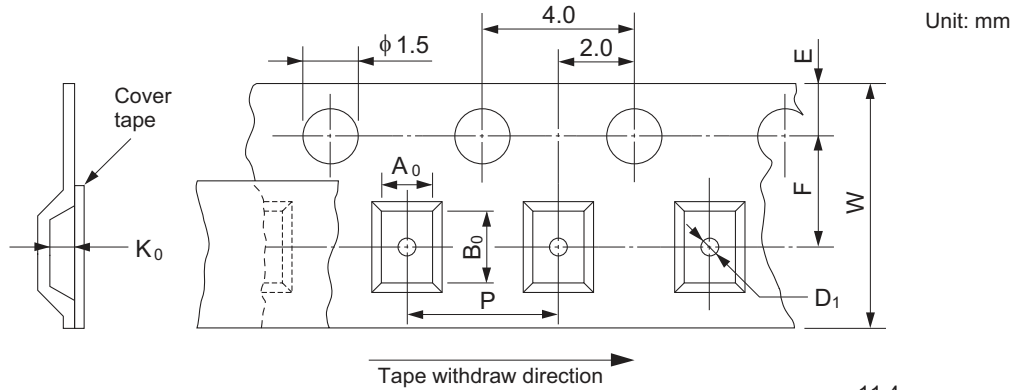
Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
A	0.8	—	1.1
A <sub>1</sub>	0	—	0.1
A <sub>2</sub>	0.8	0.9	1.0
A <sub>3</sub>	—	0.25	—
b	0.15	0.22	0.3
c	0.1	0.13	0.15
D	1.8	2.0	2.2
E	1.15	1.25	1.35
e	—	0.65	—
H <sub>E</sub>	1.8	2.1	2.4
L	0.3	—	0.7
L <sub>1</sub>	0.1	—	0.5
L <sub>P</sub>	0.2	—	0.6
x	—	—	0.05
y	—	—	0.05
Q	—	0.25	—

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### Taping & Reel Specification

[Taping]

Package Code	W	P	A <sub>0</sub>	B <sub>0</sub>	K <sub>0</sub>	E	F	D1	Maximum Storage No.
MPAK-5	8	4	3.3	3.3	1.5	1.75	3.5	1.05	3,000 pcs/reel
CMPAK-5	8	4	2.25	2.45	1.1	1.75	3.5	1.05	3,000 pcs/reel

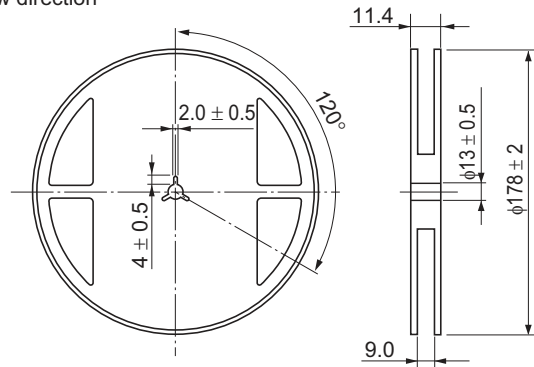


[Reel]

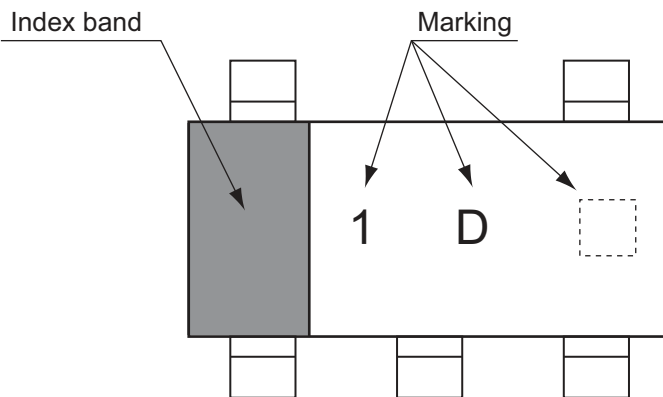
Package	Tape width	W1	W2
MPAK-5	8	11.4	9
CMPAK-5	8	11.4	9

[Ordering Information]

Ordering Unit
3,000 pcs



### Mark Indication



- 1 D □ : HA1630S04
- 1 E □ : HA1630S05
- 1 F □ : HA1630S06

□ = Control code  
(— or blank)



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