IQS7225A DATASHEET

6-Channel Device, Self Capacitance, Mutual Capacitance and Inductive sensing modes, Relative Rotational Encoder UI, I²C Communication Interface, Low Power Mode Options

1 Device Overview

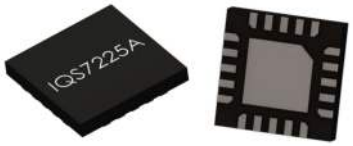
The IQS7225A ProxFusion® IC is a sensor fusion device that is mainly aimed at inductive sensing applications that require relative rotational inductive sensing and/or multiple inductive buttons. The device also has capacitive sensing capabilities that can be used to complement the inductive sensing applications, e.g. a capacitive wakeup channel. The sensor is fully I²C compatible and on-chip calculations enable the IC to respond effectively even in its lowest power modes.

1.1 Main Features

- Highly flexible ProxFusion® device
- 9 (QFN) external sensor pad connections
- Configure up to 6 Channels using the external connections
- External inductive sensor options:
  - Up to 6x self capacitive buttons
  - Up to 6x mutual capacitive buttons
  - Up to 6x inductive buttons
- Built-in basic functions:
  - Gray-coded relative rotational encoder
  - Selectable channel reference
    - LTA as reference
    - select channel to use as reference
    - fixed value as reference
  - Blocking channel
  - Automatic tuning
  - Noise filtering
  - Debounce & Hysteresis
  - Dual direction trigger indication
- Built-in Signal processing options:
  - Rotational encoder angle
  - Rotational encoder counter
  - Rotational encoder state
- Design simplicity
  - PC Software for debugging and obtaining optimal settings and performance
  - Auto-run from programmed settings for simplified integration
- Automated system power modes for optimal response vs consumption
- I²C communication interface with IRQ/RDY (up to fast plus -1MHz)
- I²C address selection using GPIO pin
- Event and streaming modes
- Customizable user interface due to programmable memory
- Supply voltage 2.2V to 3.5V
- Small packages
  - QFN20 (3 x 3 x 0.5 mm) - 0.4mm pitch

RoHS2
Compliant

QFN20 package
Representation only



1.2 Applications

- Waterproof inductive dial/counter applications
- Intergrated control panel (dial + buttons)
- Wearables
- Waterproof inductive buttons
- White goods user interface
- Smart home controllers

1.3 Block Diagram

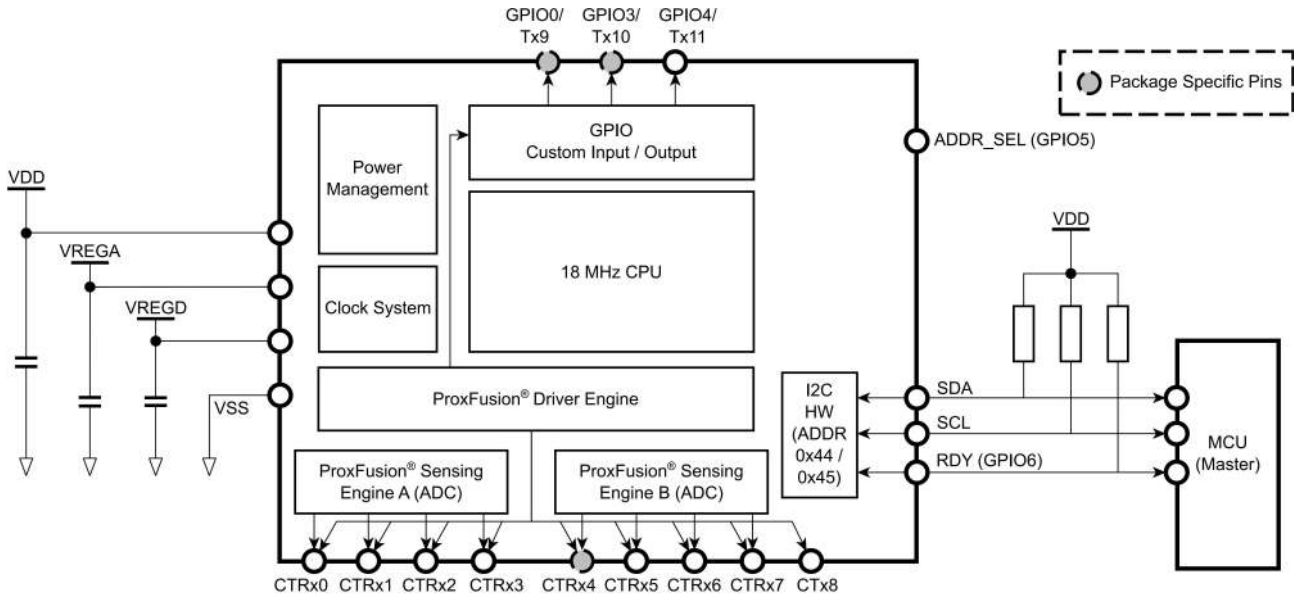


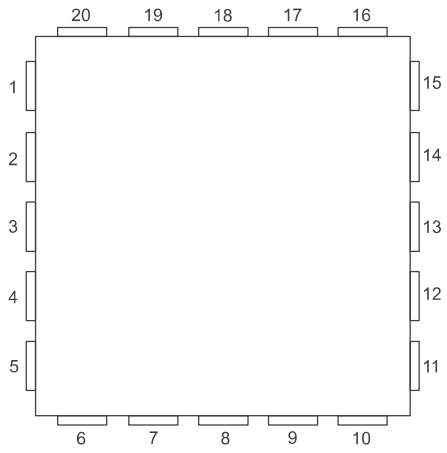
Figure 1.1: Functional Block Diagram

Contents

2 Hardware Connection

2.1 QFN20 Pin Diagram

Table 2.1: 20-pin QFN Package (Top View)



Pin no.	Signal name	Pin no.	Signal name
1	VDD	11	CRx6/CTx6
2	VREGD	12	CRx7/CTx7
3	VSS	13	CTx8/VBias
4	VREGA	14	CTx9/GPIO0
5	CRx0/CTx0	15	CTx10/GPIO3
6	CRx1/CTx1	16	CTx11/GPIO4
7	CRx2/CTx2	17	ADDR/GPIO5
8	CRx3/CTx3	18	SCL/GPIO2
9	CRx4/CTx4	19	SDA/GPIO1
10	CRx5/CTx5	20	RDY/GPIO6

Area name	Signal name
Tab	Thermal pad (floating)

2.2 Pin Attributes

Table 2.2: Pin Attributes

Pin no. QFN20	Signal name	Signal type	Buffer type	Power source
1	VDD	Power	Power	N/A
2	VREGD	Power	Power	N/A
3	VSS	Power	Power	N/A
4	VREGA	Power	Power	N/A
5	CRx0/CTx0	Analog		VREGA
6	CRx1/CTx1	Analog		VREGA
7	CRx2/CTx2	Analog		VREGA
8	CRx3/CTx3	Analog		VREGA
9	CRx4/CTx4	Analog		VREGA
10	CRx5/CTx5	Analog		VREGA
11	CRx6/CTx6	Analog		VREGA
12	CRx7/CTx7	Analog		VREGA
13	CTx8/VBias	Analog		VREGA
14	CTx9/GPIO0	Prox/Digital		VREGA/VDD
19	SDA/GPIO1	Digital		VDD
18	SCL/GPIO2	Digital		VDD
15	CTx10/GPIO3	Prox/Digital		VREGA/VDD
16	CTx11/GPIO4	Prox/Digital		VREGA/VDD
17	ADDR/GPIO5	Digital		VDD
20	RDY/GPIO6	Digital		VDD

2.3 Signal Descriptions

Table 2.3: Signal Descriptions

Function	Signal name	Pin no. QFN20	Pin type[i]	Description
ProxFusion®	CRx0/CTx0	5	IO	ProxFusion® channel
	CRx1/CTx1	6	IO	
	CRx2/CTx2	7	IO	
	CRx3/CTx3	8	IO	
	CRx4/CTx4	9	IO	
	CRx5/CTx5	10	IO	
	CRx6/CTx6	11	IO	
	CRx7/CTx7	12	IO	
	CTx8/VBias	13	IO	CTx8 pad
	CTx9/GPIO0	14	IO	CTx9 pad
	CTx10/GPIO3	15	IO	CTx10 pad
	CTx11/GPIO4	16	IO	CTx11 pad
	ADDR/GPIO5	17	IO	ADDR pad
GPIO	RDY/GPIO6	20	IO	RDY pad VPP input for OTP
I^2C	SDA/GPIO1	19	IO	I^2C Data
	SCL/GPIO2	18	IO	I^2C clock
Power	VDD	1	P	Power supply input voltage
	VREGD	2	P	Internal regulated supply output for digital domain
	VSS	3	P	Analog/Digital Ground
	VREGA	4	P	Internal regulated supply output for analog domain

[i]Pin Types: I = Input, O = Output, I/O = Input or Output, P = Power

2.4 Reference Schematic

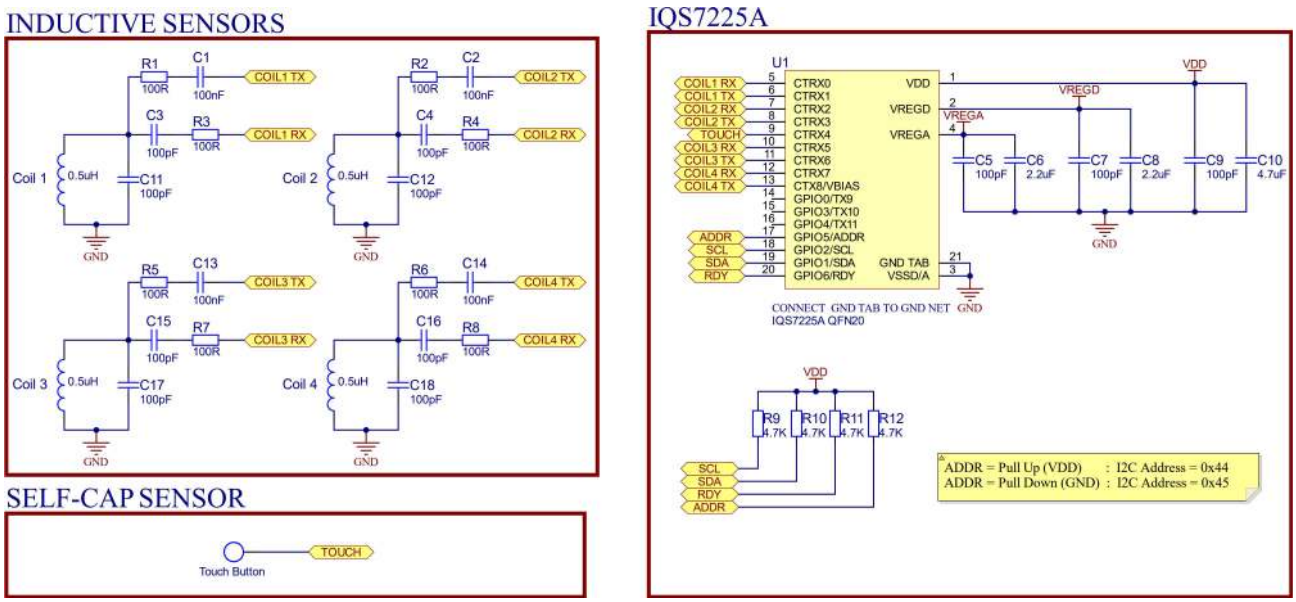


Figure 2.1: 4x Inductive Coils and 1x Self Capacitance Reference Schematic

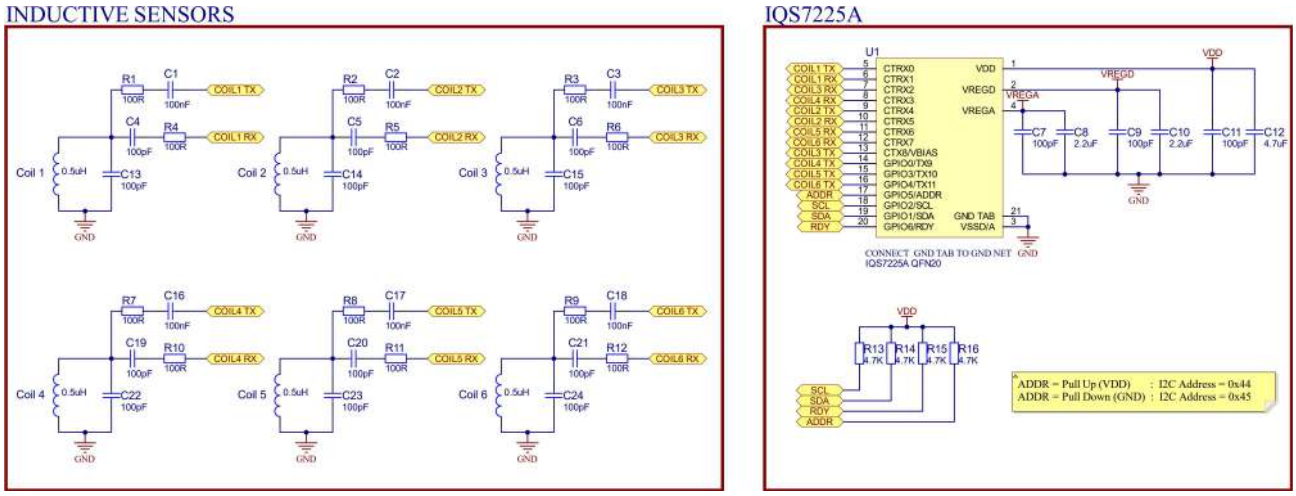


Figure 2.2: 6x Inductive Coils Reference Schematic

3 Inductive Rotational Encoder Design

A simple relative rotational sensor is implemented by spacing coils at a specified angle along the outer diameter of a rotating dial. The dial has a metal target pattern that encodes unique inductive states of the coils. The encoded states of the coils are used to determine the relative rotation of the dial.

3.1 Basic Encoder Principle

The basic geometry of the encoder has 2 coils separated by angle $\theta_{coil} = 90°$ and a metal target that spans $2 \cdot \theta_{coil} = 180°$ as shown in Figure 3.1. This coil-target configuration is capable of discerning 4 discrete Gray encoded positions at $90°$ intervals (see Table 3.1). When the metal target is fully covering the coil, the state of the coil is represented by '1' and when the metal target is completely clear of the coil the state of the coil is represented by '0'.

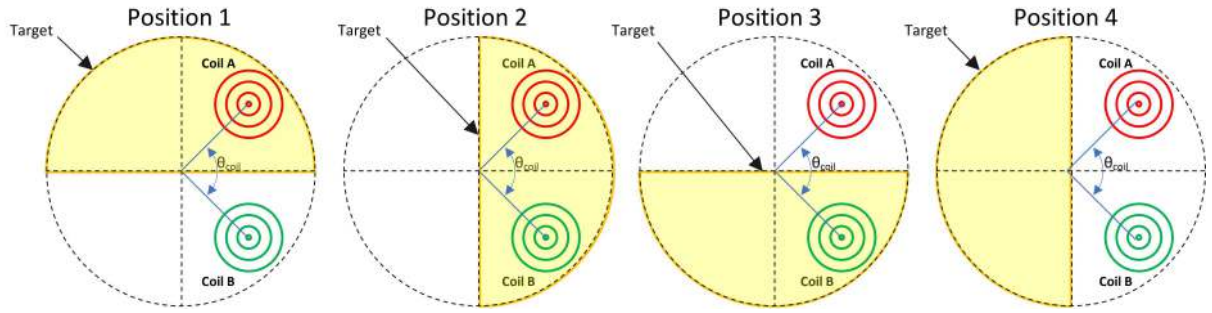


Figure 3.1: 4x position inductive rotational encoder

Table 3.1: Coil - Target Gray encoded states

Position	Angle	Gray Encoded State	
		Coil A	Coil B
1	0°	1	0
2	90°	1	1
3	180°	0	1
4	270°	0	0

3.2 Encoder Resolution

The configuration in Figure 3.1 has a resolution of $90°$. Higher resolution encoders can be defined with a smaller θ_{coil}. By changing the coil separation angle (θ_{coil}) and the target span geometry ($2 \cdot \theta_{coil}$), the resolution of the encoder can be defined.

Table 3.2: Encoder resolution geometry

Positions per Rev	Coil Seperation θ_{coil}	Target Span $2 \cdot \theta_{coil}$	Target Seperation $2 \cdot \theta_{coil}$	Number of Targets
4	90°	180°	180°	1
8	45°	90°	90°	2
12	30°	60°	60°	3
16	22.5°	45°	45°	4
20	18°	36°	36°	5
24	15°	30°	30°	6
28	12.86°	25.71°	25.71°	7
32	11.25°	22.50°	22.50°	8
N	360°/N	2 · 360°/N	2 · 360°/N	N/4

3.3 32 Position Encoder Geometry

The following geometry defines a 32-position encoder:

- Coil separation = 11.25°
- Target span = 22.50°
- Target separation = 22.50°
- Number of targets = 8

Each one of the target sections can discern 4 Gray encoded positions as shown in Figure 3.2. There are 8 target sections, thus for a full rotation of the dial there is a total of $4 \times 8 = 32$ positions.

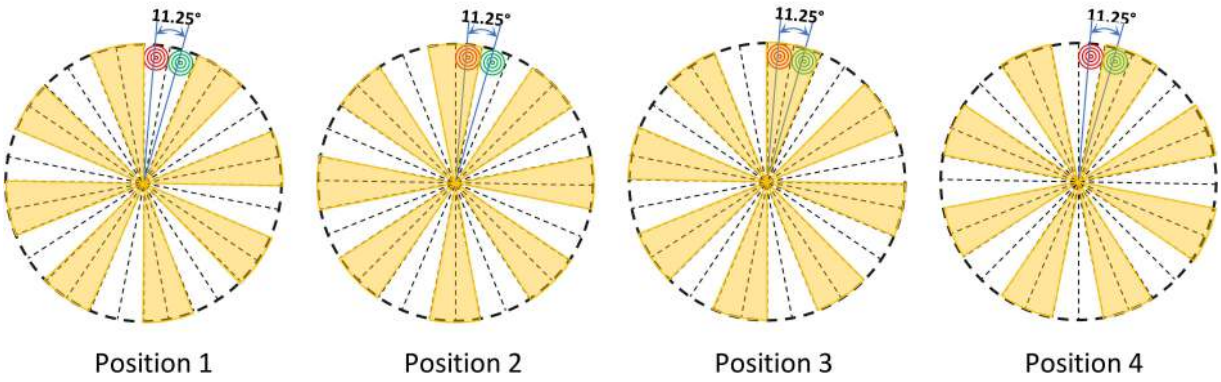


Figure 3.2: 32x position inductive rotational encoder

3.4 Equivalent Coil Position Geometry

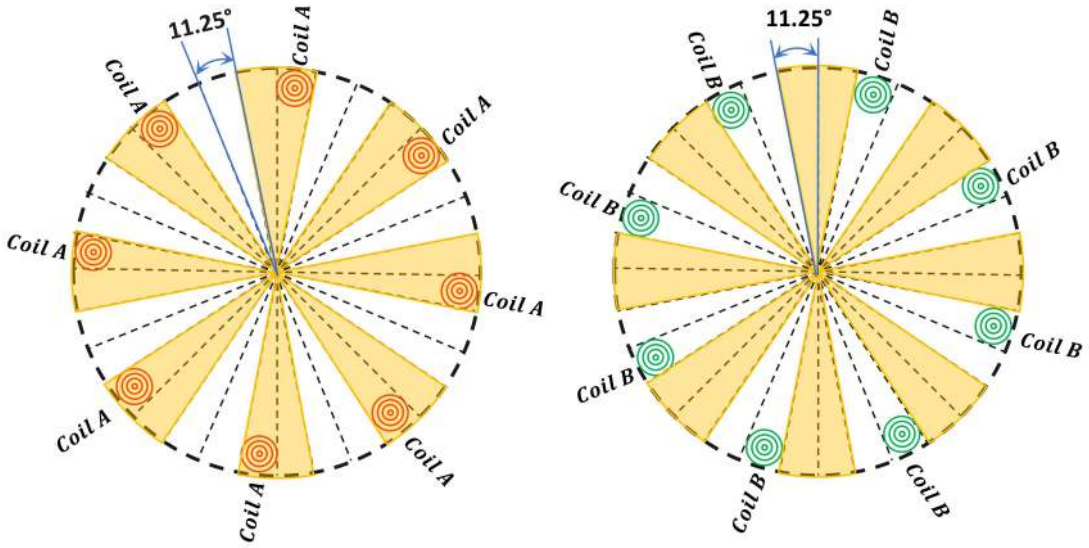


Figure 3.3: Coil A and Coil B equivalent positions

The geometrical positions of coil A and coil B have equivalent positions at every $4n \cdot \theta_{coil}$ interval. Placing the coil at any one of the equivalent positions will result in the correct encoding sequence.

3.5 Reference Coils

Coil $\overline{\mathrm{A}}$ and Coil $\overline{\mathrm{B}}$ can be used as a reference to Coil A and Coil B respectively. The use of reference coils can improve the noise immunity and temperature stability for specific applications. Table 3.3 shows the encoded states for the 32-position encoder with reference coils. The position of the reference coils is such that the state of the reference coils is always the opposite of the non-reference coils.

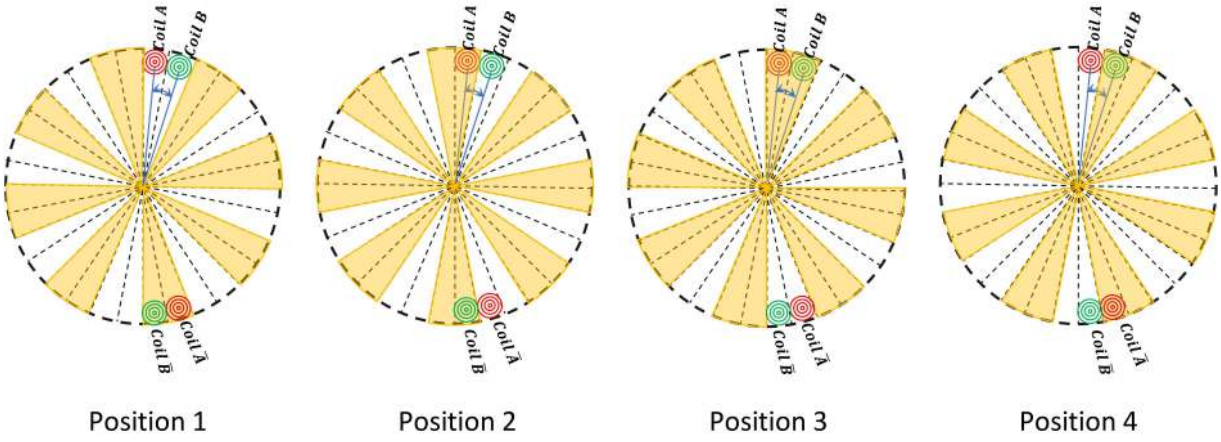


Figure 3.4: Encoder Reference Coils

Table 3.3: Gray Encoder with reference channel

Positions	Angle	Gray Encoded State			
		Coil A	Coil $\overline{A}$	Coil B	Coil $\overline{B}$
1	0°	0	1	0	1
2	90°	1	0	0	1
3	180°	1	0	1	0
4	270°	0	1	1	0

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Table 4.1: Absolute Maximum Ratings

	Min	Max	Unit
Voltage applied at VDD pin to VSS	2.2	3.5	V
Voltage applied to any ProxFusion® pin	–0.3	VREGA	V
Voltage applied to any other pin (referenced to VSS)	–0.3	VDD + 0.3 (3.5 V max)	V
Storage temperature, T_{stg}	–40	85	°C

4.2 Recommended Operating Conditions

Table 4.2: Recommended Operating Conditions

Recommended operating conditions		Min	Nom	Max	Unit
VDD	Supply voltage applied at VDD pin: F_{OSC} = 18 MHz	2.2		3.5	V
VREGA	Internal regulated supply output for analog domain: F_{OSC} = 18 MHz	1.7	1.75	1.79	V
VREGD	Internal regulated supply output for digital domain: F_{OSC} = 18 MHz	1.75	1.8	1.85	V
VSS	Supply voltage applied at VSS pin		0		V
T_A	Operating free-air temperature	–40	25	85	°C
C_{VDD}	Recommended capacitor at VDD	2×C_{VREGA}	3×C_{VREGA}		µF
C_{VREGA}	Recommended external buffer capacitor at VREGA, ESR≤ 200 mΩ	2	4.7	10	µF
C_{VREGD}	Recommended external buffer capacitor at VREGD, ESR≤ 200 mΩ	2	4.7	10	µF
$Cx_{SELF–VSS}$	Maximum capacitance between ground and all external electrodes on all ProxFusion® blocks (self-capacitance mode)	1	-	400[i]	pF
$Cm_{CTx–CRx}$	Capacitance between Receiving and Transmitting electrodes on all ProxFusion® blocks (mutual-cap mode)	0.2	-	9[i]	pF
$Cp_{CRx–VSS–1M}$	Maximum capacitance between ground and all external electrodes on all ProxFusion® blocks (mutual-capacitance mode @f_{xfer} = 1 MHz)			100[i]	pF
$Cp_{CRx–VSS–4M}$	Maximum capacitance between ground and all external electrodes on all ProxFusion® blocks (mutual-capacitance mode @ f_{xfer} = 4 MHz sensing)			25[i]	pF
$\frac{Cp_{CRx–VSS}}{Cm_{CTx–CRx}}$	Capacitance ratio for optimal SNR in mutual capacitance mode[ii]	10		20	n/a
$RCx_{CRx/CTx}$	Series (in-line) resistance of all mutual capacitance pins (Tx & Rx pins) in mutual capacitance mode	0[iii]	0.47	10[iv]	kΩ
RCx_{SELF}	Series (in-line) resistance of all self capacitance pins in self capacitance mode	0[iii]	0.47	10[iv]	kΩ

4.3 ESD Rating

Table 4.3: ESD Rating

		Value	Unit
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[v]	±4000	V

[i] RCx = 0 Ω

[ii] Please note that the the maximum values for Cp and Cm are subject to this ratio

[iii] Nominal series resistance of 470 Ω is recommended to prevent received and emitted EMI effects. Typical resistance also adds additional ESD protection

[iv] Series resistance limit is a function of f_{xfer} and the circuit time constant, RC. $R_{max} \times C_{max} = \frac{1}{(6 \times f_{xfer})}$ where C is the pin capacitance to VSS.

[v] JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±4000 V may actually have higher performance.

4.4 Current Consumption

Sensing Mode: : Inductive
Number of Inductive Channels : 4
Number of Cycles : 2
ATI Target : 256
ATI Base : 256
Tx Frequency : 4.50 MHz
Conversion Frequency : 4.50 MHz
Tx Impedance : 20kΩ
Interface Selection : Event Mode

Table 4.4: Power Mode Current Consumption

Power mode	Report rate (Sampling rate) [ms]	Typical Current [µA]
Normal Power / Low Power	10	291
	16	150
	25	97
	50	49
	100	24
	150	11
Ultra Low Power	150	5
	500	2

5 Timing and Switching Characteristics

5.1 Reset Levels

Table 5.1: Reset Levels

Parameter		Min	Typ	Max	Unit
V_{VDD}	Power-up/down level (Reset trigger) – slope > 100 V/s	1.040	1.353	1.568	V
V_{VREGD}	Power-up/down level (Reset trigger) – slope > 100 V/s	0.945	1.122	1.304	V

5.2 Miscellaneous Timings

Table 5.2: Miscellaneous Timings

Parameter		Min	Typ	Max	Unit
f_{xfer}	Charge transfer frequency (derived from f_{OSC})	42	500 – 1500	4500	kHz
f_{OSC}	Master CLK frequency tolerance 18 MHz	17.1	18	19.54	MHz

5.3 Digital I/O Characteristics

Table 5.3: Digital I/O Characteristics

Parameter		Test Conditions	Min	Typ	Max	Unit
V_{OL}	GPIO1 & GPIO2 Output low voltage	I_{sink} = 20 mA			0.3	V
V_{OL}	GPIO0, 3, 4, 5 Output low voltage	I_{sink} = 10 mA			0.15	V
V_{OH}	Output high voltage	I_{source} = 20 mA	VDD – 0.2			V
V_{IL}	Input low voltage		VDD × 0.3			V
V_{IH}	Input high voltage				VDD × 0.7	V
C_{b_max}	GPIO1 & GPIO2 maximum bus capacitance				550	pF

5.4 I²C Characteristics

Table 5.4: I²C Characteristics

Parameter		VDD	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency	1.8 V, 3.3 V			1000	kHz
$t_{HD,STA}$	Hold time (repeated) START	1.8 V, 3.3 V	0.26			µs
$t_{SU,STA}$	Setup time for a repeated START	1.8 V, 3.3 V	0.26			µs
$t_{HD,DAT}$	Data hold time	1.8 V, 3.3 V	0			ns
$t_{SU,DAT}$	Data setup time	1.8 V, 3.3 V	50			ns
$t_{SU,STO}$	Setup time for STOP	1.8 V, 3.3 V	0.26			µs
t_{SP}	Pulse duration of spikes suppressed by input filter	1.8 V, 3.3 V	0		50	ns

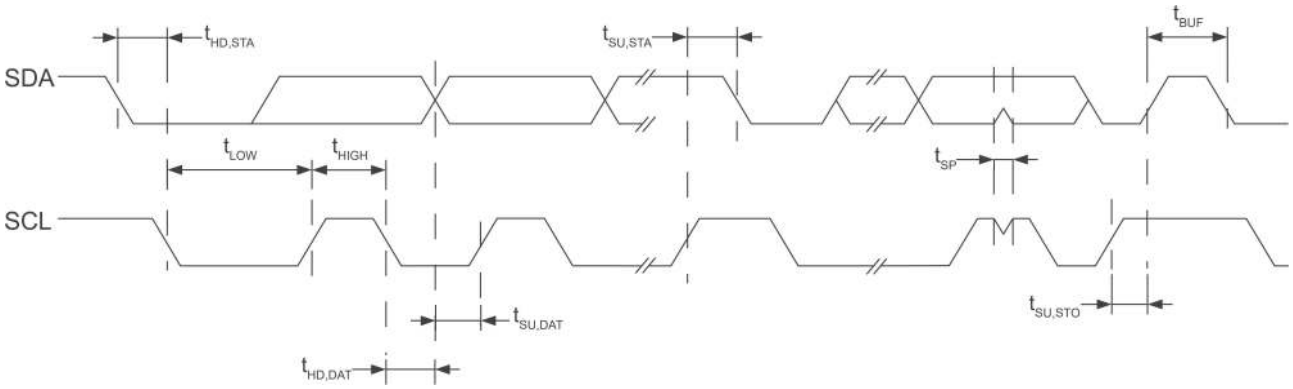


Figure 5.1: I^2C Mode Timing Diagram

6 ProxFusion® Module

The IQS7225A contains dual ProxFusion® modules that use patented technology to measure and process the sensor data. Two modules ensure a rapid response from multi-channel implementations. The multiple touch and proximity tier level outputs are the primary output from the sensor.

6.1 Channel Options

Self-capacitance, mutual capacitance, reference tracking and inductive designs are possible with the IQS7225A.

- Sensor pad design overview: AZD008
- Mutual capacitance (also known as projected capacitance) button layout guide: AZD036
- Inductive design layout guide: AZD115

6.2 Low Power Options

The IQS7225A offers 4 power modes:

- Normal power mode (NP)
  - Flexible channel scan rate
- Lower power mode (LP)
  - Flexible channel scan rate
  - Typically set to a slower rate than NP
- Ultra-low power mode (ULP)
  - Optimized firmware setup
  - Intended for rapid wake-up on a single channel (e.g. distributed proximity event), enabling immediate button response for an approaching user
  - Other sensor channels are typically sampled at a slower rate in order to optimize power consumption
- Halt power mode
  - Intended for use during shipping and storage of battery operated-assemblies
  - No conversions carried out on any of the channels

6.3 Count Value

The sensing measurement returns a *count value* for each channel. Count values are inversely proportional to capacitance/inductance, and all outputs are derived from this.

6.4 Reference Value/Long-Term Average (LTA)

User interaction is detected by comparing the measured count values to some reference value. The reference value/LTA of a sensor is slowly updated to track changes in the environment and is not updated during user interaction.

6.4.1 Reseed

Since the *Reference* for a channel is critical for the device to operate correctly, there could be known events or situations which would call for a manual reseed. A reseed takes the latest measured counts, and seeds the *reference/LTA* with this value, therefore updating the value to the latest environment. A reseed command can be given by setting the corresponding bit (Register 0xD0, bit3).

6.5 Automatic Tuning Implementation (ATI)

The ATI is a sophisticated technology implemented in the new ProxFusion® devices to allow optimal performance of the devices for a wide range of sensing electrode capacitances and inductances, without modification to external components. The ATI settings allow tuning of various parameters. For a detailed description of ATI, please contact Azoteq.

6.6 Automatic Re-ATI

6.6.1 Description

Re-ATI will be triggered if certain conditions are met. One of the most important features of the Re-ATI is that it allows easy and fast recovery from an incorrect ATI, such as when performing ATI during user interaction with the sensor. This could cause the wrong ATI Compensation to be configured, since the user affects the capacitance of the sensor. A Re-ATI would correct this. It is recommended to always have this enabled. When a Re-ATI is performed on the IQS7225A, a status bit will set momentarily to indicate that this has occurred.

6.6.2 Conditions for Re-ATI to activate

A Re-ATI is performed when the reference of a channel drifts outside of the acceptable range from the ATI Target. The boundaries where Re-ATI occurs for the channels are adjustable in registers listed in Table A.22.

$$\textbf{Re-ATI Boundary}_{\textbf{default}} = \textbf{ATI target} \pm (\tfrac{1}{8}\textbf{ATI Target})$$

For example, assume that the ATI target is configured to 800 and the default boundary value is $\frac{1}{8} \times 800 = 100$. If Re-ATI is enabled, the ATI algorithm will be repeated under the following conditions:

$$\textbf{Reference} > \textbf{900 or Reference} < \textbf{700}$$

The ATI algorithm executes in a short time, so it goes unnoticed by the user.

6.6.3 ATI Error

After the ATI algorithm is performed, a check is done to see if there was any error with the algorithm. An ATI error is reported if one of the following conditions is true for any channel after the ATI has completed:

- ATI Compensation = 0 (min value)
- ATI Compensation $\geq$ 1023 (max value)
- Count is already outside the Re-ATI range upon completion of the ATI algorithm

If any of these conditions are met, the corresponding error flag will be set (*ATI Error*). The flag status is only updated again when a new ATI algorithm is performed.

Re-ATI will not be repeated immediately if an ATI Error occurs. A configurable time (*ATI error timeout*) will pass where the Re-ATI is momentarily suppressed. This is to prevent the Re-ATI repeating indefinitely. An ATI error should however not occur under normal circumstances.

6.7 Mode Timeout

In order to optimize power consumption and performance, power modes are “stepped” by default in order to move to power efficient modes when no interaction has been detected for a certain (configurable) time, known as the “mode timeout”.

6.8 Count Filter

6.8.1 IIR Filter

The IIR filter applied to the digitized raw input offers various damping options as defined in Table A.20 and Table A.21

Damping factor = Beta/256

7 Hardware Settings

Settings specific to hardware and the ProxFusion® Module charge transfer characteristics can be changed.

Some are described below. The other hardware parameters are not discussed as they should only be adjusted under the guidance of Azoteq support engineers.

7.1 Charge Transfer Frequency

The charge transfer frequency (f_{xfer}) can be configured using the product GUI, and the relative parameters (*Charge Transfer frequency*) will be provided. For high resistance sensors, it might be needed to decrease f_{xfer}.

7.2 Reset

7.2.1 Reset Indication

After a reset, the *Device Reset* bit will be set by the system to indicate the reset event occurred. This bit will clear when the master sets the *Ack Reset*. If it becomes set again, the master will know a reset has occurred, and can react appropriately.

7.2.2 Software Reset

The IQS7225A can be reset by means of an I^2C command (*Soft Reset*).

8 Additional Features

8.1 Setup Defaults

The supplied GUI can be utilised to configure the optimal settings. The design specific settings are exported and can be written to the device by the master after every power-on reset.

8.2 RF Immunity

The IQS7225A has immunity to high power RF noise. To improve the RF immunity, extra decoupling capacitors are suggested on V_{REG} and V_{DD}.

Place a 100pF in parallel with the 2.2 µF ceramic on V_{REG}. Place a 4.7 µF ceramic on V_{DD}. All decoupling capacitors should be placed as close as possible to the V_{DD} and V_{REG} pads.

If needed, series resistors can be added to Rx electrodes to reduce RF coupling into the sensing pads. Normally these are in the range of 470 Ω – 1 kΩ. PCB ground planes also improve noise immunity.

9 I²C Interface

9.1 I²C Module Specification

The device supports a standard two wire I²C interface with the addition of a RDY (ready interrupt) line. The communications interface of the IQS7225A supports the following:

- *Fast-mode-plus* standard I²C up to 1MHz.
- Streaming data as well as event mode.
- The provided interrupt line (RDY) is an open-drain active low implementation and indicates a communication window.

The IQS7225A implements 16-bit addressing with 2 data bytes at each address. Two consecutive 8-bit read or write operations are required in this memory map structure. The two bytes at each address will be referred to as "byte 0" (least significant byte) and "byte 1" (most significant byte).

9.2 I²C Address

When GPIO5/ADDR is pulled up to VDD the 7-bit I²C device address is 0x44 ('1000100') and the full address byte will thus be 0x89 (read) or 0x88 (write). When GPIO5/ADDR is pulled low to GND the 7-bit I²C device address is 0x45 ('1000101') and the full address byte will thus be 0x8B (read) or 0x8A (write).

Other address options exist on special request. Please contact Azoteq.

9.3 I³C Compatibility

This device is not compatible with an I³C bus due to clock stretching allowed for data retrieval.

9.4 Memory Map Addressing

9.4.1 16-bit Address

Device settings are addressed with 16-bit memory addresses. When reading device settings, it is possible to address each memory block as an 8-bit address and then continue to clock into the next address locations. For example, the procedure depicted below is followed to read the values from the hypothetical address 0xE000 to 0xE003:

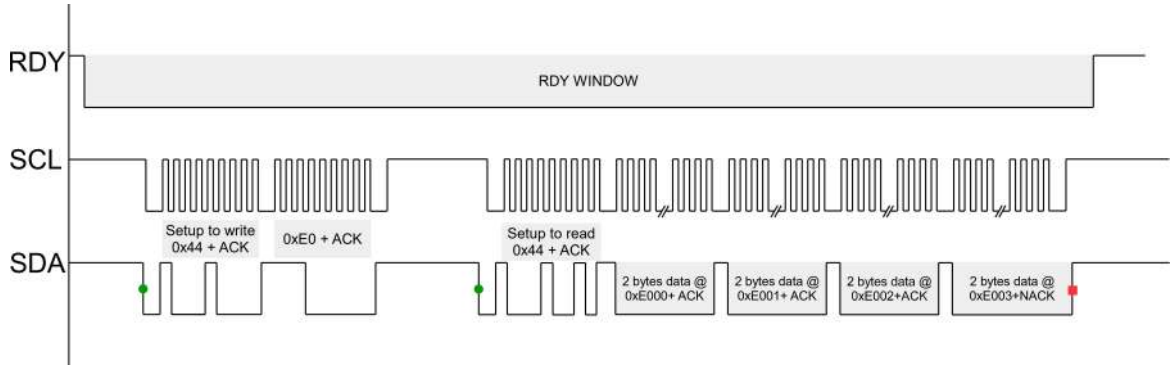


Figure 9.1: 8-bit Addressing for Continuous Block

However, if you need to address a specific memory address or write to a memory address, then you will need to address using the full 16-bit address (note the 16-bit address is high byte first, unlike the data which is low byte first):

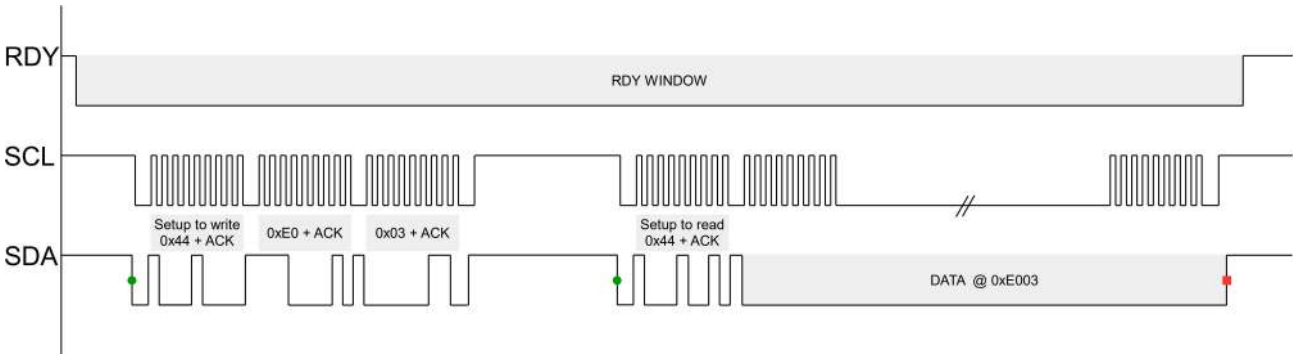


Figure 9.2: Extended 16-bit Addressing for a Specific Register

9.5 Data

The memory map implements a 16-bit addressing scheme with 16-bit words, meaning that each address contains 2 bytes of data. For example, address 0x8000 will provide two bytes, then the next two bytes read/written will be for address 0x8001.

The 16-bit data is sent in little endian byte order (least significant byte first).

9.6 I²C Timeout

If the communication window is not serviced within the *I²C timeout* period (in milliseconds), the session is ended (RDY goes HIGH), and processing continues as normal. This allows the system to continue and keep reference values up to date even if the master is not responsive. However the corresponding data was missed/lost, and this should be avoided. The default I²C timeout period is set to 10ms and can be adjusted in register 0x8002.

9.7 Terminate Communication

A standard I²C STOP ends the current communication window.

If the stop bit disable (bit 0 register 0x8003) is set, the device will not respond to a standard I²C STOP. The communication window must be terminated using the end communications command (0xFF).

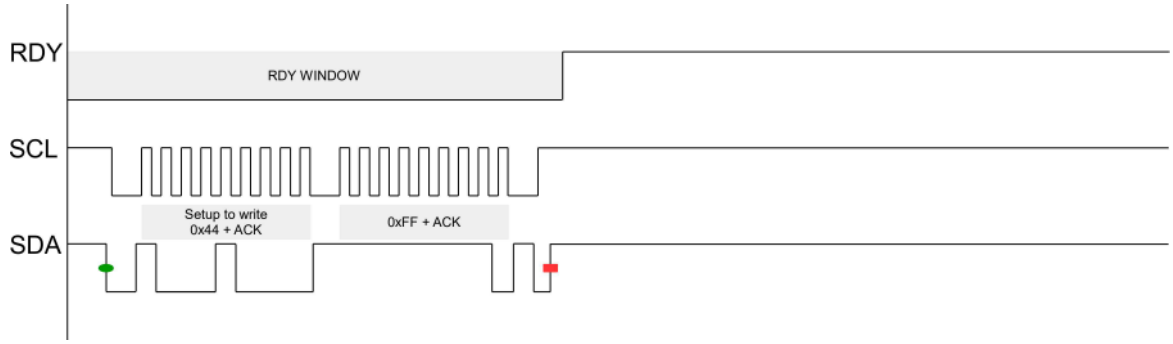


Figure 9.3: Force Stop Communication Sequence

9.7.1 Force Communication

In streaming mode, the IQS7225A I²C will provide RDY windows at intervals specified in the power mode report rate. Ideally, communication with the IQS7225A should only be initiated in a Ready window but a communcation request described in Figure 9.4 below, will force a Ready window to open. In event mode Ready windows are only provided when an event is reported and a Ready window must be requested to write or read settings outside of this window. The minimum and maximum time between the communication request and the opening of a RDY window (t_{wait}), is application specific, but the average values are 0.1ms $\leq t_{wait} \leq$ 45ms [i].

The communcation request sequence is shown in figure 9.4 below.

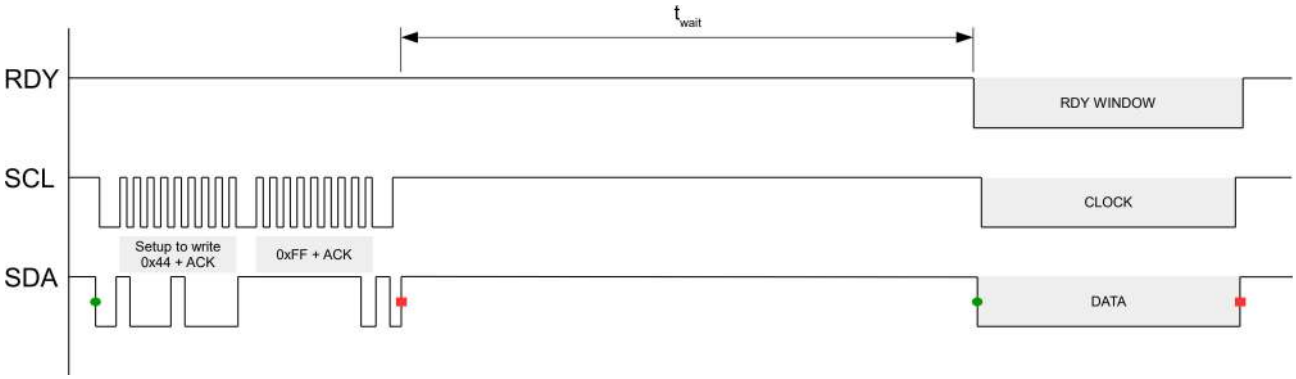


Figure 9.4: Force Communication Sequence

9.8 RDY/IRQ

The communication has an open-drain active-low RDY signal to inform the master that updated data is available. It is optimal for the master to use this as an interrupt input and obtain the data accordingly. It is also useful to allow the master MCU to enter low-power/sleep and allowing wake-up from low-power/sleep when user presence is detected. It is recommended that the RDY be placed on an interrupt-on-pin-change input on the master.

9.9 Invalid Communications Return

The device will give an invalid communication response (0xEE) under the following conditions:

- The host is trying to read from a memory map register that does not exist.
- The host is trying to read from the device outside of a communication window (i.e. while RDY = high)

9.10 I²C Interface

The IQS7225A has 3 *I²C interface options*, as described in the sections below.

9.10.1 I²C Streaming

I²C Streaming mode refers to constant data reporting at the relevant power mode report rate specified in register *0x8103* (normal power), register *0x8105* (low power) and register *0x8107* (ultra low power) respectively.

[i] Please contact Azoteq for an application specific value of t_{wait}

9.10.2 I²C Event Mode

The device can be set up to bypass the communication window when no activity is sensed (EVENT MODE). This is usually enabled since the master does not want to be interrupted unnecessarily during every cycle if no activity occurred. The communication will resume (RDY will indicate available data) if an enabled event occurs.

9.10.3 I²C Stream in Touch Mode

Stream in touch is a hybrid I²C mode between streaming mode and event mode. The device follows event mode I²C protocol but when a touch is registered on any channel, the device enters streaming mode until the touch is released.

The hybrid I²C interface is specifically aimed at the use of sliders where data needs to be received and processed for the duration of a touch.

9.11 Event Mode Communication

Event mode can only be entered if the following requirements are met:

- *Reset* bit must be cleared by acknowledging the device reset condition occurrence through writing *Ack Reset* bit to clear the System status flag.
- Events must be serviced by reading from the *Events* register 0x1001 to ensure all events flags are cleared, otherwise continuous reporting (RDY interrupts) will persist after every conversion cycle similar to streaming mode.

9.11.1 Events

Numerous events can be individually enabled to trigger communication, bit definitions can be found in Table A.4, A.5 and Table A.6:

- Power mode change events
- ATI events
- Tier0 events
- Tier1 events
- Tier2 events

10 I²C Memory Map - Register Descriptions

See Appendix A for a more detailed description of registers and bit definitions

Address Read Only	Data (16bit)	Notes
0x0000	Application Version Info	See Table A.1
0x0001		
0x0002		
0x0003		
0x0004		
0x0100	ROM Version Info	See Table A.2
0x0101		
0x0102		
0x0103		
0x0104		
Read Only	**Device Status**	
0x1000	System Status	See Table A.3
0x1001	Events	See Table A.4
0x1002	Tier0-1 Status	See Table A.5
0x1003	Tier2 Status	See Table A.6
0x1004	Rotation Encoder Gray States	See Table A.7
0x1005	Rotation Encoder Angle	Value $\in [0, 16383]$
0x1006	Rotation Encoder Counter	Value $\in [-32767, 32767]$
Read Only	**Channel Counts**	
0x1100	Channel 0 Counts	Value $\in [0, 16383]$
0x1101	Channel 1 Counts	
0x1102	Channel 2 Counts	
0x1103	Channel 3 Counts	
0x1104	Channel 4 Counts	
0x1105	Channel 5 Counts	
Read Only	**Channel LTA**	
0x1200	Channel 0 LTA	Value $\in [0, 16383]$
0x1201	Channel 1 LTA	
0x1202	Channel 2 LTA	
0x1203	Channel 3 LTA	
0x1204	Channel 4 LTA	
0x1205	Channel 5 LTA	
Read Only	**Channel Delta**	
0x1300	Channel 0 Delta	Value $\in [-16383, 16383]$
0x1301	Channel 1 Delta	
0x1302	Channel 2 Delta	
0x1303	Channel 3 Delta	
0x1304	Channel 4 Delta	
0x1305	Channel 5 Delta	
Read Only	**Unfiltered Channel Counts**	
0x1400	Channel 0 Unfiltered Counts	Value $\in [16383, 16383]$
0x1401	Channel 1 Unfiltered Counts	
0x1402	Channel 2 Unfiltered Counts	
0x1403	Channel 3 Unfiltered Counts	
0x1404	Channel 4 Unfiltered Counts	
0x1405	Channel 5 Unfiltered Counts	
Read-Write	**PMU and System Settings**	

0x8000	System Control Settings	See Table A.8
0x8001	Event Mask	See Table A.9
0x8002	I^2C Window Timeout	16-bit value (ms)
0x8003	I^2C Configuration	See Table A.10
Read-Write	**Report Rates and Timeouts**	
0x8100	ATI Error Timeout	16-bit value * 0.5s
0x8101	ATI Report Rate	16-bit value (ms)
0x8102	Normal Power Mode Timeout	16-bit value (ms)
0x8103	Normal Power Mode Report Rate	16-bit value (ms)
0x8104	Low Power Mode Timeout	16-bit value (ms)
0x8105	Low Power Mode Report Rate	16-bit value (ms)
0x8106	Ultra Low Power Mode Timeout	16-bit value (ms)
0x8107	Ultra Low Power Mode Report Rate	16-bit value (ms)
Read-Write	**Cycle Setup**	
0x9000	Cycle Setup 0	See Table A.11
0x9001		See Table A.12
0x9002		See Table A.13
0x9100	Cycle Setup 1	See Table A.11
0x9101		See Table A.12
0x9102		See Table A.13
0x9200	Cycle Setup 2	See Table A.11
0x9201		See Table A.12
0x9202		See Table A.13
0x9300	Cycle Setup 3	See Table A.11
0x9301		See Table A.12
0x9302		See Table A.13
0x9400	Cycle Setup 4	See Table A.11
0x9401		See Table A.12
0x9402		See Table A.13
0x9500	Cycle Setup 5	See Table A.11
0x9501		See Table A.12
0x9502		See Table A.13
Read-Write	**Engine Channel Select**	
0x9600	Cycle 0 Engine-Channel Select	See Table A.14
0x9601	Cycle 1 Engine-Channel Select	
0x9602	Cycle 2 Engine-Channel Select	
0x9603	Cycle 3 Engine-Channel Select	
0x9604	Cycle 4 Engine-Channel Select	
0x9605	Cycle 5 Engine-Channel Select	
Read-Write	**Button Setup** **Channel 0**	
0xA000	Tier0 Detection	See Table A.15
0xA001	Tier1 Detection	See Table A.16
0xA002	Tier2 Detection	See Table A.17
0xA003	Tier Timeouts	See Table A.18
0xA004	General Button Settings	See Table A.19
0xA005	Beta Filters	See Table A.20
0xA006	Fast Beta Filters	See Table A.21
Read-Write	**Channel 1**	
0xA100	Tier0 Detection	See Table A.15
0xA101	Tier1 Detection	See Table A.16

0xA102	Tier2 Detection	See Table A.17
0xA103	Tier Timeouts	See Table A.18
0xA104	General Button Settings	See Table A.19
0xA105	Beta Filters	See Table A.20
0xA106	Fast Beta Filters	See Table A.21
Read-Write	**Channel 2**	
0xA200	Tier0 Detection	See Table A.15
0xA201	Tier1 Detection	See Table A.16
0xA202	Tier2 Detection	See Table A.17
0xA203	Tier Timeouts	See Table A.18
0xA204	General Button Settings	See Table A.19
0xA205	Beta Filters	See Table A.20
0xA206	Fast Beta Filters	See Table A.21
Read-Write	**Channel 3**	
0xA300	Tier0 Detection	See Table A.15
0xA301	Tier1 Detection	See Table A.16
0xA302	Tier2 Detection	See Table A.17
0xA303	Tier Timeouts	See Table A.18
0xA304	General Button Settings	See Table A.19
0xA305	Beta Filters	See Table A.20
0xA306	Fast Beta Filters	See Table A.21
Read-Write	**Channel 4**	
0xA400	Tier0 Detection	See Table A.15
0xA401	Tier1 Detection	See Table A.16
0xA402	Tier2 Detection	See Table A.17
0xA403	Tier Timeouts	See Table A.18
0xA404	General Button Settings	See Table A.19
0xA405	Beta Filters	See Table A.20
0xA406	Fast Beta Filters	See Table A.21
Read-Write	**Channel 5**	
0xA500	Tier0 Detection	See Table A.15
0xA501	Tier1 Detection	See Table A.16
0xA502	Tier2 Detection	See Table A.17
0xA503	Tier Timeouts	See Table A.18
0xA504	General Button Settings	See Table A.19
0xA505	Beta Filters	See Table A.20
0xA506	Fast Beta Filters	See Table A.21
Read-Write	**Sensor Setup** Channel 0	
0xB000	CRX Select and General Channel Settings	See Table A.22
0xB001	ATI Base and Target	See Table A.23
0xB002	ATI Fine and Coarse Mirrors	See Table A.24
0xB003	ATI Compensation	See Table A.25
Read-Write	Channel 1	
0xB100	CRX Select and General Channel Settings	See Table A.22
0xB101	ATI Base and Target	See Table A.23
0xB102	ATI Fine and Coarse Mirrors	See Table A.24
0xB103	ATI Compensation	See Table A.25
Read-Write	Channel 2	
0xB200	CRX Select and General Channel Settings	See Table A.22
0xB201	ATI Base and Target	See Table A.23

0xB202	ATI Fine and Coarse Mirrors	See Table A.24
0xB203	ATI Compensation	See Table A.25
Read-Write	Channel 3	
0xB300	CRX Select and General Channel Settings	See Table A.22
0xB301	ATI Base and Target	See Table A.23
0xB302	ATI Fine and Coarse Mirrors	See Table A.24
0xB303	ATI Compensation	See Table A.25
Read-Write	Channel 4	
0xB400	CRX Select and General Channel Settings	See Table A.22
0xB401	ATI Base and Target	See Table A.23
0xB402	ATI Fine and Coarse Mirrors	See Table A.24
0xB403	ATI Compensation	See Table A.25
Read-Write	Channel 5	
0xB500	CRX Select and General Channel Settings	See Table A.22
0xB501	ATI Base and Target	See Table A.23
0xB502	ATI Fine and Coarse Mirrors	See Table A.24
0xB503	ATI Compensation	See Table A.25
Read-Write	**Rotational Encoder Setup**	
0xC000	Number of Metal Segments	See Table A.26
0xC001	Coil A Channel/Fixed Reference	See Table A.27
0xC002	Coil A Enter Threshold	See Table A.28
0xC003	Coil A Exit Threshold	See Table A.29
0xC004	Coil B Channel/Fixed Reference	See Table A.27
0xC005	Coil B Enter Threshold	See Table A.28
0xC006	Coil B Exit Threshold	See Table A.29

11 Implementation and Layout

11.1 Layout Fundamentals

NOTE

Information in the following Applications section is not part of the Azoteq component specification, and Azoteq does not warrant its accuracy or completeness. Azoteq's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

11.1.1 Power Supply Decoupling

Azoteq recommends connecting a combination of a 4.7 µF plus a 100 pF low-ESR ceramic decoupling capacitor between the VDD and VSS pins. Higher-value capacitors may be used but can impact supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the pins that they decouple (within a few millimetres).

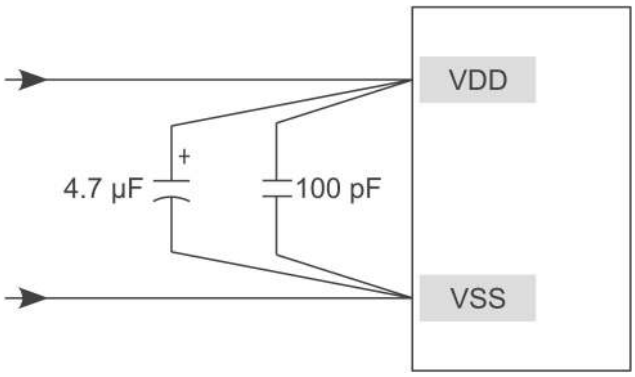


Figure 11.1: Recommended Power Supply Decoupling

11.1.2 VREG

The VREG pin requires a 2.2 µF capacitor to regulate the LDO internal to the device. This capacitor must be placed as close as possible to the microcontroller. The figure below shows an example layout where the capacitor is placed close to the IC.

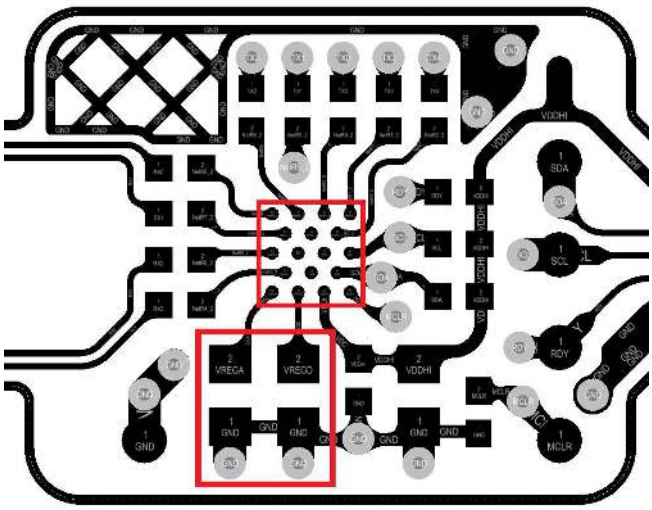


Figure 11.2: VREG Capacitor Placement Close to IC

12 Ordering Information

12.1 Ordering Code

IQS7225A zzz ppb

IC NAME	IQS7225A	=	IQS7225A	
POWER-ON CONFIGURATION	zzz	=	001	1 button self capacitance on startup. Configurable via I^2C.
PACKAGE TYPE	pp	=	QN	QFN-20 package
BULK PACKAGING	b	=	R	QFN-20 Reel (2000pcs/reel)

Figure 12.1: Order Code Description

12.2 Top Marking

12.2.1 QFN20 Package Marking Option 1

- IQS
  7225A
  pppxx

Product Name
ppp = product code
xx = batchcode

12.2.2 QFN20 Package Marking Option 2

- IQS
  722xy
  pppxx

Product Name
ppp = product code
xx = batchcode

13 Package Specification

13.1 Package Outline Description – QFN20

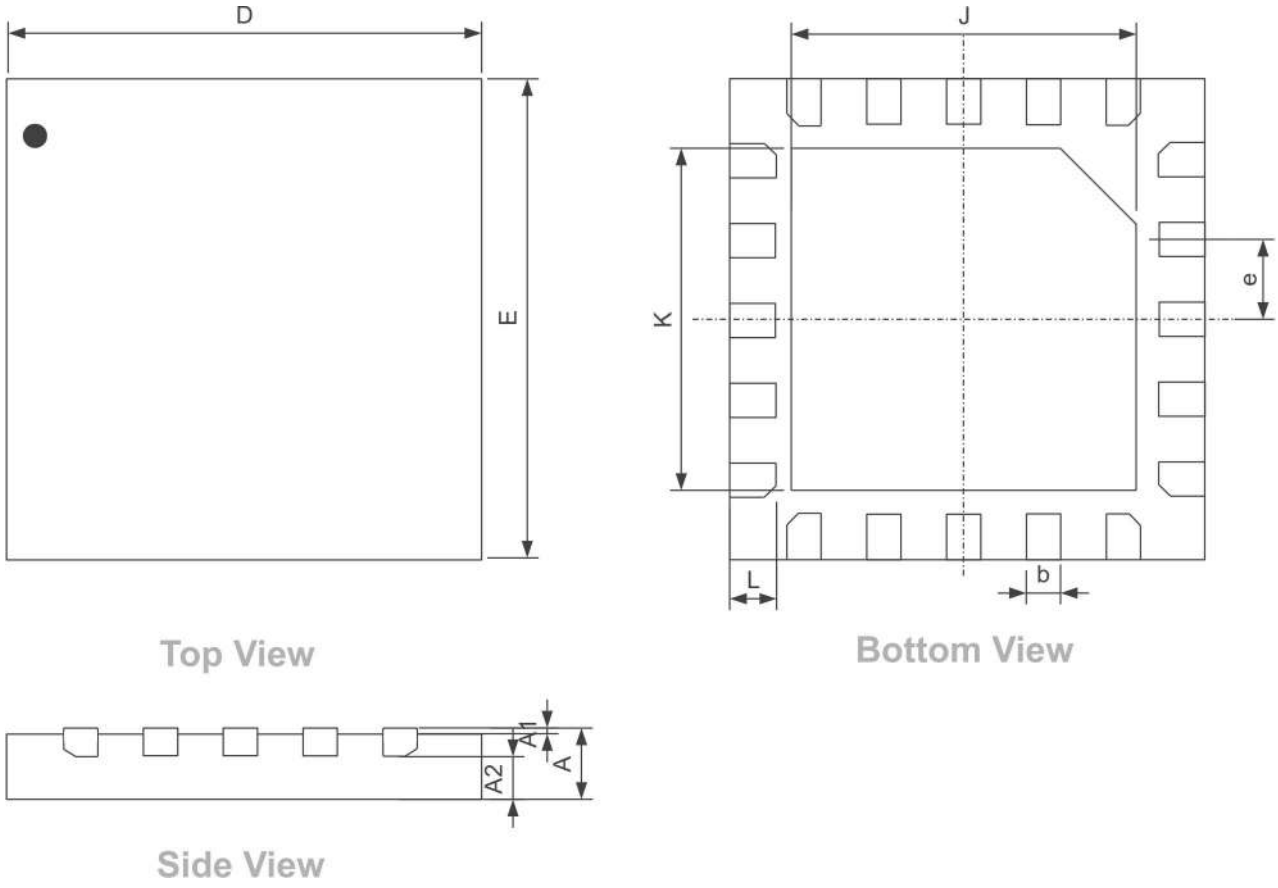
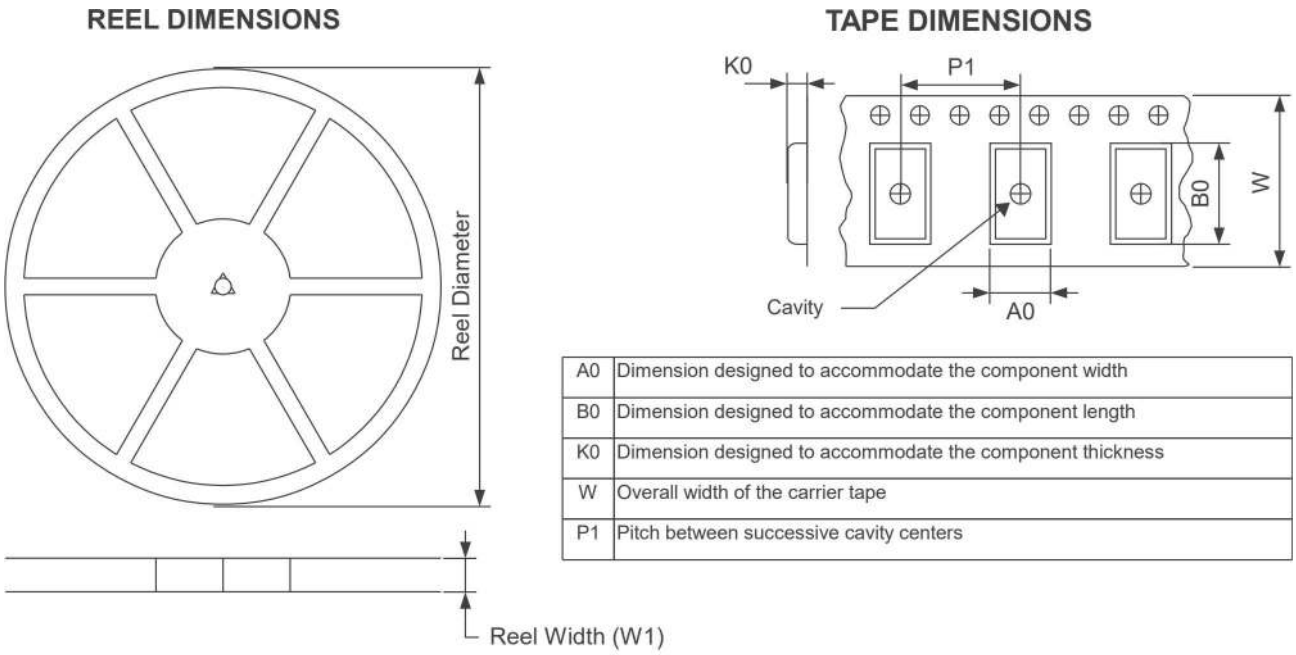


Figure 13.1: QFN (3x3)-20 Package Outline Visual Description

Table 13.1: QFN (3x3)-20 Package Outline Visual Description

Dimension	[mm]	Dimension	[mm]
A	0.5 ± 0.1	E	3
A1	0.035 ± 0.05	e	0.4
A2	0.3	J	1.7 ± 0.1
A3	0.203	K	1.7 ± 0.1
b	0.2 ± 0.05	L	0.4 ± 0.05
D	3		

13.2 Tape and Reel Specifications



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

Figure 13.2: Tape and Reel Specification

Table 13.2: Tape and reel Specifications

Package Type	Pins	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
QFN20	20	180	12.4	3.3	3.3	0.8	8	12	Q2

13.3 Moisture Sensitivity Levels

Package	MSL
QFN20	1

13.4 Reflow Specifications

Contact Azoteq

A Memory Map Descriptions

Table A.1: Application Version Information

Register: 0x0000 - 0x0004

Address	Category	Name	Value
0x0000	Application Version Info	Product Number	791
0x0001		Major Version	1
0x0002		Minor Version	10
0x0003		Patch Number (commit hash)	Value between 0 and 65535
0x0004			

Table A.2: ROM Version Information

Register: 0x0100 - 0x0104

Address	Category	Name	Value
0x1000	ROM Library Version Info	Library Number	595
0x1001		Major Version	0
0x1002		Minor Version	33
0x1003		Patch Number (commit hash)	Value between 0 and 65535
0x1004			

Table A.3: System Status

Register: 0x1000

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved								Global Halt	ULP Update	Power Mode		Reset	Tier0 Debounce	ATI Error	ATI Active

- Bit 7: **Global Halt**
  - 0: Global halt not active
  - 1: Global halt active
- Bit 6: **ULP Update**
  - 0: No ultra-low power update occured
  - 1: Ultra-low power update occured
- Bit 4-5: **Power Mode**
  - 00: Normal power mode
  - 01: Low power mode
  - 10: Ultra-low power mode
- Bit 3: **Reset**
  - 0: No reset occurred
  - 1: Reset occurred
- Bit 1: **ATI Error**
  - 0: No ATI error occurred
  - 1: ATI error occurred
- Bit 0: **ATI Active**
  - 0: ATI not active
  - 1: ATI active

Table A.4: Events

Register: 0x1001

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved				Power Event	ATI Event	Reserved							Tier2 Event	Tier1 Event	Tier0 Event

- Bit 11: **Power Event**
  - 0: No Power event occurred
  - 1: Power event occurred
- Bit 10: **ATI Event**
  - 0: No ATI event occurred
  - 1: ATI event occurred
- Bit 2: **Tier2 Event**

- 0: No Tier2 event occurred
- 1: Tier2 event occurred

› Bit 1: **Tier1 Event**
- 0: No Tier1 event occurred
- 1: Tier1 event occurred

› Bit 0: **Tier0 Event**
- 0: No Tier0 event occurred
- 1: Tier0 event occurred

Table A.5: Tier0-1 Event Status

Register: 0x1002

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved		Tier1 CH5	Tier1 CH4	Tier1 CH3	Tier1 CH2	Tier1 CH1	Tier1 CH0	Reserved		Tier0 CH5	Tier0 CH4	Tier0 CH3	Tier0 CH2	Tier0 CH1	Tier0 CH0

› Bit 0-5: **Tier0 Channel Event Status**
- 0: No Tier0 event occurred on channel
- 1: Tier0 event occurred on channel

› Bit 8-13: **Tier1 Channel Event Status**
- 0: No Tier1 event occurred on channel
- 1: Tier1 event occurred on channel

Table A.6: Tier2 Event Status

Register: 0x1003

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved										Tier2 CH5	Tier2 CH4	Tier2 CH3	Tier2 CH2	Tier2 CH1	Tier2 CH0

› Bit 0-5: **Tier2 Channel Event Status**
- 0: No Tier2 event occurred on channel
- 1: Tier2 event occurred on channel

Table A.7: Rotational Encoder Gray States

Register: 0x1004

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved														Coil A Active	Coil B Active

› Bit 0-1: **Gray Encoded State**
- 00: No Coil active
- 01: Only Coil A active
- 11: Coil A and Coil B active
- 10: Only Coil B active

Table A.8: System Control Settings

Register: 0x8000

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
I^2C Interface		Power Mode		Reserved			ULP Mode	Reserved				Reseed	Re-ATI	Reset	ACK Reset

› Bit 15-14: **I^2C Interface**
- 00: I^2C streaming mode
- 01: I^2C event mode
- 10: I^2C streaming in touch mode

› Bit 13-11: **Power Mode**
- 000: Normal Power Mode
- 001: Low Power Mode
- 010: Ultra-Low Power Mode
- 011: Halt Power Mode
- 100: Automatic Switching Power Mode

- Bit 9-10: **Auto Mode**
  Number of autonomous conversions on cycle 0 before a ULP conversion is executed
  - 00: 4 autonomous conversions
  - 01: 8 autonomous conversions
  - 10: 16 autonomous conversions
  - 11: 32 autonomous conversions
- Bit 8: **ULP Mode**
  - 0: ULP Mode Disabled
  - 1: ULP Mode Enabled
- Bit 3: **Reseed (set only, will clear when done)**
  - 1: Reseed LTA for all channels
- Bit 2: **Re-ATI (set only, will clear when done)**
  - 1: Re-ATI all channels
- Bit 1: **Reset (set only, will clear when done)**
  - 1: Perform a software reset
- Bit 0: **ACK Reset (set only, will clear when done)**
  - 1: Acknowledge device reset

Table A.9: Event Mask

Register: 0x8001

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved				Power	ATI	Reserved							Tier2	Tier1	Tier0

- Bit 11: **Power Mode Event Mask**
  - 0: Power mode event disabled
  - 1: Power mode event enabled
- Bit 10: **ATI Event Mask**
  - 0: ATI event disabled
  - 1: ATI event enabled
- Bit 2: **Tier2 Event Mask**
  - 0: Tier2 event disabled
  - 1: Tier2 event enabled
- Bit 1: **Tier1 Event Mask**
  - 0: Tier1 event disabled
  - 1: Tier1 event enabled
- Bit 0: **Tier0 Event Mask**
  - 0: Tier0 event disabled
  - 1: Tier0 event enabled

Table A.10: I^2C Communication

Register: 0x8003

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved														RW Check Disable	Stop Bit Disable

- Bit 0: **Stop Bit Disable**
  - 0: I2C communication window terminated by stop bit
  - 1: I2C communication window not terminated by stop bit, send 0xFF to slave address to terminate window
- Bit 1: **RW Check Disable**
  - 0: Write not allowed to read only registers 0x1000 - 0x1006
  - 1: Read and write allowed to read only registers 0x1000 - 0x1006

Table A.11: Cycle Setup0

Register: 0x9000,0x9100,0x9200,0x9300,0x9400,0x9500

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Conversion Frequency Period								Conversion Frequency Fraction							

- Bit 8-15: **Conversion Frequency Period**
  - Deadtime Enabled

$$\left(\frac{128}{Conversion\ Frequency\ Fraction} - 2\right)$$

- Deadtime Disabled
  $$\min\left(63\ ,\ max\left(0\ ,\ round\left(\frac{f_{clk}}{(2\cdot f_{conv}-1)}\right)\right)\right)$$
- Range: 0 - 127

› Bit 0-7: **Conversion Frequency Fraction**
- Deadtime Enabled
  $$256 * \frac{f_{conv}}{f_{clk}}$$
- Range: 0 - 255

› Note: with deadtime disabled, the following values of the conversion frequency period will result in the corresponding charge transfer frequencies:
- 1: 4.50 MHz
- 2: 3.00 MHz
- 3: 2.25 MHz
- 5: 1.50 MHz
- 8: 1.00 MHz
- 17: 500 kHz

Table A.12: Cycle Setup1

Register: 0x9001, 0x9101, 0x9201, 0x9301, 0x9401, 0x9501

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved				PXS Mode				Reserved				GND Inactive CRx	Deadtime Enabled	f_{clk} TX Freq	Vbias Enable

› Bit 8-11: **PXS Mode**
- 0000: None
- 0001: Self-capacitive
- 0010: Projected capacitance
- 0011: Inductive

› Bit 3: **GND Inactive CRx**
- 0: Inactive CRx pins floating
- 1: Inactive CRx pins grounded

› Bit 2: **Deadtime Enabled**
- 0: Deadtime disabled
- 1: Deadtime enabled

› Bit 1: **f_{clk} Tx Freq**
- 0: TX frequency set to f_{clk} Disabled
- 1: TX frequency set to f_{clk} Enabled

› Bit 0: **Vbias Enabled**
- 0: Vbias on CRX8 disabled
- 1: Vbias on CRX8 enabled

Table A.13: Cycle Setup2

Register: 0x9002, 0x9102, 0x9202, 0x9302, 0x9402, 0x9502

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved				GPIO4	GPIO3	GPIO0	Tx8	Tx7	Tx6	Tx5	Tx4	Tx3	Tx2	Tx1	Tx0

› Bit 11: **GPIO4**
- 0: GPIO4 disabled
- 1: GPIO4 enabled

› Bit 10: **GPIO3**
- 0: GPIO3 disabled
- 1: GPIO3 enabled

› Bit 9: **GPIO0**
- 0: GPIO0 disabled
- 1: GPIO0 enabled

› Bit 8: **Tx8**
- 0: Tx8 disabled
- 1: Tx8 enabled

› Bit 7: **Tx7**
- 0: Tx7 disabled
- 1: Tx7 enabled

- Bit 6: **Tx6**
  - 0: Tx6 disabled
  - 1: Tx6 enabled
- Bit 5: **Tx5**
  - 0: Tx5 disabled
  - 1: Tx5 enabled
- Bit 4: **Tx4**
  - 0: Tx4 disabled
  - 1: Tx4 enabled
- Bit 3: **Tx3**
  - 0: Tx3 disabled
  - 1: Tx3 enabled
- Bit 2: **Tx2**
  - 0: Tx2 disabled
  - 1: Tx2 enabled
- Bit 1: **Tx1**
  - 0: Tx1 disabled
  - 1: Tx1 enabled
- Bit 0: **Tx0**
  - 0: Tx0 disabled
  - 1: Tx0 enabled

Table A.14: Engine Channel Select

Register: 0x9600, 0x9601, 0x9602, 0x9603, 0x9604, 0x9605

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Engine 1 Channel Select								Engine 0 Channel Select							

- Bit 8-15: **Engine 1 Channel Select**
  - D'0': Channel 0
  - D'1': Channel 1
  - D'2': Channel 2
  - D'3': Channel 3
  - D'4': Channel 4
  - D'5': Channel 5
  - D'255': None
- Bit 0-7: **Engine 0 Channel Select**
  - D'0': Channel 0
  - D'1': Channel 1
  - D'2': Channel 2
  - D'3': Channel 3
  - D'4': Channel 4
  - D'5': Channel 5
  - D'255': None

Table A.15: Button Setup0

Register: 0xA000, 0xA100, 0xA200, 0xA300, 0xA400, 0xA500, A6000

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Tier0 Debounce Exit Threshold				Tier0 Debounce Enter Threshold				Tier0 Threshold							

- Bit 12-15: **Tier0 Debounce Exit Threshold**
  - 0000: Debounce disabled
  - 4-bit value
- Bit 8-11: **Tier0 Debounce Enter Threshold**
  - 0000: Debounce disabled
  - 4-bit value
- Bit 0-7: **Tier0 Threshold**
  - 8-bit value

Table A.16: Button Setup1

Register: 0xA001, 0xA101, 0xA201, 0xA301, 0xA401, 0xA501, 0xA601

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Tier1 Hysteresis								Tier1 Threshold							

- Bit 8-15: **Tier1 Hysteresis**
  - Tier1 hysteresis value determines the release threshold. Release threshold can be determined as follows:
    $\frac{LTA}{256} \times (\text{Threshold value} - \text{Hysteresis value})$
  - 8 bit value
- Bit 0-7: **Tier1 Threshold**
  - 8 bit value
    value $\times \frac{LTA}{256}$

Table A.17: Button Setup2

Register: 0xA002, 0xA102, 0xA202, 0xA302, 0xA402, 0xA502, 0xA602

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Tier2 Hysteresis								Tier2 Threshold							

- Bit 8-15: **Tier2 Hysteresis**
  - Tier2 hysteresis value determines the release threshold. Release threshold can be determined as follows:
    $\frac{LTA}{256} \times (\text{Threshold value} - \text{Hysteresis value})$
  - 8 bit value
- Bit 0-7: **Tier2 Threshold**
  - 8 bit value
    value $\times \frac{LTA}{256}$

Table A.18: Button Setup3

Register: 0A003, 0xA103, 0xA203, 0xA303, 0xA403, 0xA503, 0xA603

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Tier1 and 2 Timeout								Tier0 Timeout							

- Bit 8-15: **Tier1 and 2 Timeout**
  - 8-bit value * 500ms
- Bit 0-7: **Tier0 Timeout**
  - 8-bit value * 500ms

Table A.19: Button Setup4

Register: 0xA004, 0xA104, 0xA204, 0xA304, 0xA404, 0xA504, 0xA604

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Blocking Channel								Reserved				Number of Events		Temp Comp	Lin-earize Counts

- Bit 8-15: **Blocking Channel**
  - D'0': Channel 0
  - D'1': Channel 1
  - D'2': Channel 2
  - D'3': Channel 3
  - D'4': Channel 4
  - D'5': Channel 5
  - D'255': None
- Bit 2-3: **Number of Events**
  - 00: None
  - 01: Tier0 events enabled
  - 10: Tier0 and Tier1 events enabled
  - 11: Tier0, Tier1 and Tier2 events enabled
- Bit 1: **Temp Comp**
  - 0: Temperature Compensation Disabled
  - 1: Temperature Compensation Enabled ($Counts_{Temp\ Comp}$ = Counts $\times$ Target/LTA)
- Bit 0: **Linearize Counts**
  - 0: Linearize Counts Disabled
  - 1: Linearize Counts Enabled ($Counts_{linearized}$ = $Target^2$ / Counts)

Table A.20: Button Setup5

Register: 0xA005, 0xA105, 0xA205, 0xA305, 0xA405, 0xA505, 0xA605

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Low Power LTA Beta Filter				Normal Power LTA Beta Filter				Low Power Counts Beta Filter				Normal Power Counts Beta Filter			

- Bit 12-15: **Low Power LTA Beta Filter**
  - 4 bit value
- Bit 8-11: **Normal Power LTA Beta Filter**
  - 4 bit value
- Bit 4-7: **Low Power Counts Beta Filter**
  - 4 bit value
- Bit 0-3: **Normal Power Counts Beta Filter**
  - 4 bit value

Table A.21: Button Setup6

Register: 0xA006, 0xA106, 0xA206, 0xA306, 0xA406, 0xA506, 0xA606

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LTA Fast Beta Filter Bound								Low Power LTA Fast Beta Filter				Normal Power LTA Fast Beta Filter			

- Bit 8-15: **LTA Fast Beta Filter Bound**
  - 8 bit value
- Bit 4-7: **Low Power LTA Fast Beta Filter**
  - 4 bit value
- Bit 0-3: **Normal Power LTA Fast Beta Filter**
  - 4 bit value

Table A.22: CRX Select and General Channel Settings

Register: 0xB000, 0xB100, 0xB200, 0xB300, 0xB400, 0xB500

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved		ATI Band		Global Halt	Invert	Bi-direction	Channel Enable	RX3/7	RX2/6	RX1/5	RX0/4	Cs Size	Vref 0v5	Projected Bias Select	

- Bit 12-13: **ATI Band**
  - 00: 1/16 * Target
  - 01: 1/8 * Target
  - 10: 1/4 * Target
  - 11: 1/2 * Target
- Bit 11: **Global Halt**
  - 0: Global halt disabled
  - 1: Global halt enabled
- Bit 10: **Invert**
  - 0: Tier detection occurs when Counts < LTA
  - 1: Tier detection occurs when Counts > LTA
- Bit 9: **Bi-direction**
  - 0: Tier detection occurs in the direction specified by the 'Invert' option
  - 1: Tier detection occurs when Counts < LTA and when Counts > LTA
- Bit 8: **Channel Enable**
  - 0: Channel disabled
  - 1: Channel enabled
- Bit 7: **CRx3/7**
  - 0: CRx3/7 disabled
  - 1: CRx3/7 enabled
- Bit 6: **CRx2/6**
  - 0: Rx2/6 disabled
  - 1: Rx2/6 enabled
- Bit 5: **CRx1/5**
  - 0: Rx1/5 disabled
  - 1: Rx1/5 enabled
- Bit 4: **CRx0/4**
  - 0: Rx0/4 disabled
  - 1: Rx0/4 enabled
- Bit 3: **Cs Size**

- 0: 40pF
- 1: 80pF

- Bit 2: **Vref 0v5**
  - 0: 0.5V reference voltage disabled
  - 1: 0.5V reference voltage enabled
- Bit 0-1: **Projected Bias Select**
  - 00: 2μA
  - 01: 5μA
  - 10: 7μA
  - 11: 10μA

Table A.23: ATI Base and Target

Register: 0xB001, 0xB101, 0xB201, 0xB301, 0xB401, 0xB501

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ATI Target								ATI Base					ATI Mode		

- Bit 8-15: **ATI Target**
  - 8-bit value * 8
- Bit 3-7: **ATI Base**
  - 5-bit value * 16
- Bit 0-2: **ATI Mode**
  - 000: ATI disabled
  - 001: Compensation only
  - 010: ATI from compensation divider
  - 011: ATI from fine fractional divider
  - 100: ATI from coarse fractional divider
  - 101: Full ATI

Table A.24: ATI Fine and Coarse Fractional Mirrors

Register: 0xB002, 0xB102, 0xB202, 0xB302, 0xB402, 0xB502

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved			Fine Fractional Divider					Coarse Fractional Multiplier				Coarse Fractional Divider			

- Bit 9-13: **Fine Fractional Divider**
  - 5-bit value
- Bit 5-8: **Coarse Fractional Multiplier**
  - 4-bit value
- Bit 0-4: **Coarse Fractional Divider**
  - 5-bit value

Table A.25: ATI Compensation

Register: 0xB003, 0xB103, 0xB203, 0xB303, 0xB403, 0xB503

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Compensation Divider					Res	Compensation Selection									

- Bit 11-15: **Compensation Divider**
  - 5-bit value
- Bit 0-9: **Compensation Selection**
  - 10-bit value

Table A.26: Encoder angle resolution

Register: 0xC000

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Number of metal target segments															

- Bit 0-15: **Number of metal target segments**
  - 16-bit value
  - Encoder angular resolution = $\frac{360°}{4 \times \text{Number of metal target segments}}$

Table A.27: Encoder coil channel and reference select

Register: 0xC001, 0xC004

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Encoder coil channel/fixed reference								Encoder coil channel select							

- Bit 8-15: **Encoder coil channel/fixed reference**
  - D'0': Channel 0 reference
  - D'1': Channel 1 reference
  - D'2': Channel 2 reference
  - D'3': Channel 3 reference
  - D'4': Channel 4 reference
  - D'5': Channel 5 reference
  - Fixed reference if value > 5 (value*8)
- Bit 0-7: **Encoder coil channel**
  - D'0': Channel 0
  - D'1': Channel 1
  - D'2': Channel 2
  - D'3': Channel 3
  - D'4': Channel 4
  - D'5': Channel 5
  - Fixed reference if value > 5 (value*8)

Table A.28: Encoder coil channel enter threshold

Register: 0xC002, 0xC005

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Enter threshold															

- Bit 0-16: **Enter threshold**
  - 16 bit signed value

Table A.29: Encoder coil channel exit threshold

Register: 0xC003, 0xC006

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Exit threshold															

- Bit 0-16: **Exit threshold**
  - 16 bit signed value

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