LM25018 48-V, 325-mA Constant On-Time Synchronous Buck/Fly-Buck™ Regulator

1 Features

- Wide 7.5-V to 48-V input range
- Integrated 325-mA, high-side and low-side switches
- No schottky required
- Constant on-time control
- No loop compensation required
- Ultra-fast transient response
- Nearly constant operating frequency
- Intelligent peak current limit
- Adjustable output voltage from 1.225 V
- Precision 2% feedback reference
- Frequency adjustable to 1 MHz
- Adjustable undervoltage lockout
- Remote shutdown
- Thermal shutdown
- Create a custom design using the LM25018 with the WEBENCH® Power Designer

2 Applications

- Industrial equipment
- Smart power meters
- Telecommunication systems
- Isolated bias supply (Fly-Buck™)

3 Description

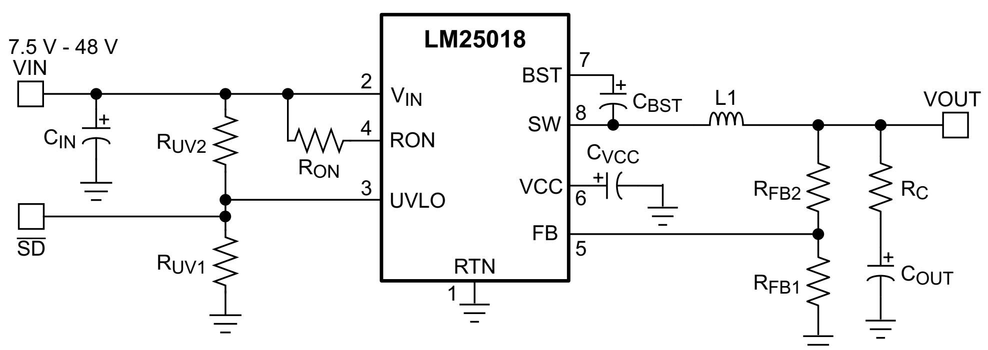
The LM25018 device is a 48-V, 325-mA synchronous step-down regulator with integrated high-side and low-side MOSFETs. The constant on-time (COT) control scheme employed in the LM25018 device requires no loop compensation, provides excellent transient response, and enables very high step-down ratios. The on-time varies inversely with the input voltage resulting in nearly constant frequency over the input voltage range. A high-voltage startup regulator provides bias power for internal operation of the IC and for integrated gate drivers.

A peak current-limit circuit protects against overload conditions. The undervoltage lockout (UVLO) circuit allows the input undervoltage threshold and hysteresis to be independently programmed. Other protection features include thermal shutdown and bias supply undervoltage lockout.

The LM25018 device is available in WSON-8 and SO Power PAD-8 plastic packages.

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM25018	SO PowerPAD (8)	4.89 mm × 3.90 mm
	WSON (8)	4.00 mm × 4.00 mm



Typical Application

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4 Revision History

Changes from Revision F (November 2017) to Revision G (May 2021) — **Page**

- Added "Synchronous Fly-Buck" to the title 1
- Hyperlinked *Applications* bullets.... 1
- Updated the numbering format for tables, figures, and cross-references throughout the document. 1

Changes from Revision E (November 2015) to Revision F (November 2017) — **Page**

- Added WEBENCH links and top nav icon for TI Designs 1
- Deleted lead temperature and related footnote from Abs Max table 5

Changes from Revision D (December 2014) to Revision E (November 2015) — **Page**

- Changed 14 V to 13 V in V_{CC} *Regulator* section 10
- Changed 8 to 4 on equation in *Input Capacitor* 17
- Changed 0.17 µF to 0.34 µF in *Input Capacitor* section 17

Changes from Revision C (December 2013) to Revision D (November 2014) — **Page**

- Added *Pin Configuration and Functions* section, *ESD Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1
- Changed VIN voltage in *Typical Application* 1
- Changed max operating junction temperature in *Recommended Operating Conditions* table. 5
- Changed *Soft-Start Circuit* graphic.... 13
- Changed *Frequency Selection* section, *Inductor Selection* section, *Output Capacitor* section, *Input Capacitor* section, and *UVLO Resistors* section.... 16
- Changed *Series Ripple Resistor* R_C section to *Type III Ripple Circuit* 17

Changes from Revision B (December 2013) to Revision C (December 2013) — **Page**

- Added Thermal Parameters.... 5

Changes from Revision A (September 2013) to Revision B (December 2013)	Page
• Changed formatting throughout document to the TI standard	1
• Changed minimum input voltage from 9 V to 7.5 V in *Features*	1
• Changed minimum input voltage from 9 V to 7.5 V in *Typical Application*	1
• Changed minimum input voltage from 9 V to 7.5 V in *Pin Descriptions*	4
• Added Absolute Maximum Junction Temperature	5
• Changed minimum input voltage from 9 V to 7.5 V in *Recommended Operating Conditions*	5

Changes from Revision * (December 2012) to Revision A (September 2013)	Page
• Added SW to RTN (100-ns transient) in *Absolute Maximum Ratings*	5

5 Pin Configuration and Functions

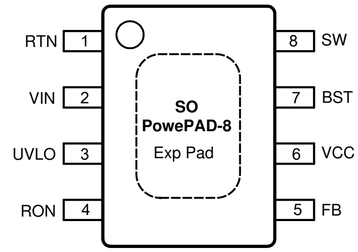


Figure 5-1. DDA Package Top View

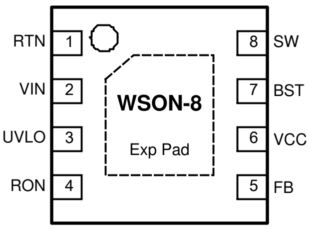


Figure 5-2. 8-Pin WSON NGU Package Top View

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION	APPLICATION INFORMATION
NO.	NAME			
1	RTN	—	Ground	Ground connection of the integrated circuit
2	VIN	I	Input Voltage	Operating input range is 7.5 V to 48 V
3	UVLO	I	Input Pin of Undervoltage Comparator	Resistor divider from V_{IN} to UVLO to GND programs the undervoltage detection threshold. An internal current source is enabled when UVLO is above 1.225 V to provide hysteresis. When the UVLO pin is pulled below 0.66 V externally, the regulator is in shutdown mode.
4	RON	I	On-Time Control	A resistor between this pin and V_{IN} sets the buck switch on-time as a function of V_{IN}. Minimum recommended on-time is 100 ns at max input voltage.
5	FB	I	Feedback	This pin is connected to the inverting input of the internal regulation comparator. The regulation level is 1.225 V.
6	VCC	O	Output from the Internal High Voltage Series Pass Regulator. Regulated at 7.6 V	The internal V_{CC} regulator provides bias supply for the gate drivers and other internal circuitry. A 1-µF decoupling capacitor is recommended.
7	BST	I	Bootstrap Capacitor	An external capacitor is required between the BST and SW pins (0.01-µF ceramic). The BST pin capacitor is charged by the V_{CC} regulator through an internal diode when the SW pin is low.
8	SW	O	Switching Node	Power switching node. Connect to the output inductor and bootstrap capacitor.
—	EP	—	Exposed Pad	Exposed pad must be connected to the RTN pin. Solder to the system ground plane on application board for reduced thermal resistance.

6 Specifications

6.1 Absolute Maximum Ratings

	MIN[1]	MAX	UNIT
V_{IN}, UVLO to RTN	–0.3	53	V
SW to RTN	–1.5	V_{IN} + 0.3	V
SW to RTN (100-ns transient)	–5	V_{IN} + 0.3	V
BST to V_{CC}		53	V
BST to SW		13	V
R_{ON} to RTN	–0.3	53	V
V_{CC} to RTN	–0.3	13	V
FB to RTN	–0.3	5	V
Maximum Junction Temperature [2]		150	°C
Storage temperature range, T_{stg}	–55	150	°C

(1) *Absolute Maximum Ratings* are limits beyond which damage to the device may occur. *Section 6.3* are conditions under which operation of the device is intended to be functional. For specifications and test conditions, see *Section 6.5* . The RTN pin is the GND reference electrically connected to the substrate.
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[1]

	MIN	MAX	UNIT
V_{IN} Voltage	7.5	48	V
Operating Junction Temperature[2]	–40	125	°C

(1) *Recommended Operating Conditions* are conditions under the device is intended to be functional. For specifications and test conditions, see *Section 6.5*.
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

6.4 Thermal Characteristics

THERMAL METRICS[1]		LM25018		UNIT
		WSON NGU	SO PowerPAD DDA	
		8 PINS		
θ_{JA}	Junction-to-ambient thermal resistance	41.3	41.1	°C/W
θ_{JC}(bot)	Junction-to-case (bottom) thermal resistance	3.2	2.4	°C/W
Ψ_{JB}	Junction-to-board thermal characteristic parameter	19.2	24.4	°C/W
θ_{JB}	Junction-to-board thermal resistance	19.1	30.6	°C/W
θ_{JC}(top)	Junction-to-case (top) thermal resistance	34.7	37.3	°C/W
Ψ_{JT}	Junction-to-top thermal characteristic parameter	0.3	6.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over –40°C to 125°C junction temperature range, unless otherwise stated. V_{IN} = 48 V unless otherwise stated. See[(1)].

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC} SUPPLY						
V_{CC} Reg	V_{CC} Regulator Output	V_{IN} = 48 V, I_{CC} = 20 mA	6.25	7.6	8.55	V
	V_{CC} Current Limit	V_{IN} = 48 V[(2)]	26			mA
	V_{CC} Undervoltage Lockout Voltage (V_{CC} increasing)		4.15	4.5	4.9	V
	V_{CC} Undervoltage Hysteresis			300		mV
	V_{CC} Dropout Voltage	V_{IN} = 9 V, I_{CC} = 20 mA		2.3		V
	I_{IN} Operating Current	Nonswitching, FB = 3 V		1.75		mA
	I_{IN} Shutdown Current	UVLO = 0 V		50	225	µA
SWITCH CHARACTERISTICS						
	Buck Switch $R_{DS(ON)}$	I_{TEST} = 200 mA, BST-SW = 7 V		0.8	1.8	Ω
	Synchronous $R_{DS(ON)}$	I_{TEST} = 200 mA		0.45	1	Ω
	Gate Drive UVLO	V_{BST} – V_{SW} Rising	2.4	3	3.6	V
	Gate Drive UVLO Hysteresis			260		mV
CURRENT LIMIT						
	Current Limit Threshold		390	575	750	mA
	Current Limit Response Time	Time to Switch Off		150		ns
	OFF-Time Generator (Test 1)	FB = 0.1 V, V_{IN} = 48 V		12		µs
	OFF-Time Generator (Test 2)	FB = 1.0 V, V_{IN} = 48 V		2.5		µs
REGULATION AND OVERVOLTAGE COMPARATORS						
	FB Regulation Level	Internal Reference Trip Point for Switch ON	1.2	1.225	1.25	V
	FB Overvoltage Threshold	Trip Point for Switch OFF		1.62		V
	FB Bias Current			60		nA
UNDERVOLTAGE SENSING FUNCTION						
	UV Threshold	UV Rising	1.19	1.225	1.26	V
	UV Hysteresis Input Current	UV = 2.5 V	–10	–20	–29	µA
	Remote Shutdown Threshold	Voltage at UVLO Falling	0.32	0.66		V
	Remote Shutdown Hysteresis			110		mV
THERMAL SHUTDOWN						
T_{sd}	Thermal Shutdown Temperature			165		°C
	Thermal Shutdown Hysteresis			20		°C

(1) All hot and cold limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) V_{CC} provides self bias for the internal gate drive and control circuits. Device thermal limitations limit external loading.

6.6 Switching Characteristics

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over –40°C to 125°C junction temperature range unless otherwise stated. V_{IN} = 48 V unless otherwise stated.

		MIN	TYP	MAX	UNIT
ON-TIME GENERATOR					
T_{ON} Test 1	V_{IN} = 32 V, R_{ON} = 100 k	270	350	460	ns
T_{ON} Test 2	V_{IN} = 48 V, R_{ON} = 100 k	188	250	336	ns
T_{ON} Test 4	V_{IN} = 10 V, R_{ON} = 250 k	1880	3200	4425	ns
MINIMUM OFF-TIME					

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over –40°C to 125°C junction temperature range unless otherwise stated. V_{IN} = 48 V unless otherwise stated.

		MIN	TYP	MAX	UNIT
Minimum Off-Timer	FB = 0 V		144		ns

6.7 Typical Characteristics

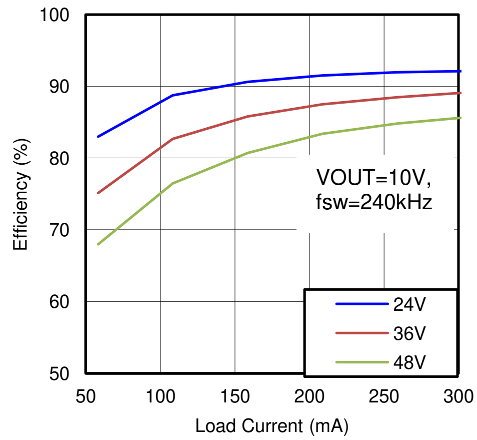


Figure 6-1. Efficiency at 240 kHz, 10 V

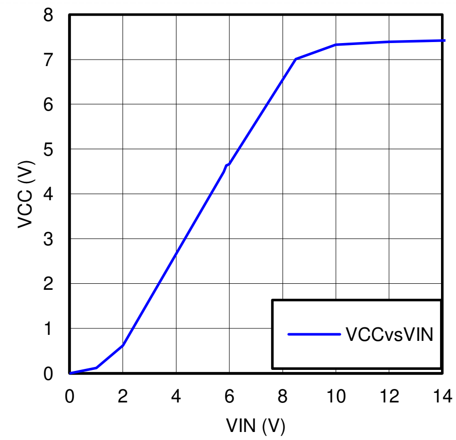


Figure 6-2. V_{CC} versus V_{IN}

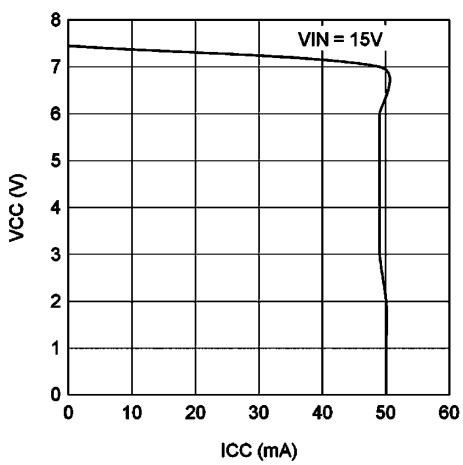


Figure 6-3. V_{CC} versus I_{CC}

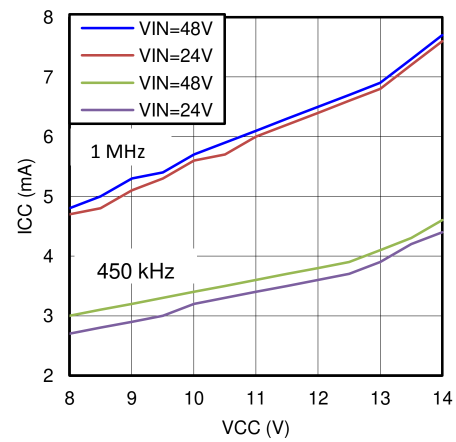


Figure 6-4. I_{CC} versus External V_{CC}

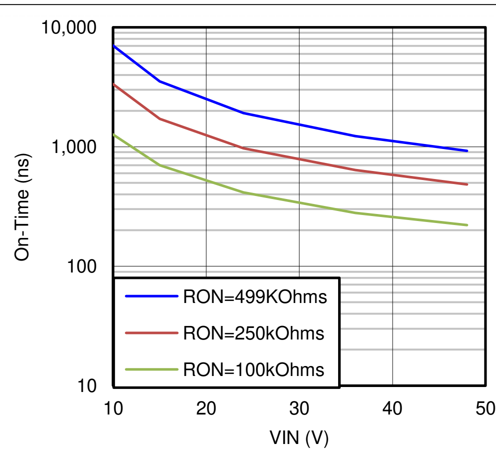


Figure 6-5. T_{ON} versus V_{IN} and R_{ON}

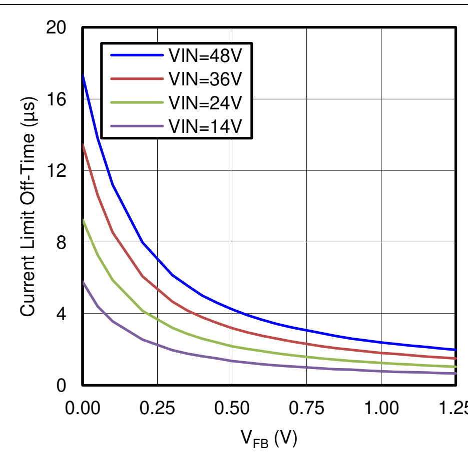


Figure 6-6. T_{OFF} (I_{LIM}) vs V_{FB} and V_{IN}

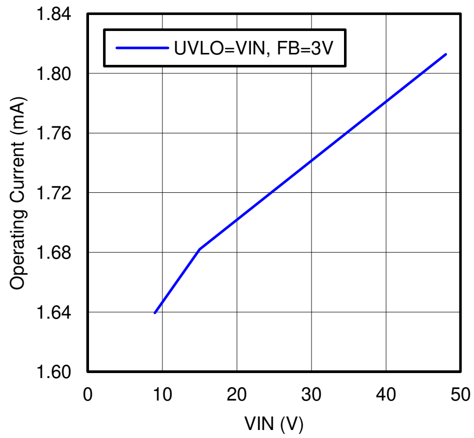


Figure 6-7. I_{IN} versus V_{IN} (Operating, Nonswitching)

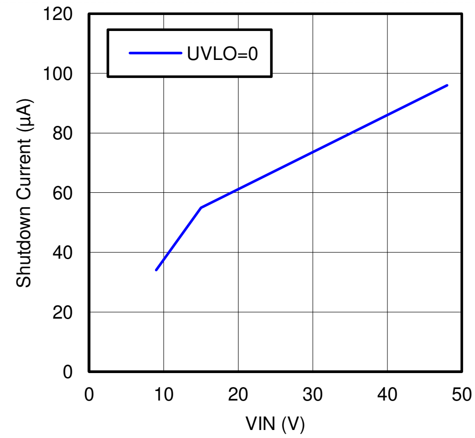


Figure 6-8. I_{IN} versus V_{IN} (Shutdown)

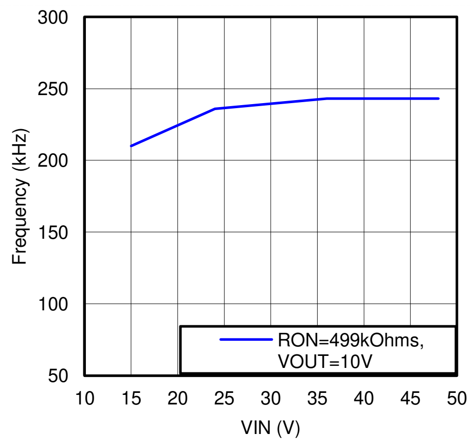


Figure 6-9. Switching Frequency versus V_{IN}

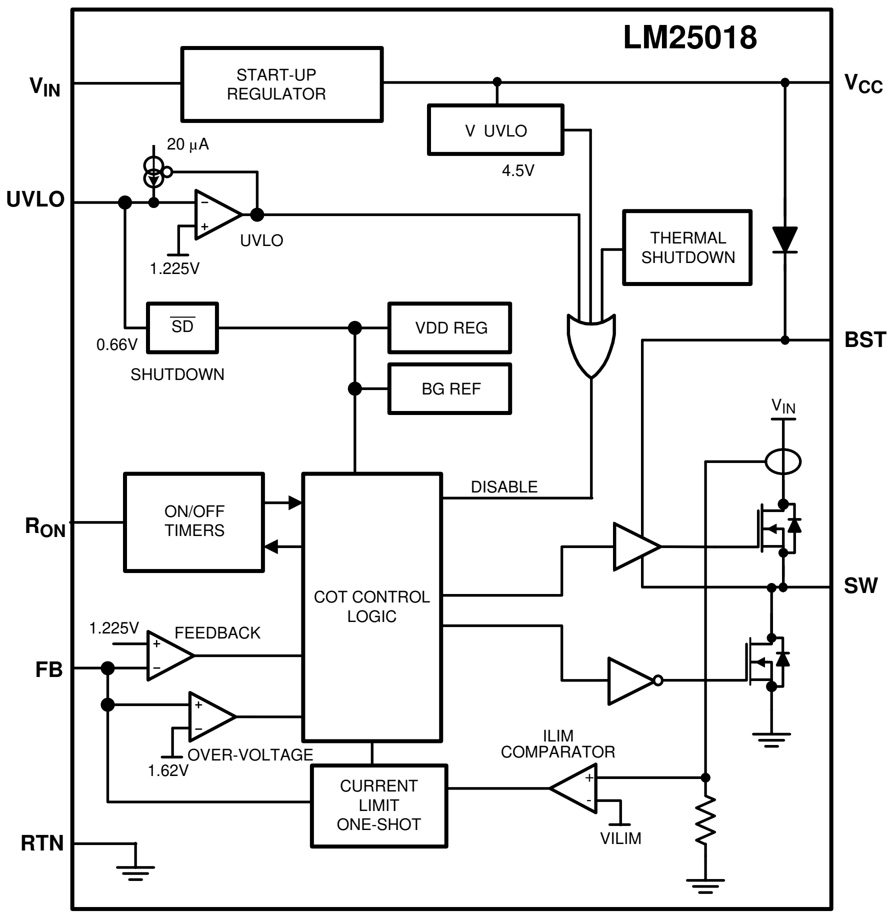
7 Detailed Description

7.1 Overview

The LM25018 step-down switching regulator features all the functions needed to implement a low-cost, efficient buck converter capable of supplying up to 325 mA to the load. This high voltage regulator contains 48 V, N-channel buck and synchronous switches, is easy to implement, and is provided in thermally-enhanced SO PowerPAD-8 and WSON-8 packages. The regulator operation is based on a constant on-time control scheme using an on-time inversely proportional to V_{IN}. This control scheme does not require loop compensation. The current limit is implemented with a forced off-time inversely proportional to V_{OUT}. This scheme ensures short circuit protection while providing minimum foldback.

The LM25018 device can be applied in numerous applications to efficiently regulate down higher voltages. This regulator is well-suited for 12-V and 24-V rails. Protection features include: thermal shutdown, undervoltage lockout (UVLO), minimum forced off-time, and an intelligent current limit.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Control Overview

The LM25018 buck regulator employs a control principle based on a comparator and a one-shot on-timer, with the output voltage feedback (FB) compared to an internal reference (1.225 V). If the FB voltage is below the reference, the internal buck switch is turned on for the one-shot timer period, which is a function of the input voltage and the programming resistor (R_{ON}). Following the on-time, the switch remains off until the FB voltage falls below the reference, but never before the minimum off-time forced by the minimum off-time one-shot timer. When the FB pin voltage falls below the reference and the minimum off-time one-shot period expires, the buck switch is turned on for another on-time one-shot period. This continues until regulation is achieved and the FB voltage is approximately equal to 1.225 V (typ).

In a synchronous buck converter, the low-side (sync) FET is on when the high-side (buck) FET is off. The inductor current ramps up when the high-side switch is on and ramps down when the high-side switch is off. There is no diode emulation feature in this IC, therefore, the inductor current can ramp in the negative direction at light load. This causes the converter to operate in continuous conduction mode (CCM) regardless of the output loading. The operating frequency remains relatively constant with load and line variations. The operating frequency can be calculated as shown in Equation 1.

$$f_{SW} = \frac{V_{OUT}}{9 \times 10^{-11} \times R_{ON}} \quad (1)$$

The output voltage (V_{OUT}) is set by two external resistors (R_{FB1} and R_{FB2}). The regulated output voltage is calculated as shown in Equation 2.

$$V_{OUT} = 1.225V \times \frac{R_{FB2} + R_{FB1}}{R_{FB1}} \quad (2)$$

This regulator regulates the output voltage based on ripple voltage at the feedback input, requiring a minimum amount of ESR for the output capacitor (C_{OUT}). A minimum of 25 mV of ripple voltage at the feedback pin (FB) is required for the LM25018. In cases where the capacitor ESR is too small, additional series resistance can be required (R_C in Figure 7-1).

For applications where lower output voltage ripple is required, the output can be taken directly from a low ESR output capacitor, as shown in Figure 7-1. However, R_C slightly degrades the load regulation.

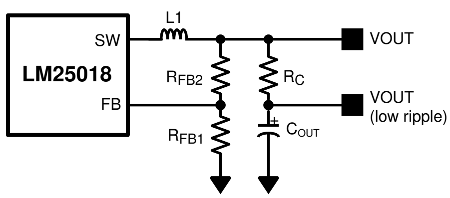


Figure 7-1. Low Ripple Output Configuration

7.3.2 V_{CC} Regulator

The LM25018 device contains an internal high voltage linear regulator with a nominal output of 7.6 V. The input pin (V_{IN}) can be connected directly to the line voltages up to 48 V. The V_{CC} regulator is internally current limited to 30 mA. The regulator sources current into the external capacitor at V_{CC}. This regulator supplies current to internal circuit blocks including the synchronous MOSFET driver and the logic circuits. When the voltage on the V_{CC} pin reaches the undervoltage lockout threshold of 4.5 V, the IC is enabled.

The V_{CC} regulator contains an internal diode connection to the BST pin to replenish the charge in the gate drive boot capacitor when SW pin is low.

At high input voltages, the power dissipated in the high voltage regulator is significant and can limit the overall achievable output power. As an example, with the input at 48 V and switching at high frequency, the V_{CC} regulator can supply up to 7 mA of current, resulting in 48 V × 7 mA = 336 mW of power dissipation. If the V_{CC} voltage is driven externally by an alternate voltage source, between 8.55 V and 13 V, the internal regulator is disabled. This reduces the power dissipation in the IC.

7.3.3 Regulation Comparator

The feedback voltage at FB is compared to an internal 1.225-V reference. In normal operation, when the output voltage is in regulation, an on-time period is initiated when the voltage at FB falls below 1.225 V. The high-side switch stays on for the on-time, causing the FB voltage to rise above 1.225 V. After the on-time period, the high-side switch stays off until the FB voltage again falls below 1.225 V. During start-up, the FB voltage is below 1.225 V at the end of each on-time, causing the high-side switch to turn on immediately after the minimum forced off-time of 144 ns. The high-side switch can be turned off before the on-time is over if the peak current in the inductor reaches the current limit threshold.

7.3.4 Overvoltage Comparator

The feedback voltage at FB is compared to an internal 1.62-V reference. If the voltage at FB rises above 1.62 V, the on-time pulse is immediately terminated. This condition can occur if the input voltage and the output load change suddenly. The high-side switch does not turn on again until the voltage at FB falls below 1.225 V.

7.3.5 On-Time Generator

The on-time for the LM25018 device is determined by the R_{ON} resistor, and is inversely proportional to the input voltage (V_{IN}), resulting in a nearly constant frequency as V_{IN} is varied over its range. The on-time equation for the LM25018 is determined in Equation 3.

$$T_{ON} = \frac{10^{-10} \times R_{ON}}{V_{IN}} \quad (3)$$

See Figure 6-5. R_{ON} must be selected for a minimum on-time (at maximum V_{IN}) greater than 100 ns, for proper operation. This requirement limits the maximum switching frequency for high V_{IN}.

7.3.6 Current Limit

The LM25018 device contains an intelligent current limit off-timer. If the current in the buck switch exceeds 575 mA, the present cycle is immediately terminated, and a non-resetable off-timer is initiated. The length of off-time is controlled by the FB voltage and the input voltage V_{IN}. As an example, when FB = 0 V and V_{IN} = 48 V, the maximum off-time is set to 16 µs. This condition occurs when the output is shorted, and during the initial part of start-up. This amount of time ensures safe short circuit operation up to the maximum input voltage of 48 V.

In cases of overload where the FB voltage is above zero volts (not a short circuit), the current limit off-time is reduced. Reducing the off-time during less severe overload reduces the amount of foldback, recovery time, and start-up time. The off-time is calculated from Equation 4.

$$T_{OFF(ILIM)} = \frac{0.07 \times V_{IN}}{V_{FB} + 0.2V} \mu s \quad (4)$$

The current limit protection feature is peak limited. The maximum average output is less than the peak.

7.3.7 N-Channel Buck Switch and Driver

The LM25018 device integrates an N-Channel Buck switch and associated floating high-voltage gate driver. The gate driver circuit works in conjunction with an external bootstrap capacitor and an internal high-voltage diode. A 0.01-µF ceramic capacitor connected between the BST pin and the SW pin provides the voltage to the driver during the on-time. During each off-time, the SW pin is at approximately 0 V, and the bootstrap capacitor charges from V_{CC} through the internal diode. The minimum off-timer, set to 144 ns, ensures a minimum time each cycle to recharge the bootstrap capacitor.

7.3.8 Synchronous Rectifier

The LM25018 device provides an internal synchronous N-Channel MOSFET rectifier. This MOSFET provides a path for the inductor current to flow when the high-side MOSFET is turned off.

The synchronous rectifier has no diode emulation mode, and is designed to keep the regulator in continuous conduction mode even during light loads which would otherwise result in discontinuous operation.

7.3.9 Undervoltage Detector

The LM25018 device contains a dual-level undervoltage lockout (UVLO) circuit. A summary of threshold voltages and operational states is provided in the *Section 7.4*. When the UVLO pin voltage is below 0.66 V, the controller is in a low current shutdown mode. When the UVLO pin voltage is greater than 0.66 V but less than 1.225 V, the controller is in standby mode. In standby mode, the V_{CC} bias regulator is active while the regulator output is disabled. When the V_{CC} pin exceeds the V_{CC} undervoltage threshold and the UVLO pin voltage is greater than 1.225 V, normal operation begins. An external set-point voltage divider from V_{IN} to GND can be used to set the minimum operating voltage of the regulator.

UVLO hysteresis is accomplished with an internal 20-µA current source that is switched on or off into the impedance of the set-point divider. When the UVLO threshold is exceeded, the current source is activated to quickly raise the voltage at the UVLO pin. The hysteresis is equal to the value of this current times the resistance R_{UV2}.

If the UVLO pin is wired directly to the V_{IN} pin, the regulator begins operation once the V_{CC} undervoltage is satisfied.

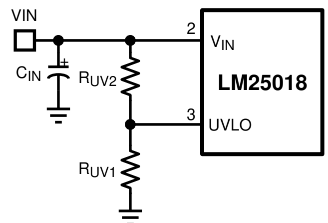


Figure 7-2. UVLO Resistor Setting

7.3.10 Thermal Protection

The LM25018 device must be operated so the junction temperature does not exceed 150°C during normal operation. An internal Thermal Shutdown circuit is provided to protect the LM25018 in the event of a higher than normal junction temperature. When activated, typically at 165°C, the controller is forced into a low power reset state, disabling the buck switch and the V_{CC} regulator. This feature prevents catastrophic failures from accidental device overheating. When the junction temperature reduces below 145°C (typical hysteresis = 20°C), the V_{CC} regulator is enabled, and normal operation is resumed.

7.3.11 Ripple Configuration

The LM25018 uses constant on-time (COT) control scheme, in which the on-time is terminated by an on-timer, and the off-time is terminated by the feedback voltage (V_{FB}) falling below the reference voltage (V_{REF}). Therefore, for stable operation, the feedback voltage must decrease monotonically, in phase with the inductor current during the off-time. Furthermore, this change in feedback voltage (V_{FB}) during off-time must be large enough to suppress any noise component present at the feedback node.

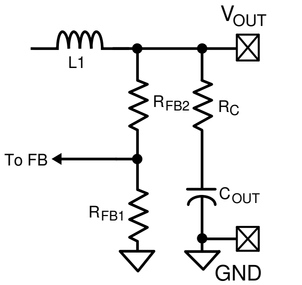
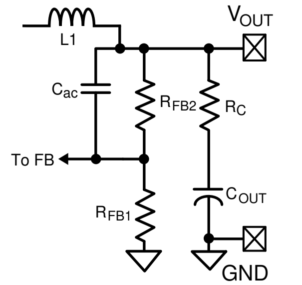
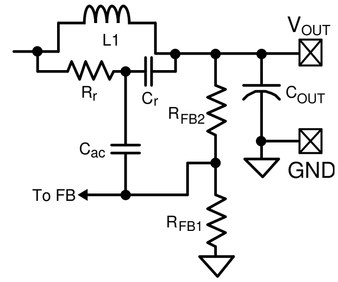
Table 7-1 shows three different methods for generating appropriate voltage ripple at the feedback node. Type 1 and Type 2 ripple circuits couple the ripple at the output of the converter to the feedback node (FB). The output voltage ripple has two components:

1. Capacitive ripple caused by the inductor current ripple charging/discharging the output capacitor.
2. Resistive ripple caused by the inductor current ripple flowing through the ESR of the output capacitor.

The capacitive ripple is not in phase with the inductor current. As a result, the capacitive ripple does not decrease monotonically during the off-time. The resistive ripple is in phase with the inductor current and decreases monotonically during the off-time. The resistive ripple must exceed the capacitive ripple at the output node (V_{OUT}) for stable operation. If this condition is not satisfied unstable switching behavior is observed in COT converters, with multiple on-time bursts in close succession followed by a long off-time.

Type 3 ripple method uses R_r and C_r and the switch node (SW) voltage to generate a triangular ramp. This triangular ramp is ac-coupled using C_{ac} to the feedback node (FB). Since this circuit does not use the output voltage ripple, it is ideally suited for applications where low output voltage ripple is required. See *AN-1481 Controlling Output Ripple and Achieving ESR Independence in Constant On-Time (COT) Regulator Designs Application Report* for more details for each ripple generation method.

Table 7-1. Ripple Configurations

TYPE 1 LOWEST COST CONFIGURATION	TYPE 2 REDUCED RIPPLE CONFIGURATION	TYPE 3 MINIMUM RIPPLE CONFIGURATION
		
$R_C \geq \frac{25\text{ mV}}{\Delta I_{L(MIN)}} \times \frac{V_{OUT}}{V_{REF}}$ (5)	$C \geq \frac{5}{f_{sw}(R_{FB2} \| R_{FB1})}$ $R_C \geq \frac{25\text{ mV}}{\Delta I_{L(MIN)}}$ (6)	$C_r = 3300\text{ pF}$ $C_{ac} = 100\text{ nF}$ $R_r C_r \leq \frac{(V_{IN(MIN)} - V_{OUT}) \times T_{ON}}{25\text{ mV}}$ (7)

7.3.12 Soft Start

A soft-start feature can be implemented with the LM25018 using an external circuit. As shown in Figure 7-3, the soft-start circuit consists of one capacitor, C_1, two resistors, R_1 and R_2, and a diode, D. During the initial start-up, the VCC voltage is established prior to the V_{OUT} voltage. Capacitor C_1 is discharged and D is thereby forward biased. The FB voltage is pulled up above the reference voltage (1.225 V) and switching is thereby disabled. As capacitor C_1 charges, the voltage at node B gradually decreases and switching commences. V_{OUT} gradually rises to maintain the FB voltage at the reference voltage. Once the voltage at node B is less than a diode drop above the FB voltage, the soft-start sequence is finished and D is reverse biased.

During the initial part of the start-up, the FB voltage can be approximated as shown in Equation 8.

$$V_{FB} = (VCC - V_D) \times \frac{R_{FB1} \times R_{FB2}}{R_2 \times (R_{FB1} + R_{FB2}) + R_{FB1} \times R_{FB2}} \quad (8)$$

C1 is charged after the first start-up. Diode D1 is optional and can be added to discharge C1 and initialize the soft-start sequence when the input voltage experiences a momentary drop.

To achieve the desired soft start, the following design guidance is recommended:

1. R_2 is selected so that V_{FB} is higher than 1.225 V for a V_{CC} of 4.5 V, but is lower than 5 V when V_{CC} is 8.55 V. If an external V_{CC} is used, V_{FB} must not exceed 5 V at maximum V_{CC}.
2. C_1 is selected to achieve the desired start-up time which can be determined from Equation 9.

$$t_S = C_1 \times \left(R_2 + \frac{R_{FB1} \times R_{FB2}}{R_{FB1} + R_{FB2}} \right) \quad (9)$$

3. R_1 is used to maintain the node B voltage at zero after the soft start is finished. A value larger than the feedback resistor divider is preferred. Note that the effect of resistor R1 is ignored in Equation 9.

With component values from the applications schematic shown in Figure 8-1, selecting C_1 = 1 μF, R_2 = 1 kΩ, and R_1 = 30 kΩ results in a soft-start time of about 2 ms.

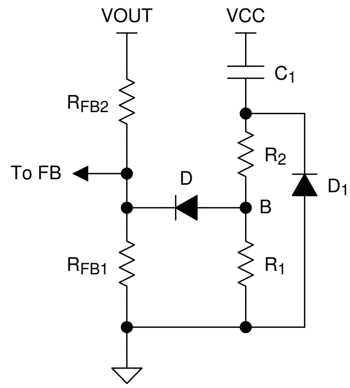


Figure 7-3. Soft-Start Circuit

7.4 Device Functional Modes

The UVLO pin controls the operating mode of the LM25018 device (see Table 7-2 for the detailed functional states).

Table 7-2. UVLO Mode

UVLO	V_{CC}	MODE	DESCRIPTION
< 0.66 V	Disabled	Shutdown	V_{CC} Regulator Disabled. Switching Disabled
0.66 V to 1.225 V	Enabled	Standby	V_{CC} Regulator Enabled Switching Disabled
> 1.225 V	V_{CC} < 4.5 V	Standby	V_{CC} Regulator Enabled. Switching Disabled
	V_{CC} > 4.5 V	Operating	V_{CC} Enabled. Switching Enabled

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The LM25018 device is step-down dc-to-dc converter. The device is typically used to convert a higher dc voltage to a lower dc voltage with a maximum available output current of 325 mA. Use the following design procedure to select component values for the LM25018 device. Alternately, use the WEBENCH® software to generate a complete design. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

8.2 Typical Applications

8.2.1 Application Circuit: 12.5-V to 48-V Input and 10-V, 325-mA Output Buck Converter

The application schematic of a buck supply is shown in Figure 8-1. For output voltage (V_{OUT}) above the maximum regulation threshold of V_{CC} (8.55 V, see *Section 6.5*), the V_{CC} pin can be connected to V_{OUT} through a diode (D2), for higher efficiency and lower power dissipation in the IC.

The design example shown in Figure 8-1 uses equations from the *Section 7.3* with component names provided in the *Typical Application*. Corresponding component designators from Figure 8-1 are also provided for each selected value.

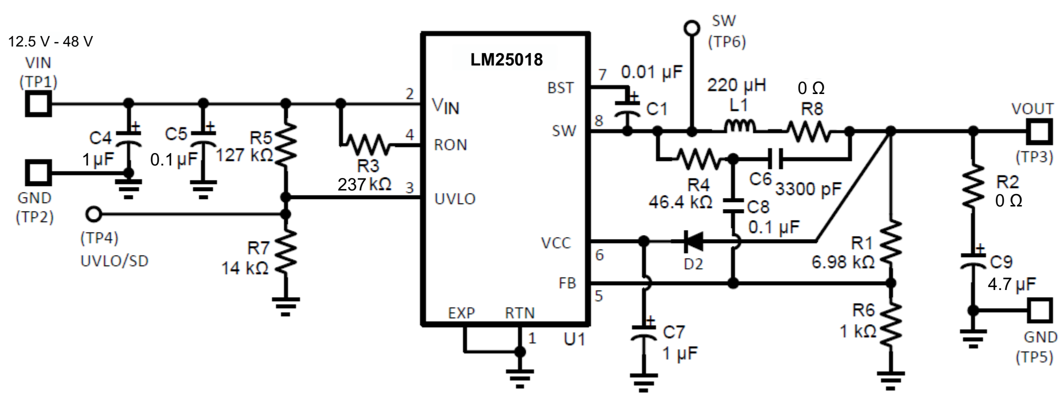


Figure 8-1. Final Schematic for 12.5-V to 48-V Input, and 10-V, 300-mA Output Buck Converter

8.2.1.1 Design Requirements

Selection of external components is illustrated through a design example. The design example specifications are shown in Table 8-1.

Table 8-1. Buck Converter Design Specifications

DESIGN PARAMETERS	VALUE
Input Voltage Range	12.5 V to 48 V
Output Voltage	10 V
Maximum Load Current	300 mA
Nominal Switching Frequency	≈ 440 kHz

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM25018 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.1.2.2 RFB1, RFB2

$V_{OUT} = V_{FB} \times (R_{FB2} / R_{FB1} + 1)$, and since V_{FB} = 1.225 V, the ratio of R_{FB2} to R_{FB1} is calculated to be 7:1. Standard values of R_{FB2} = R1 = 6.98 kΩ and R_{FB1} = R6 = 1.00 kΩ are chosen. Other values can be used as long as the 7:1 ratio is maintained.

8.2.1.2.3 Frequency Selection

At the minimum input voltage, the maximum switching frequency of LM25018 is restricted by the forced minimum off-time ($T_{OFF(MIN)}$) as shown in Equation 10.

$$f_{SW(MAX)} = \frac{1 - D_{MAX}}{T_{OFF(MIN)}} = \frac{1 - 10/12.5}{200\ \text{ns}} = 1\ \text{MHz} \quad (10)$$

Similarly, at maximum input voltage, the maximum switching frequency of LM25018 is restricted by the minimum T_{ON} as shown in Equation 11.

$$f_{SW(MAX)} = \frac{D_{MIN}}{T_{ON(MIN)}} = \frac{10/48}{100\ \text{ns}} = 2.1\ \text{MHz} \quad (11)$$

Resistor R_{ON} sets the nominal switching frequency based on Equation 12.

$$f_{SW} = \frac{V_{OUT}}{K \times R_{ON}} \quad (12)$$

where

- $K = 9 \times 10^{-11}$

Operation at high switching frequency results in lower efficiency while providing the smallest solution. For this example, 440 kHz was selected as the target switching frequency. The calculated value of R_{ON} = 253 kΩ. The standard value for R_{ON} = R3 is 237 kΩ is selected.

8.2.1.2.4 Inductor Selection

The minimum inductance is selected to limit the output ripple to 30 to 40 percent of the maximum load current. In addition, the peak inductor current at maximum load must be smaller than the minimum current limit threshold as given in *Equation 13*. The inductor current ripple is calculated using Equation 13.

$$\Delta I_L = \frac{V_{IN} - V_{OUT}}{L1 \times f_{SW}} \times \frac{V_{OUT}}{V_{IN}} \quad (13)$$

The maximum ripple is observed at maximum input voltage. To achieve the required output current of 300 mA without exceeding the peak current limit threshold, lower ripple current is required. Substituting V_{IN} = 48 V and Δ_{IL} = 30 percent × $I_{OUT\ (max)}$ results in L1 = 200 µH. The higher standard value of 220 µH is chosen. With this inductor value, the peak-to-peak minimum and maximum inductor current ripple are 21 mA and 82 mA at minimum and maximum input voltages, respectively. The peak inductor and switch current is shown in Equation 14.

$$I_{LI}(peak) = I_{OUT} + \frac{\Delta I_L(max)}{2} = 341\,mA \tag{14}$$

The calculated peak current of 341 mA is smaller than the minimum current limit threshold, which is 390 mA. In addition, the selected inductor must be able to operate at the maximum current limit threshold of 750 mA during startup and overload conditions without saturating.

8.2.1.2.5 Output Capacitor

The output capacitor is selected to minimize the capacitive ripple across it. The maximum ripple is observed at maximum input voltage and can be calculated using Equation 15.

$$C_{OUT} = \frac{\Delta I_L}{8 \times f_{sw} \times \Delta V_{ripple}} \tag{15}$$

where

- ΔV_{ripple} is the voltage ripple across the capacitor and ΔI_L is the peak-to-peak inductor current ripple.

Assuming V_{IN} = 48V and substituting ΔV_{ripple} = 10 mV gives C_{OUT} = 2.3 µF. A 4.7-µF standard value is selected for C_{OUT} = C9. An X5R or X7R type capacitor with a voltage rating 16 V or higher must be selected.

8.2.1.2.6 Type III Ripple Circuit

Type III ripple circuit as described in *Section 7.3.11* is chosen for this example. For a constant on-time converter to be stable, the injected in-phase ripple must be larger than the capacitive ripple on COUT.

Using type III ripple circuit equations, the injected ripple at the FB pin is set to a level greater than the capacitive ripple as follows:

C_r = C6 = 3300 pF

C_{ac} = C8 = 100 nF

$$R_r \le \frac{(V_{IN(MIN)} - V_{OUT}) \times T_{ON(VINMIN)}}{(25\,mV \times C_r)} \tag{16}$$

For T_{ON}, refer to Equation 3.

Ripple resistor R_r is calculated to be 57.6 kΩ. This value provides the minimum ripple for stable operation. A smaller resistance must be selected to allow for variations in T_{ON}, C_{OUT1}, and other components. R_r = R4 = 46.4 kΩ is selected for this example application.

8.2.1.2.7 V_{CC} and Bootstrap Capacitor

The V_{CC} capacitor provides charge to the bootstrap capacitor as well as internal circuitry and low-side gate driver. The bootstrap capacitor provides charge to high-side gate driver. The recommended value for CV_{CC} = C7 is 1 µF. A good value for C_{BST} = C1 is 0.01 µF.

8.2.1.2.8 Input Capacitor

Input capacitor must be large enough to limit the input voltage ripple, which is calculated using Equation 17.

$$C_{IN} \ge \frac{I_{OUT(MAX)}}{4 \times f_{SW} \times \Delta V_{IN}} \tag{17}$$

Choosing a ΔV_{IN} = 0.5 V gives a minimum C_{IN} = 0.34 µF. A standard value of 1 µF is selected for C_{IN} = C4 . The input capacitor must be rated for the maximum input voltage under all conditions. A 50-V, X7R dielectric must be selected for this design.

Input capacitor must be placed directly across V_{IN} and RTN (pin 2 and 1) of the IC. If it is not possible to place all of the input capacitor close to the IC, a 0.1-µF capacitor must be placed near the IC to provide a bypass path for the high frequency component of the switching current. This helps limit the switching noise.

8.2.1.2.9 UVLO Resistors

The UVLO resistors R_{UV1} and R_{UV2} set the UVLO threshold and hysteresis according to the following relationship between Equation 18 and Equation 19.

$$V_{IN}(HYS) = I_{HYS} \times R_{UV2} \tag{18}$$

$$V_{IN}(UVLO,rising) = 1.225V \times \left(\frac{R_{UV2}}{R_{UV1}} + 1\right) \tag{19}$$

where

- I_{HYS} = 20 µA

Setting UVLO hysteresis of 2.5 V and UVLO rising threshold of 12 V results in R_{UV1} = 14.53 kΩ and R_{UV2} = 125 kΩ. Selecting standard values of R_{UV1} = R7 = 14 kΩ and R_{UV2} = R5 = 127 kΩ results in UVLO thresholds and hysteresis of 12.5 V to 2.5 V, respectively.

8.2.2 Application Curves

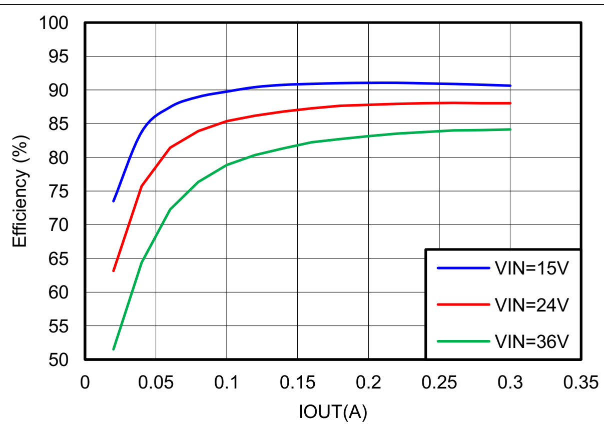


Figure 8-2. Efficiency versus Load Current

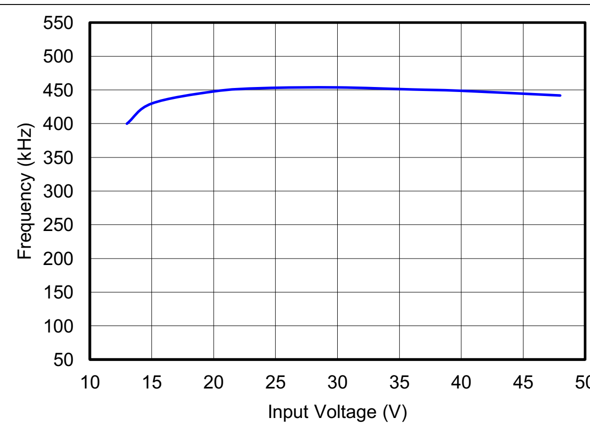


Figure 8-3. Frequency versus Input Voltage (I_{OUT} = 100 mA)

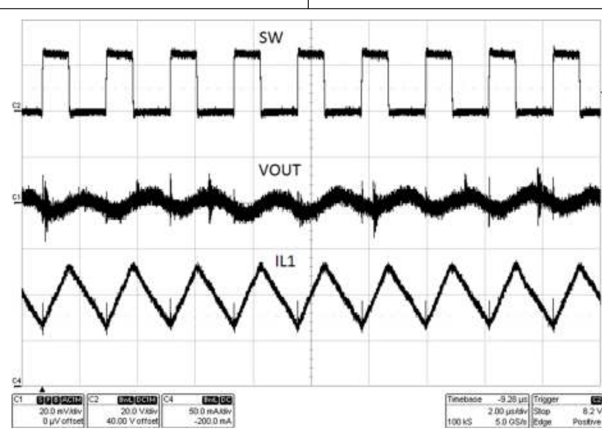


Figure 8-4. Typical Switching Waveform (V_{IN} = 24 V, I_{OUT} = 100 mA)

8.2.3 Typical Isolated DC-DC Converter Using LM25018

An isolated supply using LM25018 is shown in Figure 8-5. Inductor (L) in a typical buck circuit is replaced with a coupled inductor (X1). A diode (D1) is used to rectify the voltage on a secondary output. The nominal voltage at the secondary output (V_{OUT2}) is given by Equation 20.

$$V_{OUT2} = V_{OUT1} \times \frac{N_S}{N_P} - V_F \quad (20)$$

where

- V_F is the forward voltage drop of D1.
- N_P and N_S are the number of turns on the primary and secondary of coupled inductor X1.

For output voltage (V_{OUT1}) more than one diode drop above the maximum V_{CC} (8.55 V), the V_{CC} pin can be diode connected to V_{OUT1} for higher efficiency and low dissipation in the IC. See the *AN-2292 Designing an Isolated Buck (Flybuck) Converter Application Report* for a complete isolated bias design with a Fly-Buck™ converter.

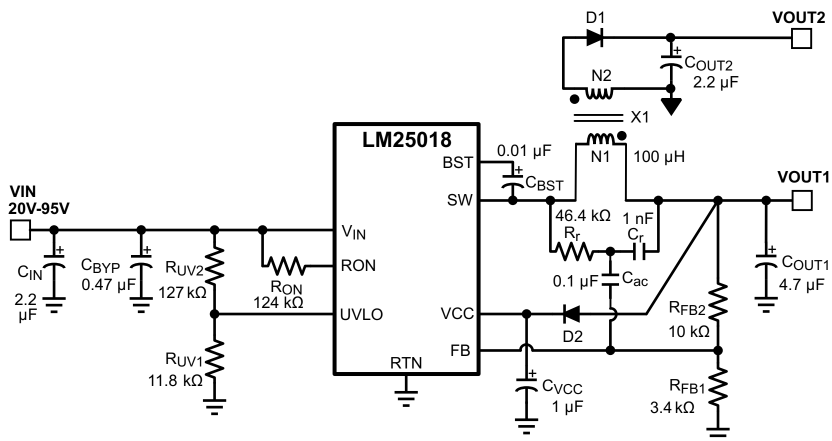


Figure 8-5. Typical Isolated Application Schematic

8.2.3.1 Design Requirements

DESIGN PARAMETERS	VALUE
Input Range	15 V to 48 V
Primary Output Voltage	5.25 V
Secondary (Isolated) Output Voltage	4.75 V
Maximum Output Current (Primary + Secondary)	300 mA
Maximum Power Output	1.5 W
Nominal Switching Frequency	500 kHz

8.2.3.2 Detailed Design Procedure

8.2.3.2.1 Transformer Turns Ratio

The transformer turns ratio is selected based on the ratio of the primary output voltage to the secondary (isolated) output voltage. In this design example, the two outputs are nearly equal and a 1:1 turns ratio transformer is selected. Therefore, N2 / N1 = 1. If the secondary (isolated) output voltage is significantly higher or lower than the primary output voltage, a turns ratio less than or greater than 1 is recommended. The primary output voltage is normally selected based on the input voltage range such that the duty cycle of the converter does not exceed 50% at the minimum input voltage. This condition is satisfied if VOUT1 < V_{IN_MIN} / 2.

8.2.3.2.2 Total IOUT

The total primary referred load current is calculated by multiplying the isolated output loads by the turns ratio of the transformer as shown in Equation 21.

$$I_{OUT(MAX)} = I_{OUT1} + I_{OUT2} \times \frac{N2}{N1} = 0.3\ A \tag{21}$$

8.2.3.2.3 RFB1, RFB2

The feedback resistors are selected to set the primary output voltage. The selected value for R_{FB1} is 3.40 kΩ. R_{FB2} can be calculated using the following equations to set V_{OUT1} to the specified value of 5 V. A standard resistor value of 10 kΩ is selected for R_{FB2}.

$$V_{OUT1} = 1.225V \times \left(1 + \frac{R_{FB2}}{R_{FB1}}\right) \tag{22}$$

$$\rightarrow R_{FB2} = \left(\frac{V_{OUT1}}{1.225} - 1\right) \times R_{FB1} = 10.4\ k\Omega \tag{23}$$

8.2.3.2.4 Frequency Selection

Equation 1 is used to calculate the value of R_{ON} required to achieve the desired switching frequency.

$$f_{SW} = \frac{V_{OUT1}}{K \times R_{ON}} \tag{24}$$

where

- $K = 9 \times 10^{-11}$

For V_{OUT1} of 5 V and f_{SW} of 500 kHz, the calculated value of R_{ON} is 111 kΩ. A standard value of 124 kΩ is selected for this design to allow for second-order effects at high switching frequency that are not included in Equation 24.

8.2.3.2.5 Transformer Selection

A coupled inductor or a flyback-type transformer is required for this topology. Energy is transferred from primary to secondary when the low-side synchronous switch of the buck converter is conducting.

The maximum inductor primary ripple current that can be tolerated without exceeding the buck switch peak current limit threshold (0.39-A minimum) is given by Equation 25.

$$\Delta I_{L1} = \left(0.39\ A - I_{OUT1} - I_{OUT2} \times \frac{N2}{N1}\right) \times 2 = 0.18\ A \tag{25}$$

Using the maximum peak-to-peak inductor ripple current ΔI_{L1} from Equation 25, the minimum inductor value is given by Equation 26.

$$L1 = \frac{V_{IN(MAX)} - V_{OUT}}{\Delta I_{L1} \times f_{SW}} \times \frac{V_{OUT}}{V_{IN(MAX)}} = 49.7\ \mu H \tag{26}$$

A higher value of 100 μH is selected to insure the high-side switch current does not exceed the minimum peak current limit threshold.

8.2.3.2.6 Primary Output Capacitor

In a conventional buck converter, the output ripple voltage is calculated as shown in Equation 27.

$$\Delta V_{OUT} = \frac{\Delta I_{L1}}{8 \times f \times C_{OUT1}} \tag{27}$$

To limit the primary output ripple voltage ΔV_{OUT1} to approximately 50 mV, an output capacitor C_{OUT1} of 0.45 µF would be required for a conventional buck converter.

Figure 8-6 shows the primary winding current waveform (I_{L1}) of a Fly-Buck converter. The reflected secondary winding current adds to the primary winding current during the buck switch off-time. Because of this increased current, the output voltage ripple is not the same as in conventional buck converter. The output capacitor value calculated in Equation 27 must be used as the starting point. Optimization of output capacitance over the entire line and load range must be done experimentally. If the majority of the load current is drawn from the secondary isolated output, a better approximation of the primary output voltage ripple is given by Equation 28.

$$\Delta V_{OUT1} = \frac{\left(I_{OUT2} \times \frac{N2}{N1}\right) \times T_{ON(MAX)}}{C_{OUT1}} \tag{28}$$

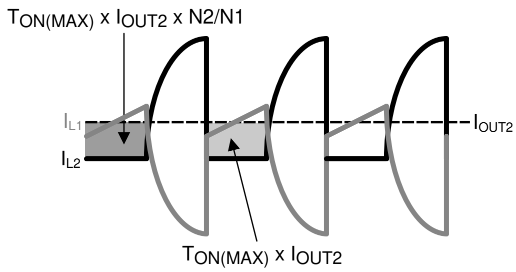


Figure 8-6. Current Waveforms for C_{OUT1} Ripple Calculation

To limit the maximum primary output voltage ripple due to reflected secondary current to 50 mV, an output capacitor (C_{OUT1}) of 4 µF is required. A standard 4.7-µF, 16-V capacitor is selected for this design. If lower output voltage ripple is required, a higher value must be selected for C_{OUT1} and C_{OUT2}.

8.2.3.2.7 Secondary Output Capacitor

A simplified waveform for secondary output current (I_{OUT2}) is shown in Figure 8-7.

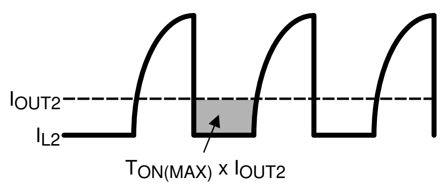


Figure 8-7. Secondary Current Waveforms for C_{OUT2} Ripple Calculation

The secondary output current (I_{OUT2}) is sourced by C_{OUT2} during on-time of the buck switch, T_{ON}. Ignoring the current transition times in the secondary winding, the secondary output capacitor ripple voltage can be calculated using Equation 29.

$$\Delta V_{OUT2} = \frac{I_{OUT2} \times T_{ON(MAX)}}{C_{OUT2}} \tag{29}$$

For a 1:1 transformer turns ratio, the primary and secondary voltage ripple equations are identical. A C_{OUT2} value of 2.2 µF is selected for this design example.

If lower output voltage ripple is required, a higher value must be selected for C_{OUT1} and C_{OUT2}.

8.2.3.2.8 Type III Feedback Ripple Circuit

Type III ripple circuit as described in *Section 7.3.11* is required for the Fly-Buck topology. Type I and Type II ripple circuits use series resistance and the triangular inductor ripple current to generate ripple at V_{OUT} and the FB pin. The primary ripple current of a Fly-Buck is the combination or primary and reflected secondary currents as shown in Figure 8-6. In the Fly-Buck topology, Type I and Type II ripple circuits suffer from large jitter as the reflected load current affects the feedback ripple.

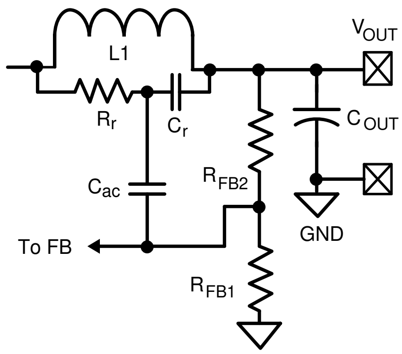


Figure 8-8. Type III Ripple Circuit

Selecting the Type III ripple components using the equations from the *Section 7.3.11* section ensures that the FB pin ripple is be greater than the capacitive ripple from the primary output capacitor C_{OUT1}. The feedback ripple component values are chosen as shown in Equation 30.

$$C_r = 1000\ \text{pF}$$
$$C_{ac} = 0.1\ \mu\text{F}$$
$$R_r C_r \leq \frac{(V_{IN(MIN)} - V_{OUT}) \times T_{ON}}{100\ \text{mV}} \quad (30)$$

The calculated value for Rr is 66 kΩ. This value provides the minimum ripple for stable operation. A smaller resistance must be selected to allow for variations in T_{ON}, C_{OUT1}, and other components. For this design, Rr value of 46.4 kΩ is selected.

8.2.3.2.9 Secondary Diode

The reverse voltage across secondary-rectifier diode D1 when the high-side buck switch is off can be calculated using Equation 31.

$$V_{D1} = \frac{N2}{N1} V_{IN} \quad (31)$$

For a V_{IN_MAX} of 48 V and the 1:1 turns ratio of this design, a 60-V Schottky is selected.

8.2.3.2.10 V_{CC} and Bootstrap Capacitor

A 1-µF capacitor of 16-V or higher rating is recommended for the V_{CC} regulator bypass capacitor.

A good value for the BST pin bootstrap capacitor is 0.01-µF with a 16-V or higher rating.

8.2.3.2.11 Input Capacitor

The input capacitor is typically a combination of a smaller bypass capacitor located near the regulator IC and a larger bulk capacitor. The total input capacitance must be large enough to limit the input voltage ripple to a desired amplitude. For input ripple voltage ΔV_{IN}, C_{IN} can be calculated using Equation 32.

$$C_{IN} \geq \frac{I_{OUT(MAX)}}{4 \times f \times \Delta V_{IN}} \quad (32)$$

Choosing a ΔV_{IN} of 0.5 V gives a minimum C_{IN} of 0.3 µF. A standard value of 0.47 µF is selected for C_{BYP} in this design. A bulk capacitor of higher value reduces voltage spikes due to parasitic inductance between the power source to the converter. A standard value of 2.2 µF is selected for for C_{IN} in this design. The voltage ratings of the two input capacitors must be greater than the maximum input voltage under all conditions.

8.2.3.2.12 UVLO Resistors

UVLO resistors R_{UV1} and R_{UV2} set the undervoltage lockout threshold and hysteresis according to Equation 33 and Equation 34.

$$V_{IN\,(HYS)} = I_{HYS} \times R_{UV2} \quad (33)$$

$$V_{IN}(\text{UVLO, rising}) = 1.225\text{V} \times \left(\frac{R_{UV2}}{R_{UV1}} + 1\right) \quad (34)$$

where

- I_{HYS} = 20 µA, typical

For a UVLO hysteresis of 2.5 V and UVLO rising threshold of 15 V, Equation 33 and Equation 34 require R_{UV1} of 11.8 kΩ and R_{UV2} of 127 kΩ.

8.2.3.2.13 V_{CC} Diode

Diode D2 is an optional diode connected between V_{OUT1} and the V_{CC} regulator output pin. When V_{OUT1} is more than one diode drop greater than the V_{CC} voltage, the V_{CC} bias current is supplied from V_{OUT1}. This results in reduced power losses in the internal V_{CC} regulator which improves converter efficiency. V_{OUT1} must be set to a voltage at least one diode drop higher than 8.55 V (the maximum V_{CC} voltage) if D2 is used to supply bias current.

8.2.3.3 Application Curves

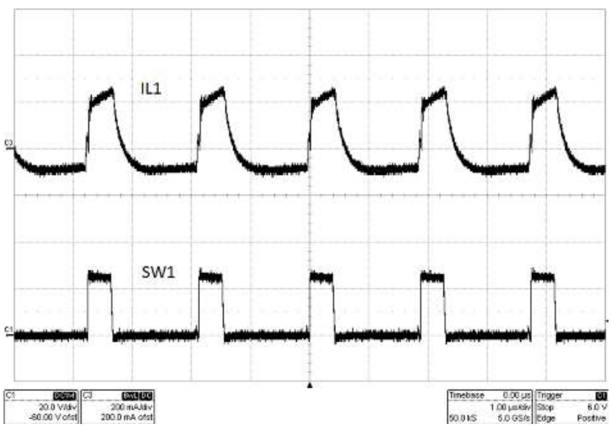


Figure 8-9. Steady State Waveform (V_{IN} = 24 V, I_{OUT1} = 0 mA, I_{OUT2} = 200 mA)

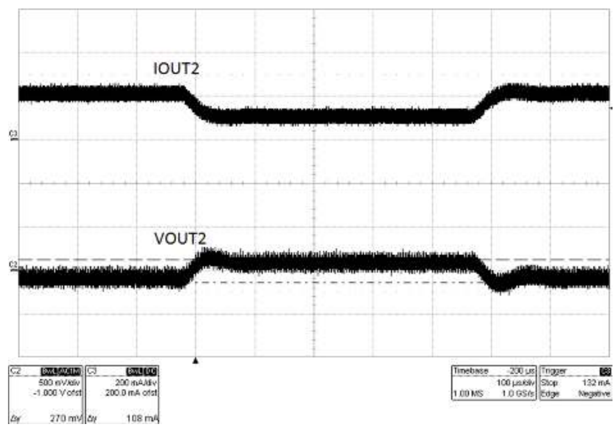


Figure 8-10. Step Load Response (V_{IN} = 24 V, I_{OUT1} = 0, Step Load on I_{OUT2} = 100 mA to 200 mA)

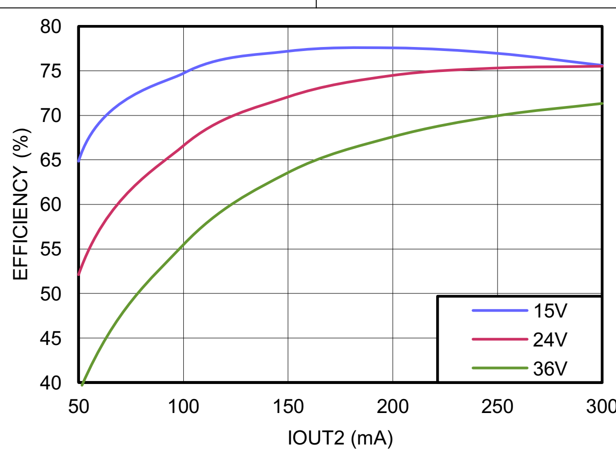


Figure 8-11. Efficiency at 500 kHz, V_{OUT1} = 5 V

9 Power Supply Recommendations

The LM25018 is a power-management device. The power supply for the device is any DC voltage source within the specified input range.

10 Layout

10.1 Layout Guidelines

A proper layout is essential for optimum performance of the circuit. In particular, the following guidelines must be observed:

1. C_{IN}: The loop consisting of input capacitor (C_{IN}), V_{IN} pin, and RTN pin carries switching currents. Therefore, the input capacitor must be placed close to the IC, directly across V_{IN} and RTN pins, and the connections to these two pins must be direct to minimize the loop area. In general, it is not possible to accommodate all of input capacitance near the IC. A good practice is to use a 0.1-µF or 0.47-µF capacitor directly across the V_{IN} and RTN pins close to the IC, and the remaining bulk capacitor as close as possible (see Figure 10-1).
2. C_{VCC} and C_{BST}: The V_{CC} and bootstrap (BST) bypass capacitors supply switching currents to the high and low side gate drivers. These two capacitors must also be placed as close to the IC as possible, and the connecting trace length and loop area should be minimized (see Figure 10-1).
3. The Feedback trace carries the output voltage information and a small ripple component that is necessary for proper operation of LM25018. Therefore, take care while routing the feedback trace to avoid coupling any noise to this pin. In particular, feedback trace should not run close to magnetic components, or parallel to any other switching trace.
4. SW trace: The SW node switches rapidly between V_{IN} and GND every cycle and is therefore a possible source of noise. The SW node area should be minimized. In particular, the SW node should not be inadvertently connected to a copper plane or pour.

10.2 Layout Example

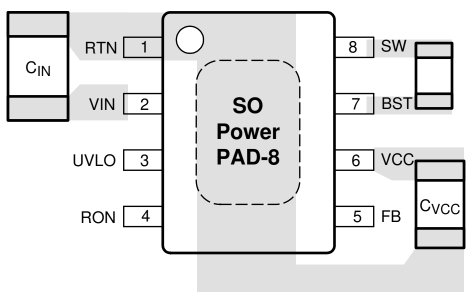


Figure 10-1. Placement of Bypass Capacitors

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.1.2 Development Support

11.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM25018 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

11.2 Documentation Support

11.2.1 Related Documentation

- *AN-1481 Controlling Output Ripple and Achieving ESR Independence in Constant On-Time (COT) Regulator Designs Application Report*
- *AN-2292 Designing an Isolated Buck (Flybuck) Converter Application Report*

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.5 Trademarks

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WEBENCH® are registered trademarks of Texas Instruments.
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11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM25018MR/NOPB	ACTIVE	SO PowerPAD	DDA	8	95	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	L25018 MR	Samples
LM25018MRE/NOPB	ACTIVE	SO PowerPAD	DDA	8	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	L25018 MR	Samples
LM25018MRX/NOPB	ACTIVE	SO PowerPAD	DDA	8	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	L25018 MR	Samples
LM25018SD/NOPB	ACTIVE	WSON	NGU	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L25018	Samples
LM25018SDE/NOPB	ACTIVE	WSON	NGU	8	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L25018	Samples
LM25018SDX/NOPB	ACTIVE	WSON	NGU	8	4500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L25018	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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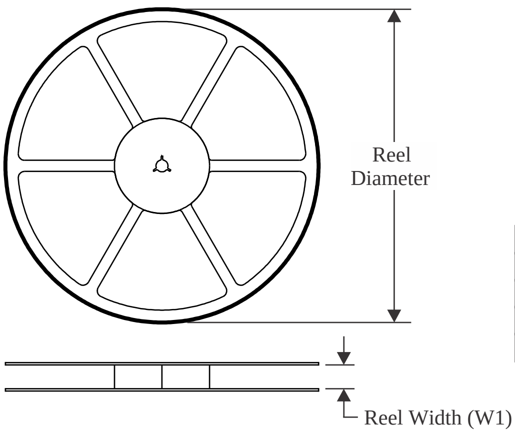
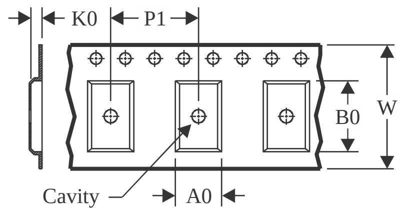
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

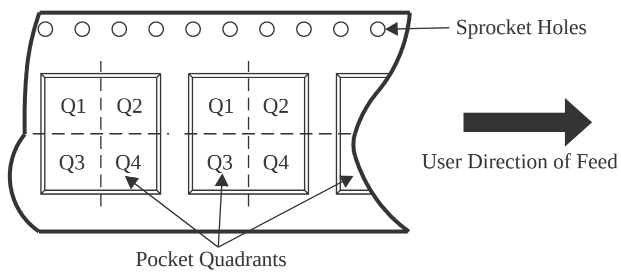


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

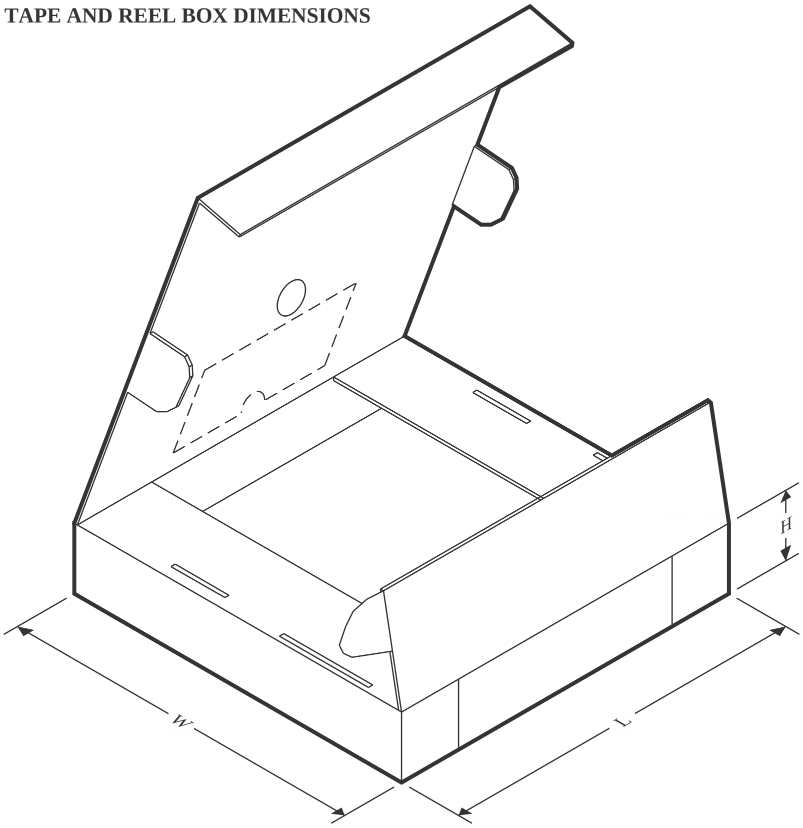
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM25018MRE/NOPB	SO PowerPAD	DDA	8	250	178.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM25018MRX/NOPB	SO PowerPAD	DDA	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM25018SD/NOPB	WSON	NGU	8	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM25018SDE/NOPB	WSON	NGU	8	250	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM25018SDX/NOPB	WSON	NGU	8	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

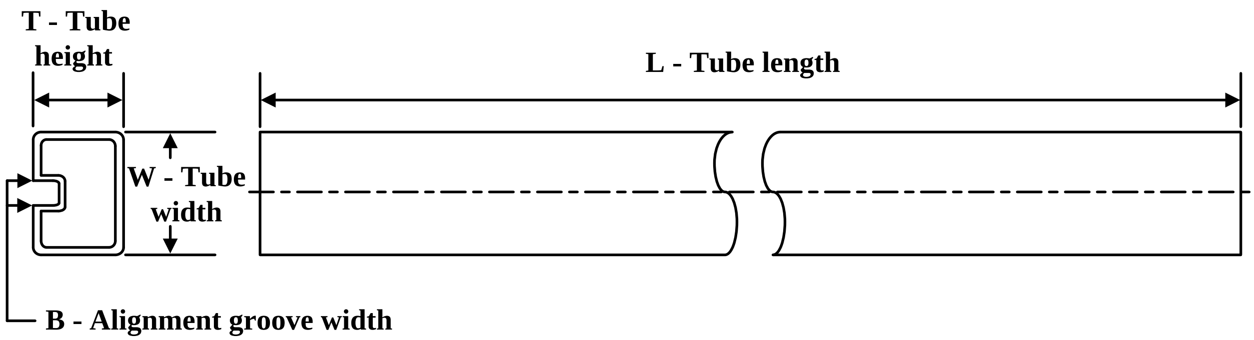
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

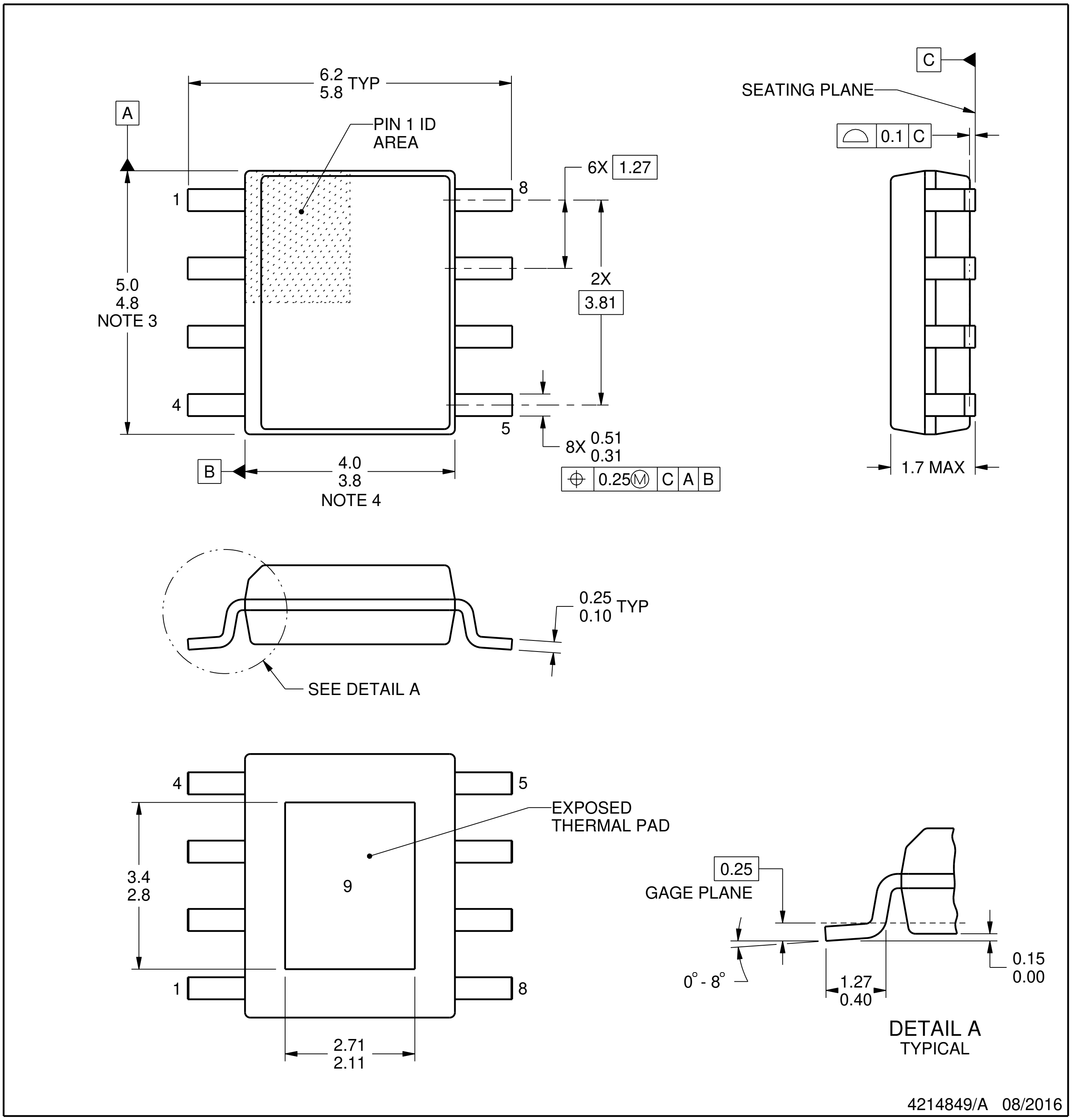
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM25018MRE/NOPB	SO PowerPAD	DDA	8	250	208.0	191.0	35.0
LM25018MRX/NOPB	SO PowerPAD	DDA	8	2500	356.0	356.0	35.0
LM25018SD/NOPB	WSON	NGU	8	1000	210.0	185.0	35.0
LM25018SDE/NOPB	WSON	NGU	8	250	210.0	185.0	35.0
LM25018SDX/NOPB	WSON	NGU	8	4500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

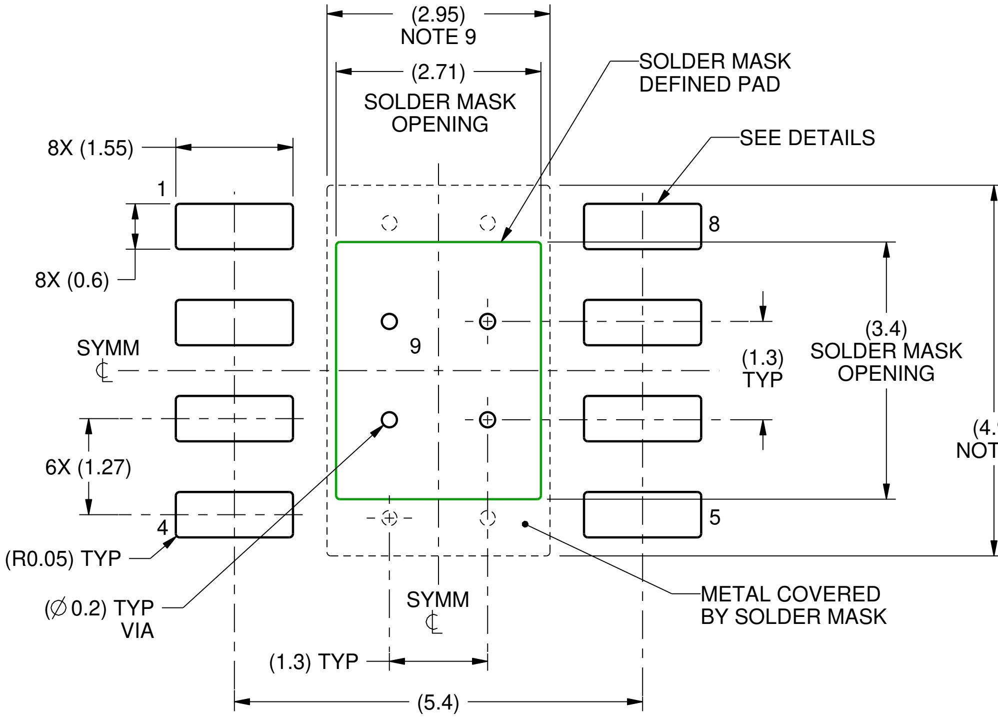
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM25018MR/NOPB	DDA	HSOIC	8	95	495	8	4064	3.05



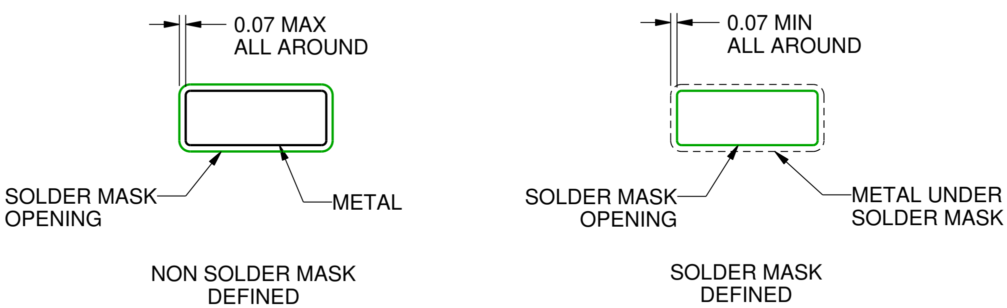
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.



LAND PATTERN EXAMPLE
SCALE:10X

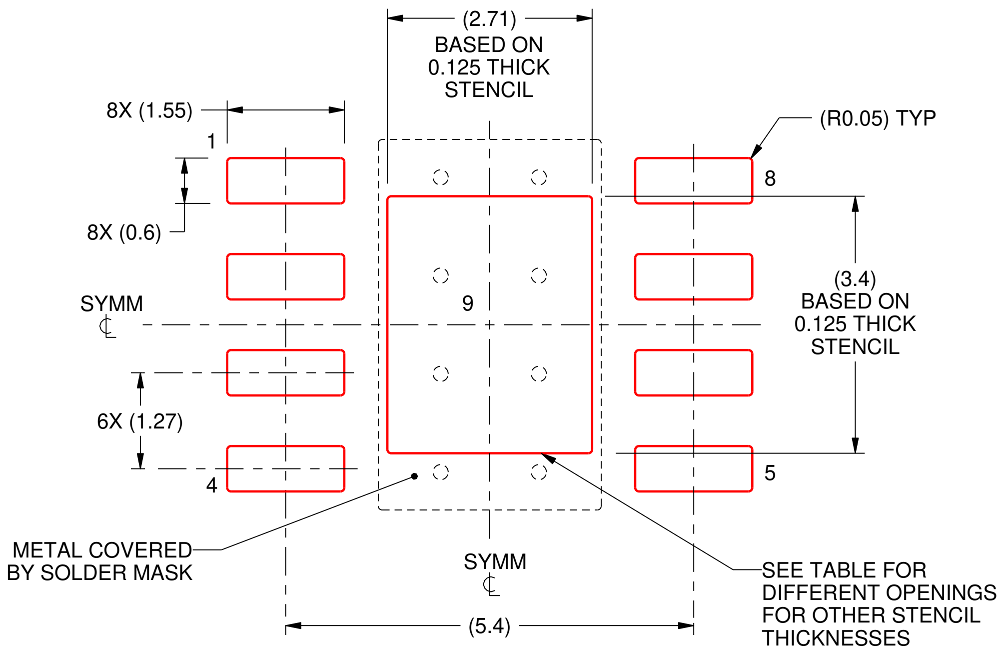


SOLDER MASK DETAILS
PADS 1-8

4214849/A 08/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



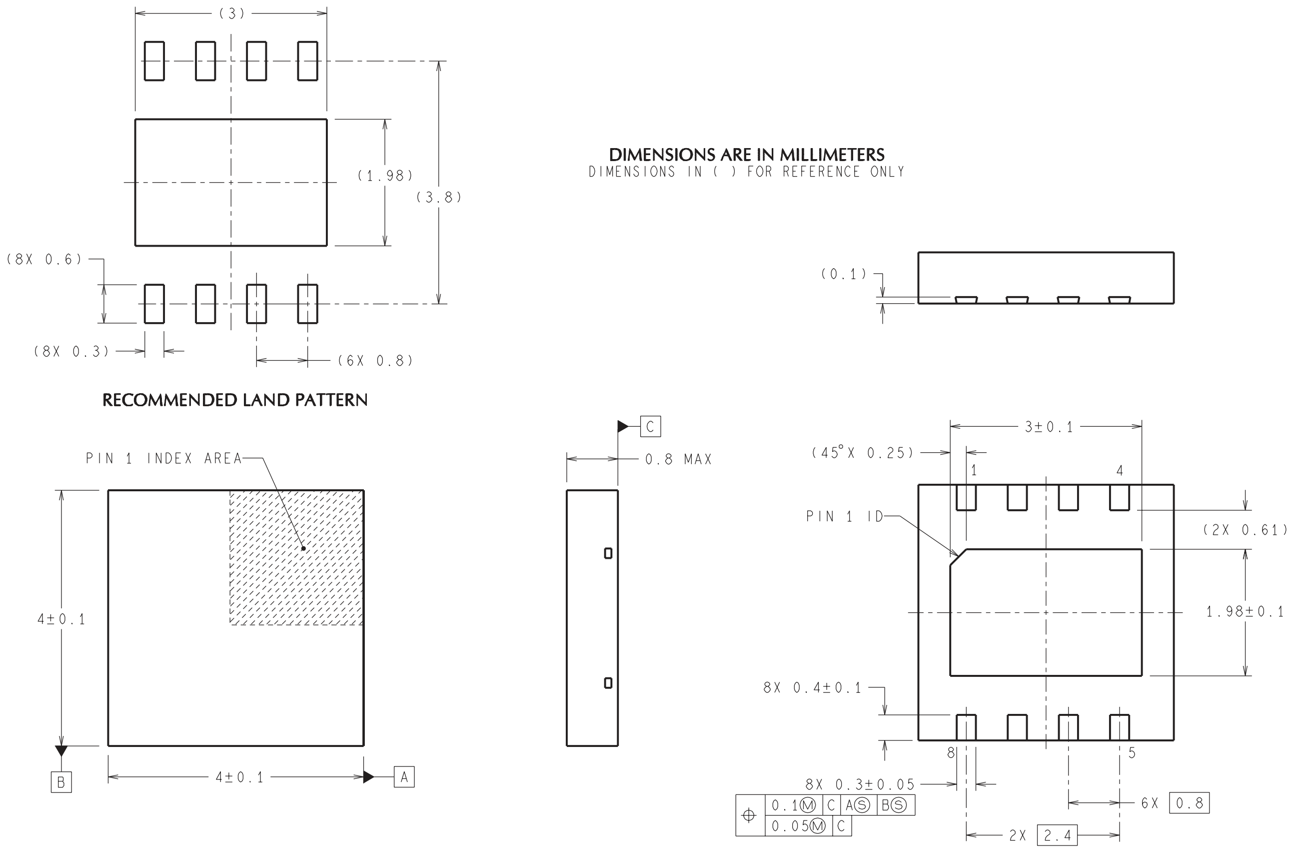
SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.03 X 3.80
0.125	2.71 X 3.40 (SHOWN)
0.150	2.47 X 3.10
0.175	2.29 X 2.87

4214849/A 08/2016

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.


(3)
(1.98)
(3.8)
(8X 0.6)
(8X 0.3)
(6X 0.8)
RECOMMENDED LAND PATTERN
DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY
(0.1)
PIN 1 INDEX AREA
4±0.1
B
4±0.1
A
C
0.8 MAX
3±0.1
(45°X 0.25)
1
4
PIN 1 ID
(2X 0.61)
1.98±0.1
8X 0.4±0.1
8
5
8X 0.3±0.05
0.1Ⓜ C AⓈ BⓈ
0.05Ⓜ C
6X 0.8
2X 2.4

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