

SN74ALVC16270

12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS

SCAS433A – OCTOBER 1993 – REVISED JULY 1995

- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Member of the Texas Instruments Widebus™ Family**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

description

The SN74ALVC16270 is a 12-bit to 24-bit registered bus exchanger, which is intended for use in applications where data must be transferred from a narrow high-speed bus to a wide lower-frequency bus. This device is designed specifically for low-voltage (3.3-V) V_{CC} operation.

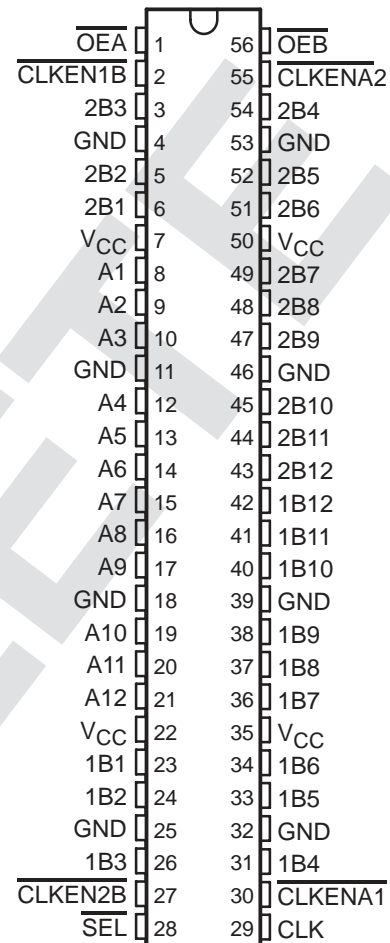
The device provides synchronous data exchange between the two ports. Data is stored in the internal registers on the low-to-high transition of the clock (CLK) input when the appropriate \overline{CLKEN} inputs are low. The select (\overline{SEL}) line selects 1B or 2B data for the A outputs. For data transfer in the A-to-B direction, a two-stage pipeline is provided in the A-to-1B path, with a single storage register in the A to 2B path. Proper control of the \overline{CLKENA} inputs allows two sequential 12-bit words to be presented synchronously as a 24-bit word on the B port. Data flow is controlled by the active-low output enables (\overline{OEA} , \overline{OEB}). The control terminals are registered to synchronize the bus direction changes with CLK.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVC16270 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16270 is characterized for operation from -40°C to 85°C .

DGG OR DL PACKAGE
(TOP VIEW)



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Function Tables

OUTPUT ENABLE

INPUTS			OUTPUTS	
CLK	\overline{OEA}	\overline{OEB}	A	1B, 2B
↑	H	H	Z	Z
↑	H	L	Z	Active
↑	L	H	Active	Z
↑	L	L	Active	Active

A-TO-B STORAGE ($\overline{OEB} = L$)

INPUTS				OUTPUTS	
$\overline{CLKENA1}$	$\overline{CLKENA2}$	CLK	A	1B	2B
L	H	↑	L	L [†]	2B ₀ [‡]
L	H	↑	H	H [†]	2B ₀ [‡]
L	L	↑	L	L [†]	L
L	L	↑	H	H [†]	H
H	L	↑	L	1B ₀ [‡]	L
H	L	↑	H	1B ₀ [‡]	H
H	H	X	X	1B ₀ [‡]	2B ₀ [‡]

[†] Two CLK edges are needed to propagate data.

[‡] Output level before the indicated steady-state input conditions were established

B-TO-A STORAGE ($\overline{OEA} = L$)

INPUTS						OUTPUT
$\overline{CLKEN1B}$	$\overline{CLKEN2B}$	CLK	\overline{SEL}	1B	2B	A
H	X	X	H	X	X	A ₀ [‡]
X	H	X	L	X	X	A ₀ [‡]
L	X	↑	H	L	X	L
L	X	↑	H	H	X	H
X	L	↑	L	X	L	L
X	L	↑	L	X	H	H

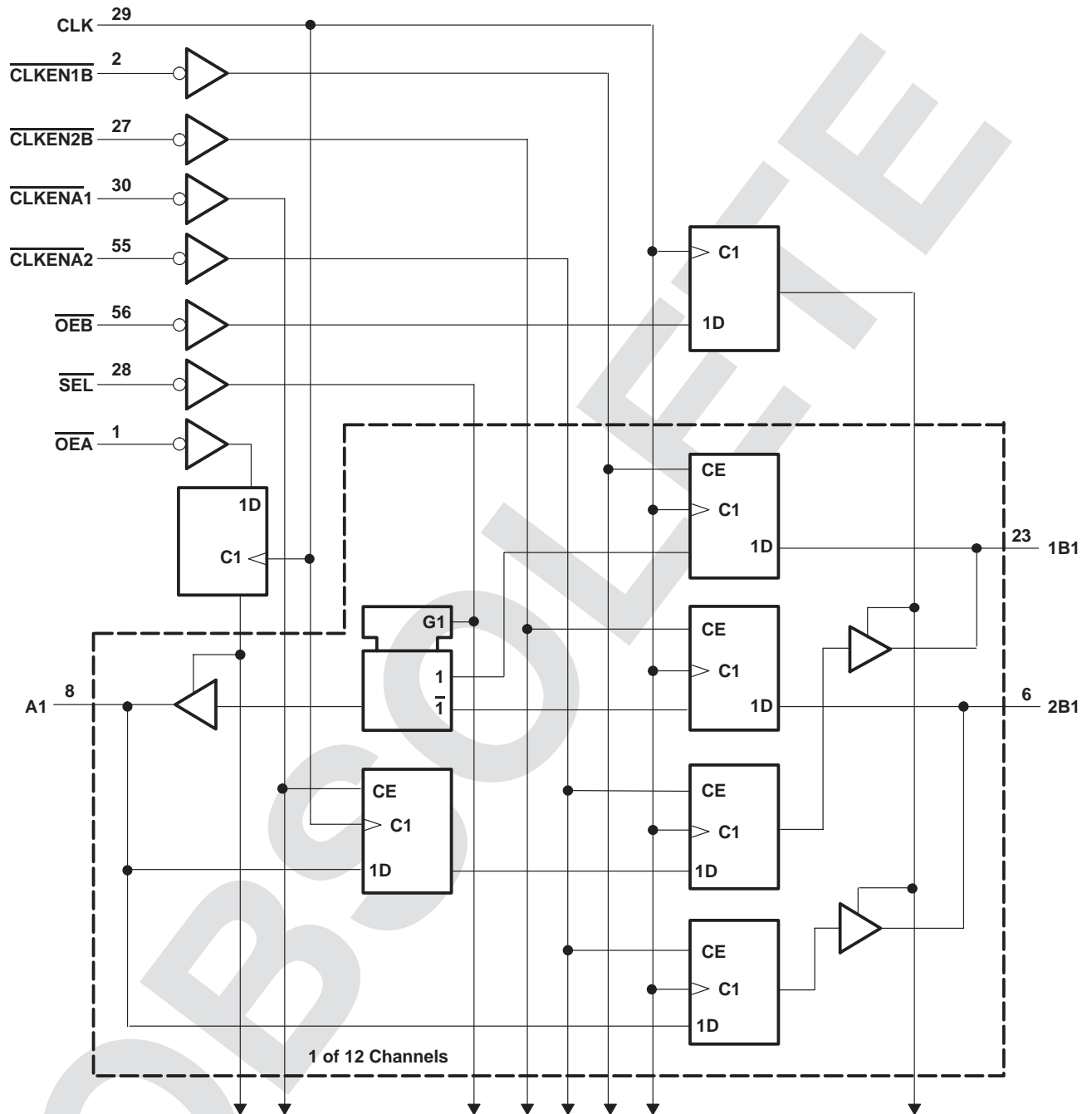
[‡] Output level before the indicated steady-state input conditions were established

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logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I : Except I/O ports (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
I/O ports (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND	± 100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3): DGG package	1 W
DL package	1.4 W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. The input and output positive-voltage ratings may be exceeded up to 4.6 V if the input and output clamp-current ratings are observed.
 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.3	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.3$ V to 2.7 V	1.7	V
		$V_{CC} = 2.7$ V to 3.6 V	2	
V_{IL}	Low-level input voltage	$V_{CC} = 2.3$ V to 2.7 V	0.7	V
		$V_{CC} = 2.7$ V to 3.6 V	0.8	
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.3$ V	-12	mA
		$V_{CC} = 2.7$ V	-12	
		$V_{CC} = 3$ V	-24	
I_{OL}	Low-level output current	$V_{CC} = 2.3$ V	12	mA
		$V_{CC} = 2.7$ V	12	
		$V_{CC} = 3$ V	24	
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_A	Operating free-air temperature	-40	85	$^\circ\text{C}$

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC} [†]	T _A = -40°C to 85°C			UNIT	
			MIN	TYP [‡]	MAX		
V _{OH}	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2			V	
	I _{OH} = -6 mA, V _{IH} = 1.7 V	2.3 V	2				
	I _{OH} = -12 mA	V _{IH} = 1.7 V	2.3 V	1.7			
		V _{IH} = 2 V	2.7 V	2.2			
		V _{IH} = 2 V	3 V	2.4			
I _{OH} = -24 mA, V _{IH} = 2 V	3 V	2					
V _{OL}	I _{OL} = 100 μA	MIN to MAX	0.2			V	
	I _{OL} = 6 mA, V _{IL} = 0.7 V	2.3 V	0.4				
	I _{OL} = 12 mA	V _{IL} = 0.7 V	2.3 V	0.7			
		V _{IL} = 0.8 V	2.7 V	0.4			
	I _{OL} = 24 mA, V _{IL} = 0.8 V	3 V	0.55				
I _I	V _I = V _{CC} or GND	3.6 V	±5			μA	
I _I (hold)	V _I = 0.7 V	2.3 V	45			μA	
	V _I = 1.7 V		-45				
	V _I = 0.8 V	3 V	75				
	V _I = 2 V		-75				
	V _I = 0 to 3.6 V	3.6 V	±500				
I _{OZ} [§]	V _O = V _{CC} or GND	3.6 V	±10			μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V	40			μA	
ΔI _{CC}	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V	750			μA	
C _i	Control inputs V _I = V _{CC} or GND	3.3 V	3.5			pF	
C _{io}	A or B ports V _O = V _{CC} or GND	3.3 V	9			pF	

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

[‡] All typical values are at V_{CC} = 3.3 V.

[§] For I/O ports, the parameter I_{OZ} includes the input leakage current.



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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT	
			MIN	MAX	MIN	MAX	MIN	MAX		
f _{clock}	Clock frequency		150		150		150		MHz	
t _w	Pulse duration, CLK high or low		3.3		3.3		3.3		ns	
t _{su}	Setup time	A data before CLK↑	High or low		4.1		3.8		3.1	
		B data before CLK↑	High or low		0.9		1.2		0.9	
		CLKENA1 or CLKENA2 before CLK↑	High or low		3.5		3.2		2.7	
		CLKEN1B or CLKEN2B before CLK↑	High or low		3.4		3		2.6	
		OE data before CLK↑	High or low		4.4		3.9		3.2	
t _h	Hold time	A data after CLK↑	High or low		0		0		0.2	
		B data after CLK↑	High or low		1.4		1		1.7	
		CLKENA1 or CLKENA2 after CLK↑	High or low		0		0.1		0.3	
		CLKEN1B or CLKEN2B after CLK↑	High or low		0		0		0.6	
		OE after CLK↑	High or low		0		0		0.1	

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	CLK	B	2	6.5	5.8		1.1	5.1	ns
	CLK	A	1.7	6	5.4		1	4.7	
	SEL	A	1.9	6.8	6.4		1	5.5	
t _{en}	CLK	A or B	1.6	7.5	6.8		1	6	ns
t _{dis}	CLK	A or B	2.6	7.4	6.5		1.1	5.8	ns



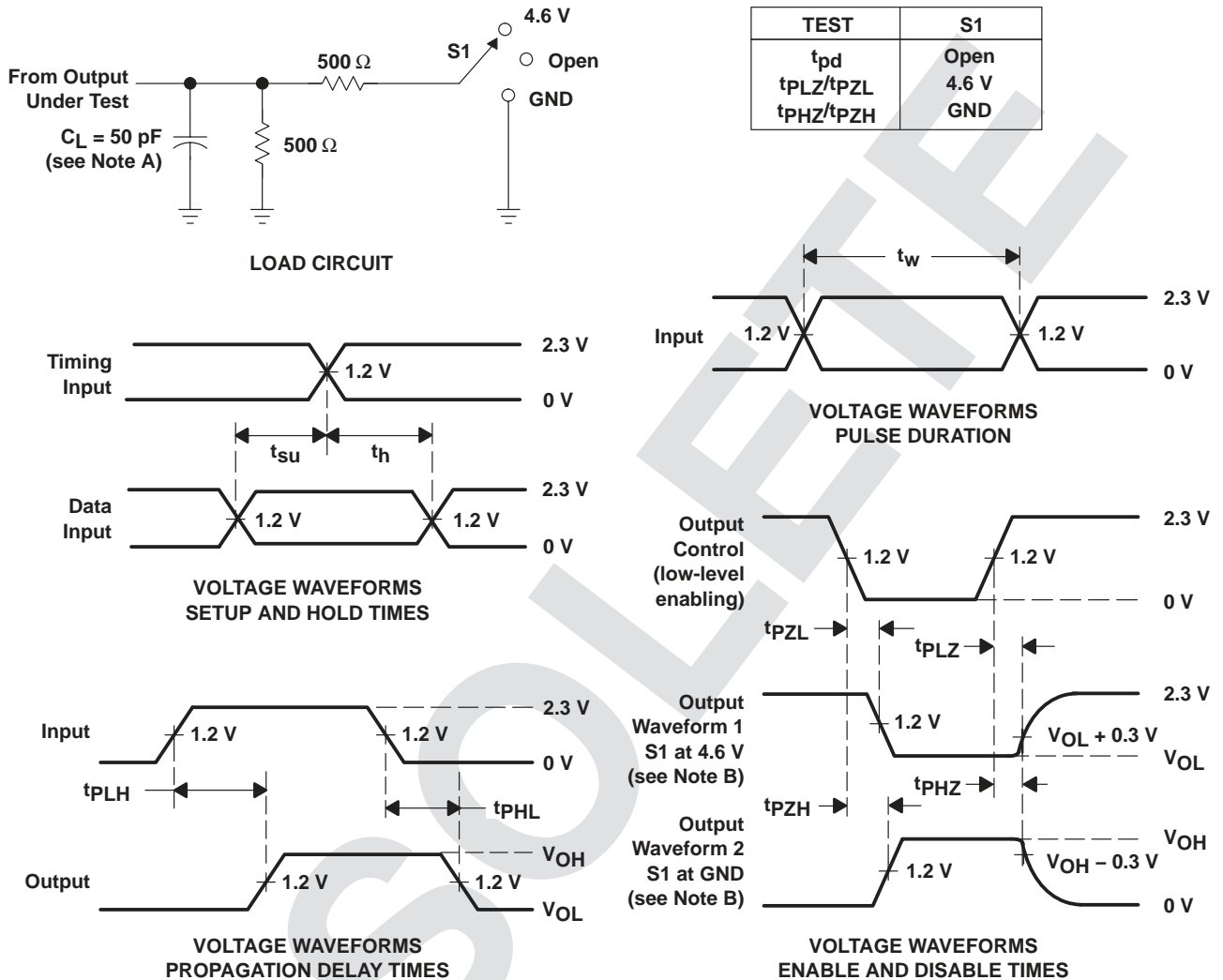
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PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PHL} and t_{PLH} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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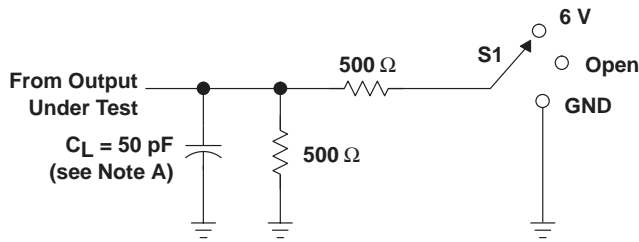
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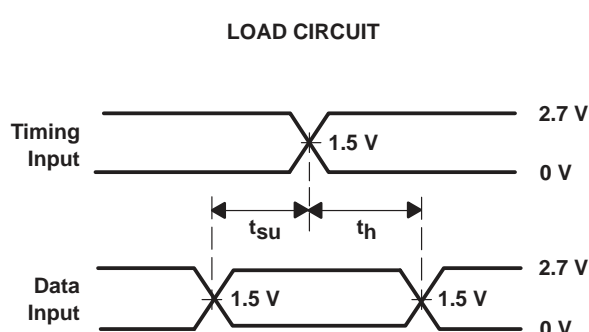
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$

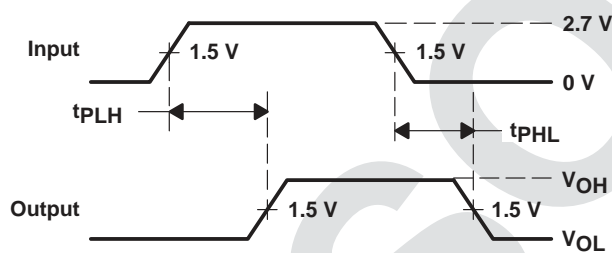


LOAD CIRCUIT

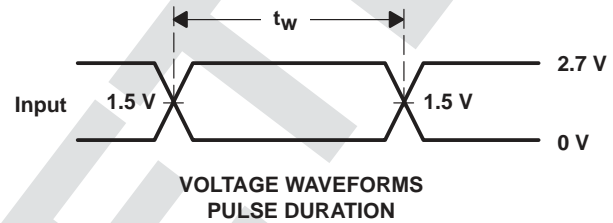
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



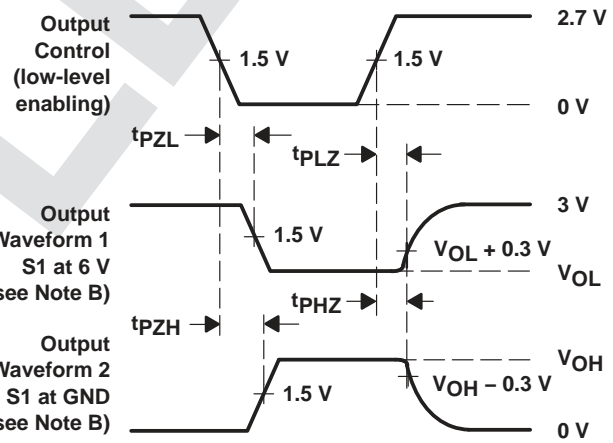
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PHL} and t_{PLH} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN74ALVC16270DL	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI	-40 to 85		
SN74ALVC16270DLR	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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