FAN7031

2W Stereo Power Amplifier with Four Selectable Gain Setting and Headphone Drive

Features

- 1.85W$_{RMS}$ and 2.45W$_{RMS}$ Power Per Each Channel Into 4Ω Load With Less Than 1% and 10% THD+N, Respectively
- Selectable Gain Via Internal Gain Control Circuit Which Eliminates External Gain Setting Resistors : 6dB, 10.3dB, 15.6dB, 21.6dB(Select)
- Low Quiescent Current : Typical 5.5mA@5V
- Low Shutdown Current : Typical 0.04μA@5V
- Fully Differential Input, Which Immunes the Common Mode Noise
- Stereo Headphone Drive
- Active Low Shutdown Logic
- Guaranteed Stability Under No Load Condition
- Thermally Enhanced Surface-Mount 20TSSOP-EP Package

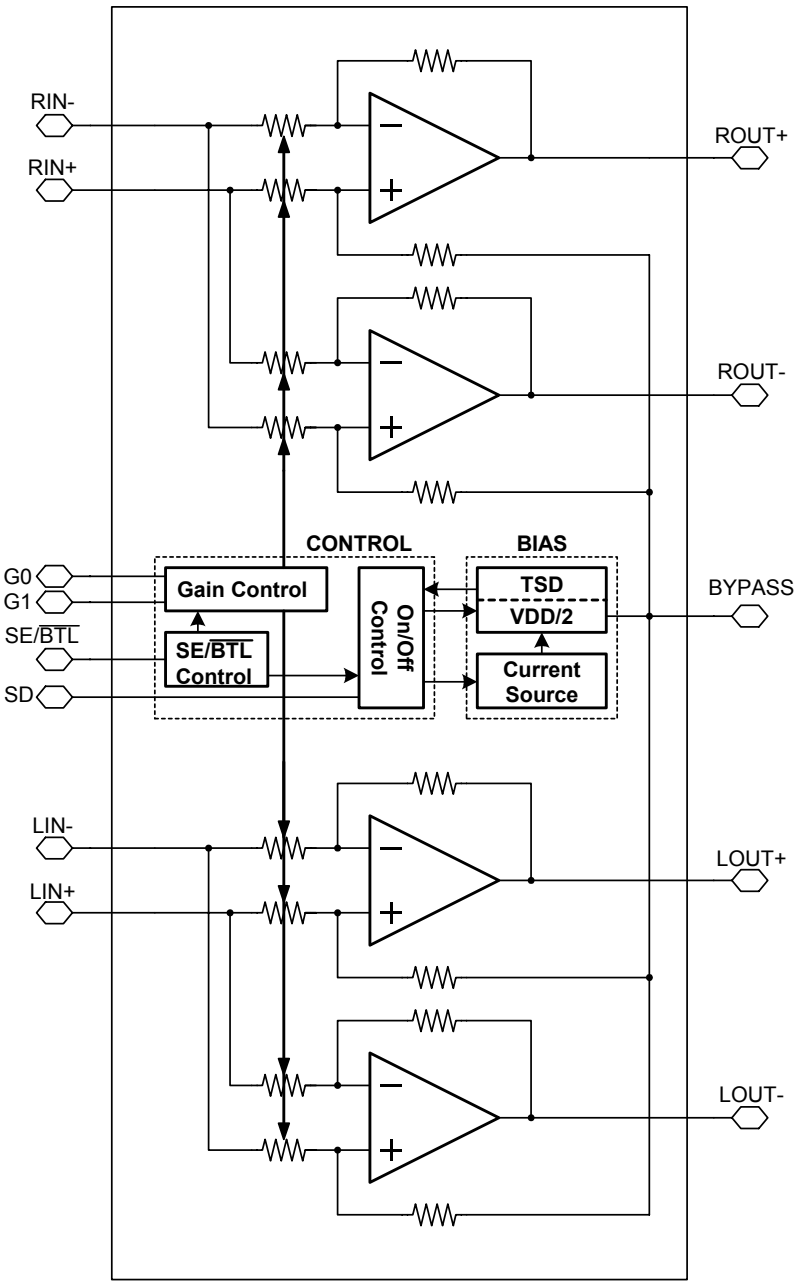
Description

The FAN7031 is a dual fully differential power amplifier in a 20-pin TSSOP-EP thermally enhanced package. When delivering 1.85W of continuous RMS power into 4Ω speaker at 5V supply, the FAN7031 has less than 1% of THD+N over the entire audible frequency range, 20Hz to 20kHz. To save power consumption in the portable applications, the FAN7031 provides shutdown function. Setting the shutdown pin to ground level, the FAN7031 falls into shutdown mode and consumes less than 4μA over all supply voltage range, 2.7V to 5.5V. Two gain setting pins(G0 and G1) control the gain of the FAN7031. The gain is selectable to 6dB, 10dB, 15.6dB and 21.6dB. The FAN7031 provides the single-ended(SE) operation by setting SE/$\overline{BTL}$ pin to above $V_{DD}/2$. Using SE/$\overline{BTL}$ pin and a mechanical switch which provides at the headphone jack, SE mode and BTL mode are automatically determined. Additional components such as resistors for gain setting and bootstrap capacitors are not needed, making the FAN7031 well suited for portable sound systems and other hand-held sound equipment. Target applications include notebook and desktop computers and portable audio equipment.

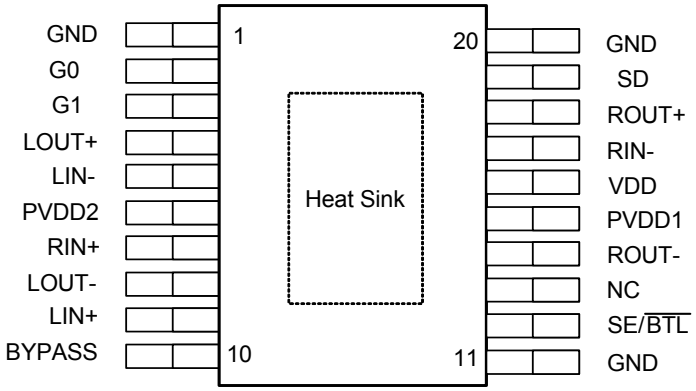
20-TSSOP-EP

Rev. 1.0.3

Internal Block Diagram



Pin Assignments



Pin Description

Pin No	Symbol	I/O	Decription
1*	GND	-	Ground
2	G0	I	Gain Selection Input(MSB)
3	G1	I	Gain Selection Input(LSB)
4	LOUT+	O	Left Channel (+) Output
5	LIN-	I	Left Channel (-) Input
6**	PVDD2	I	Left Channel Power Supply Voltage
7	RIN+	I	Right Channel (+) Input
8	LOUT-	O	Left Channel (-) Output
9	LIN+	I	Left Channel (+) Input
10	BYPASS	O	Bypass Capacitor Connect
11*	GND	-	Ground
12	SE/$\overline{\text{BTL}}$	I	Single-Ended & BTL Selection: GND ≤ SE/$\overline{\text{BTL}}$ ≤ VDD/2:BTL Mode VDD/2 < SE/$\overline{\text{BTL}}$ ≤ VDD: SE Mode
13	NC	-	No Connection
14	ROUT-	O	Right Channel (-) Output
15**	PVDD1	I	Right Channel Power Supply Voltage
16**	VDD	I	Power Supply Voltage
17	RIN-	I	Right Channel (-) Input
18	ROUT+	O	Right Channel (+) Output
19	SD	I	Shutdown Logic Low SD=VDD: Chip Enable SD=GND: Chip Shutdown
20*	GND	-	Ground

* All GND is internally tied together.
** For the best performance, VDD, PVDD1 and PVDD2 must be the same voltage level(strongly recommend).

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Remark
Maximum Supply Voltage	VDDmax	6.0V	V	
Power Dissipation	P_D	Internally Limited	W	See Derating Curve
Operating Temperature	T_{OPG}	-40 ~ +85	°C	
Storage Temperature	T_{STG}	-65 ~ +150	°C	
Junction Temperature	T_J	150	°C	
Thermal Resistance (Junction to Ambient)	Rthja	30.4	°C/W	Multi Layer Board
		112.5		Single Layer Board
ESD Rating (Human Body Model)		2000	V	

Note1 : Rthja was derived using a JEDEC multi layer and single layer.

Operating Ratings

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{DD}	2.7	-	5.5	V

Electrical Characteristics

(V_{DD} = 5.0V, Ta = 25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Offset Voltage	V_{OFF}	RL=4Ω, Av=6dB	-25	-	25	mV
Supply Current	I_{DD}	No Input, No Load	-	5.5	10	mA
Shutdown Current	I_{SD}	SD = GND	-	0.04	4	μA
Output Power	P_O	THD+N =1%, RL = 4Ω, f = 1kHz	-	1.85	-	W
		THD+N =10%, RL = 4Ω, f = 1kHz	-	2.45	-	W
BTL Mode Gain	Av	SE/$\overline{BTL}$=GND, G0=GND, G1=GND, Vin=4Vpp, No Load	-	6	-	dB
		SE/$\overline{BTL}$=GND, G0=GND, G1=VDD, Vin=2.44Vpp, No Load	-	10.3	-	dB
		SE/$\overline{BTL}$=GND, G0=VDD, G1=GND, Vin=1.34Vpp, No Load	-	15.6	-	dB
		SE/$\overline{BTL}$=GND, G0=VDD, G1=VDD, Vin=0.66Vpp, No Load	-	21.3	-	dB
SE Mode Gain		SE/$\overline{BTL}$=VDD, Vin=2.44Vpp, No Load	-	4.3	-	dB
Total Harmonic Distortion + Noise	THD+N	P_O = 1W, RL=4Ω, f = 20kHz	-	0.2	0.75	%
Power Supply Rejection Ratio	PSRR	C_{byp} = 0.47μF, RL=4Ω, BTL Mode, ΔVDD=500mVpp, f = 1kHz	40	70	-	dB

Electrical Characteristics (Continued)

(V_{DD} = 3.3 V, Ta = 25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Offset Voltage	V_{OFF}	RL=4Ω, Av=6dB	-25	-	25	mV
Supply Current	I_{DD}	No Input, No Load	-	4.3	8	mA
Shutdown Current	I_{SD}	SD = GND	-	0.08	4	μA
Output Power	P_O	THD+N =10%, RL = 4Ω, f=1kHz	-	1.02	-	W
Total Harmonic Distortion + Noise	THD+N	P_O = 0.5W, RL = 4Ω, f = 20kHz	-	0.2	0.75	%
Power Supply Rejection Ratio	PSRR	C_{byp} = 0.47μF, RL=4Ω, BTL Mode, ΔVDD=330mVpp, f = 1kHz	40	70	-	dB

Electrical Characteristics (Continued)

(V_{DD} = 2.7 V, Ta = 25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Offset Voltage	V_{OFF}	RL=4Ω, Av=6dB	-25	-	25	mV
Supply Current	I_{DD}	No Input, No Load	-	4.1	7	mA
Shutdown Current	I_{SD}	SD = GND	-	0.04	4	μA
Output Power	P_O	THD+N =10%, RL = 4Ω, f=1kHz	-	0.54	-	W
Total Harmonic Distortion + Noise	THD+N	P_O = 0.25W, RL = 4Ω, f = 20kHz	-	0.2	0.75	%
Power Supply Rejection Ratio	PSRR	C_{byp} = 0.47μF, RL=4Ω, BTL Mode, ΔVDD=270mVpp, f = 1kHz	-	65	-	dB

Performance Characteristics

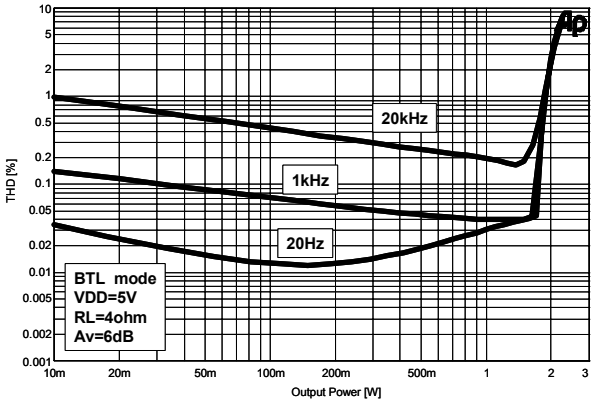


Figure 1. THD+N vs. Output Power

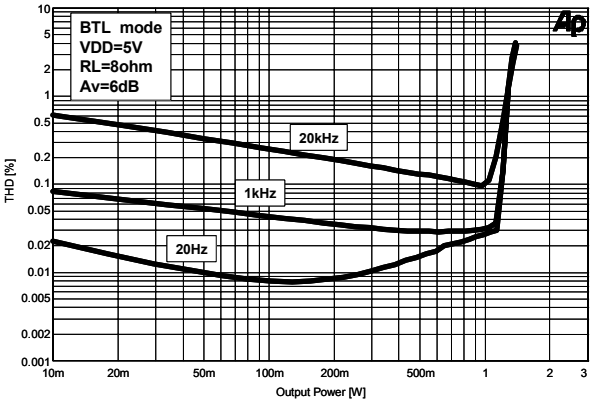


Figure 2. THD+N vs. Output Power

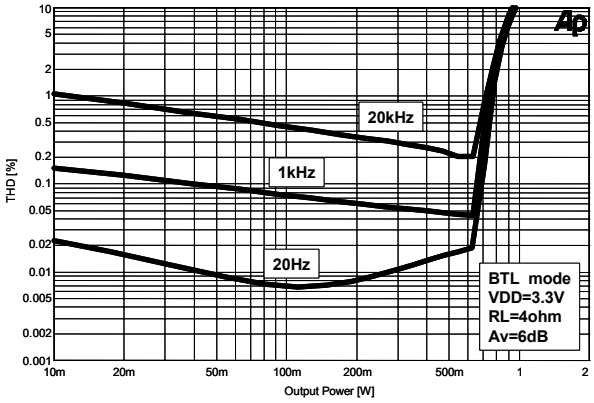


Figure 3. THD+N vs. Output Power

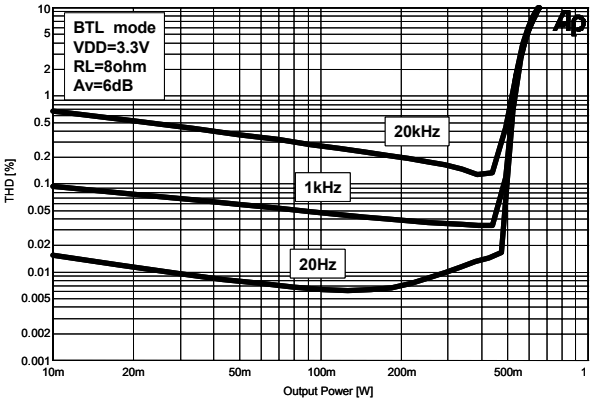


Figure 4. THD+N vs. Output Power

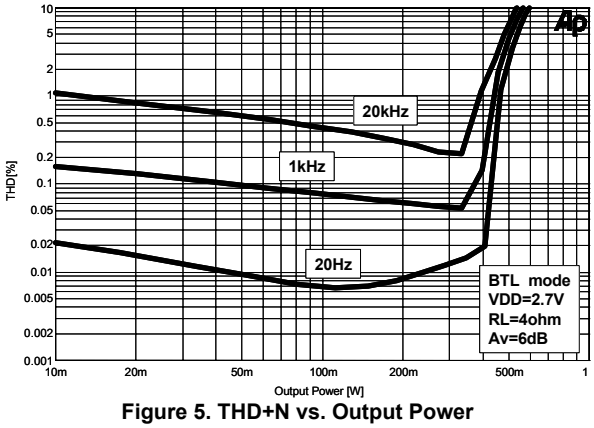


Figure 5. THD+N vs. Output Power

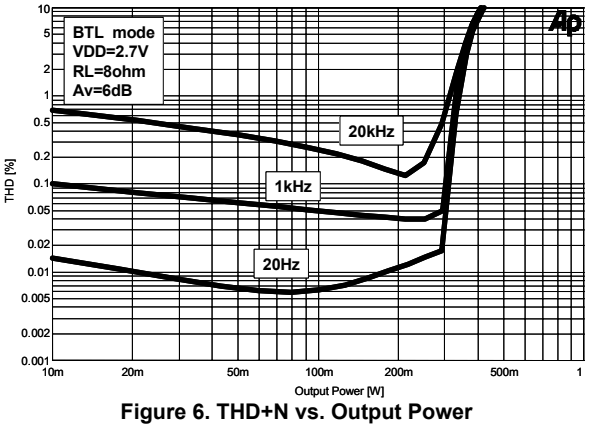


Figure 6. THD+N vs. Output Power

Performance Characteristics(Continued)

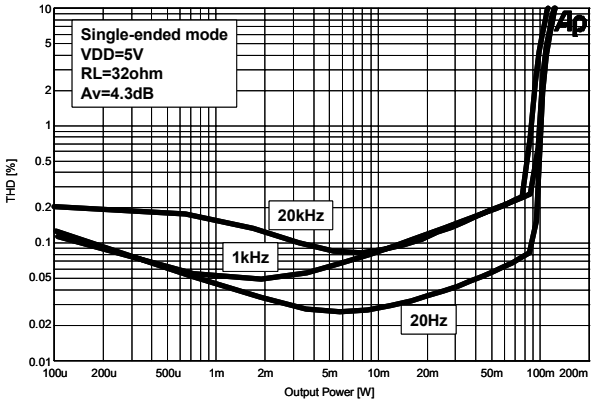


Figure 7. THD+N vs. Output Power

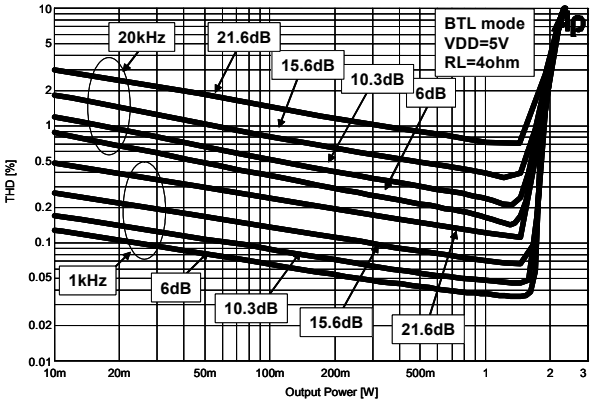


Figure 8. THD+N vs. Gain

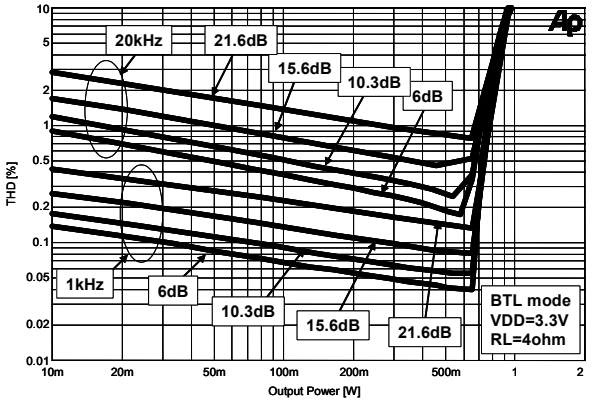


Figure 9. THD+N vs. Gain

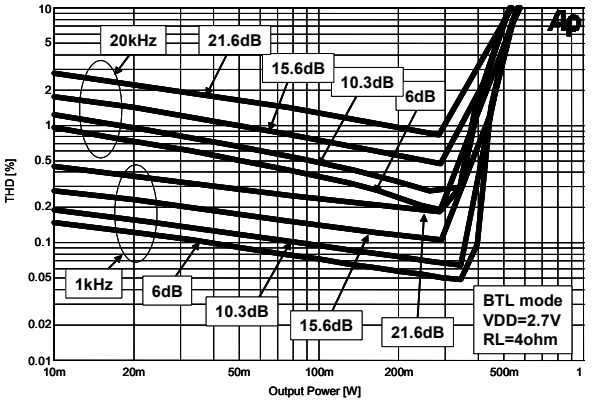


Figure 10. THD+N vs. Gain

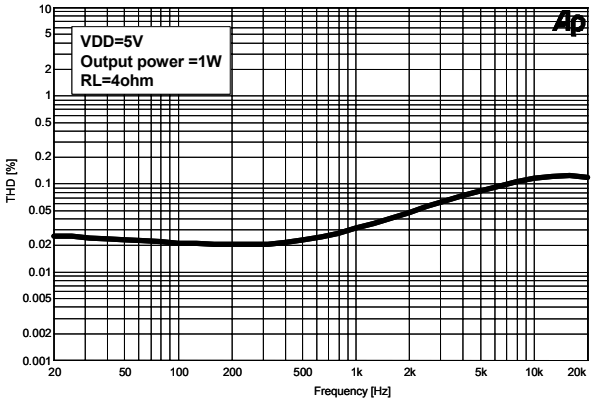


Figure 11. THD+N vs. Frequency

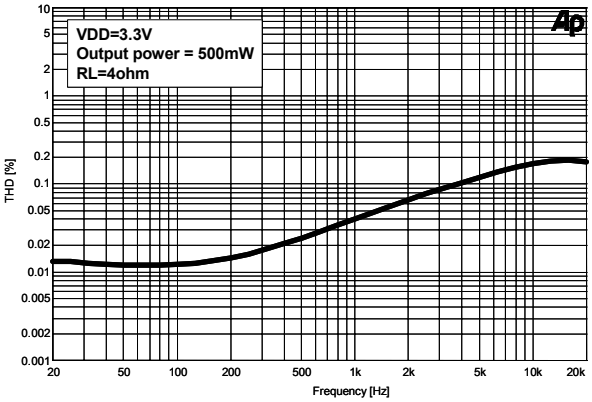


Figure 12. THD+N vs. Frequency

Performance Characteristics(Continued)

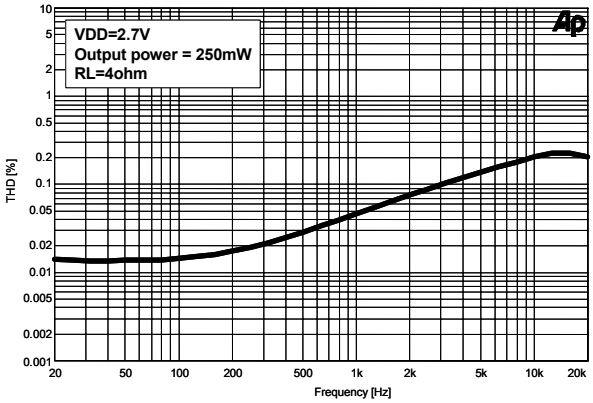


Figure 13. THD+N vs. Frequency

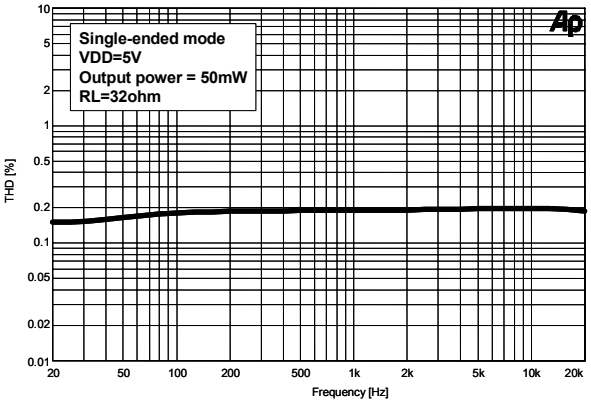


Figure 14. THD+N vs. Frequency

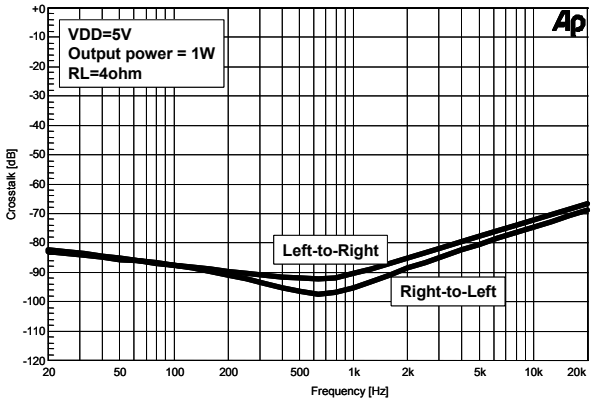


Figure 15. Crosstalk vs. Frequency

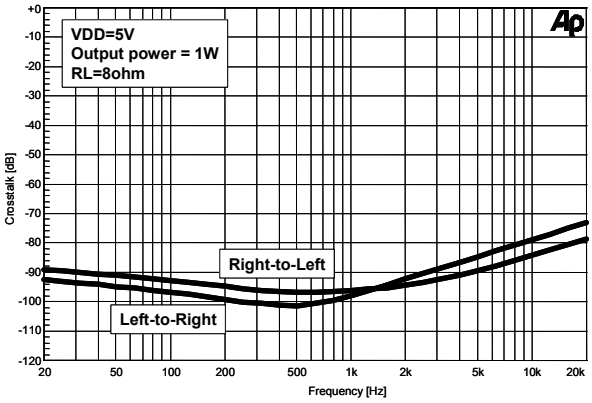


Figure 16. Crosstalk vs. Frequency

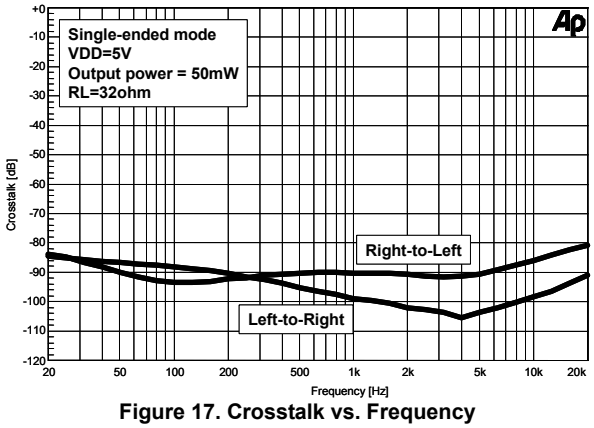


Figure 17. Crosstalk vs. Frequency

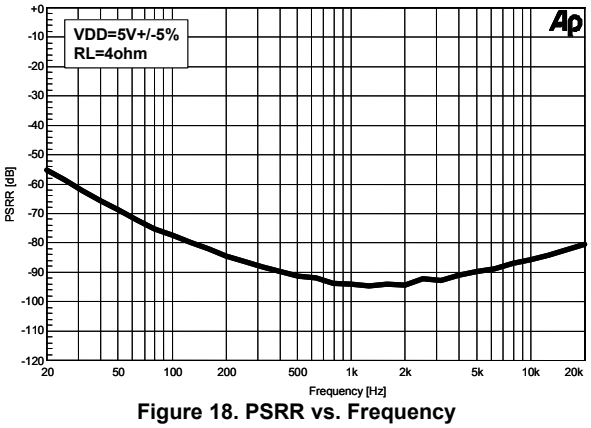


Figure 18. PSRR vs. Frequency

Performance Characteristics(Continued)

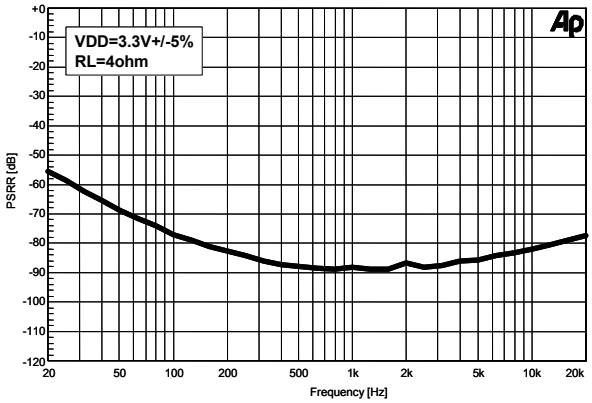


Figure 19. PSRR vs. Frequency

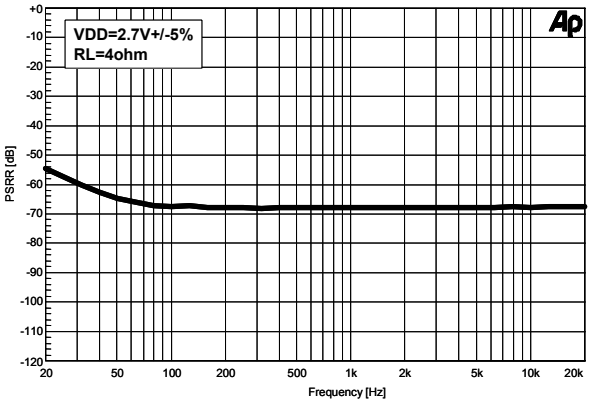


Figure 20. PSRR vs. Frequency

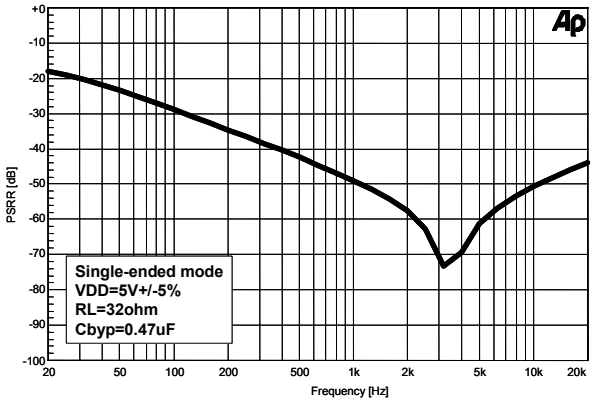


Figure 21. PSRR vs. Frequency

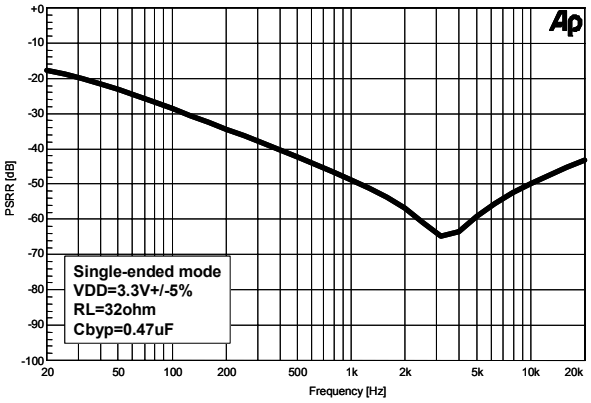


Figure 22. PSRR vs. Frequency

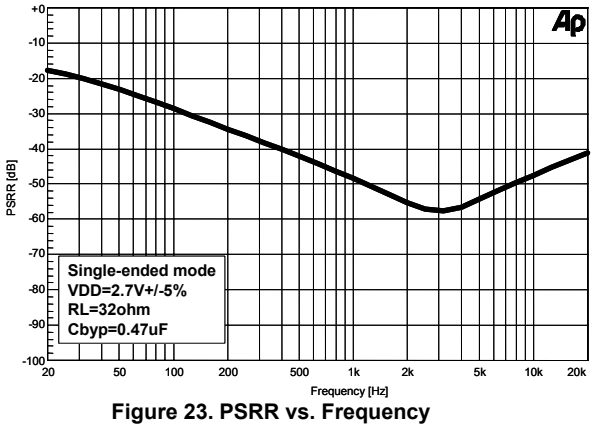


Figure 23. PSRR vs. Frequency

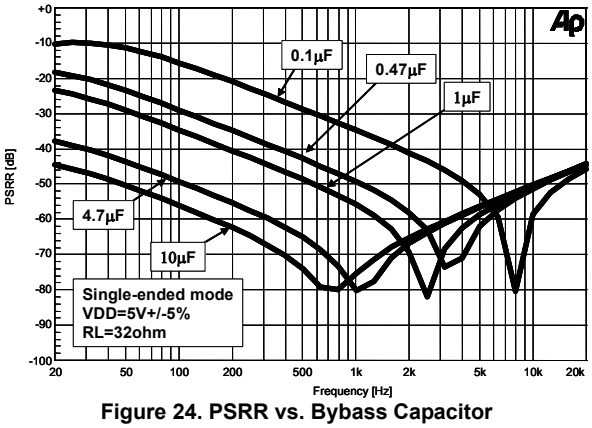


Figure 24. PSRR vs. Bybass Capacitor

Performance Characteristics(Continued)

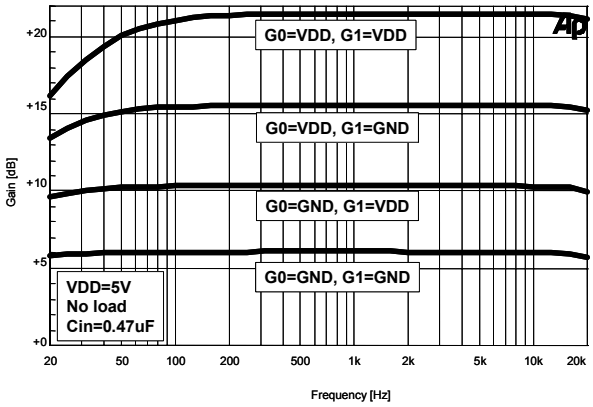


Figure 25. BTL Mode Gain vs. Frequency

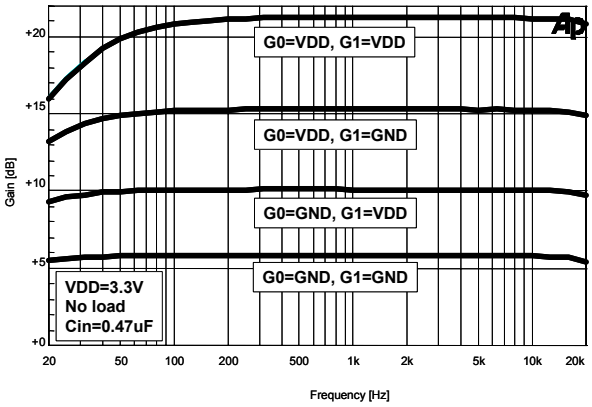


Figure 26. BTL Mode Gain vs. Frequency

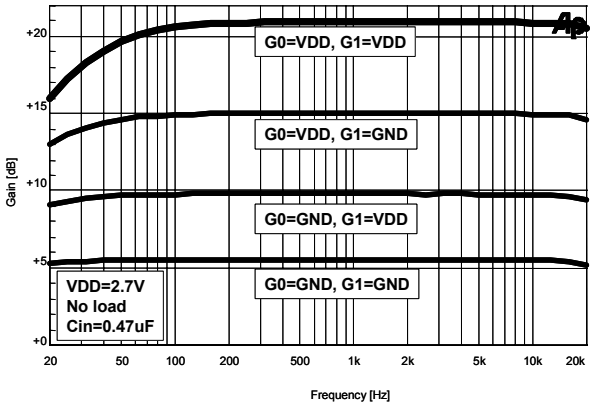


Figure 27. BTL Mode Gain vs. Frequency

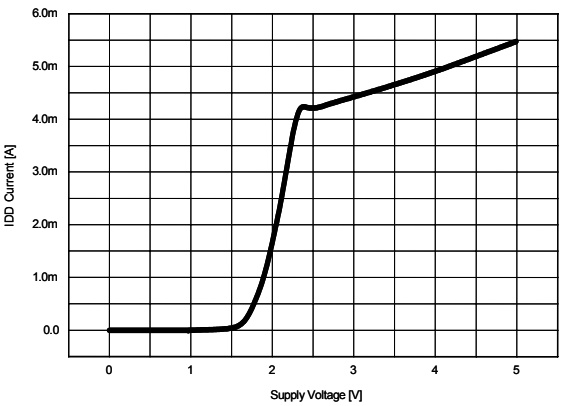


Figure 28. IDD vs. Supply Voltage

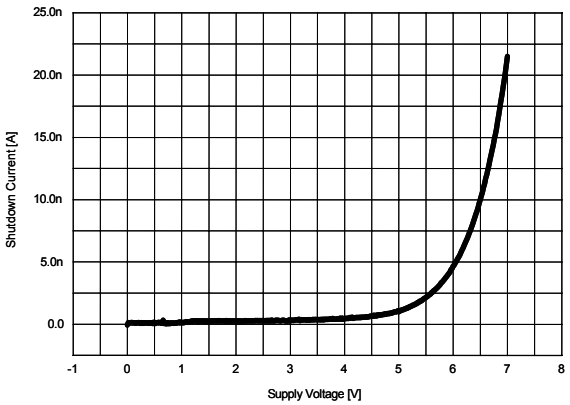


Figure 29. Shutdown Current vs. Supply Voltage

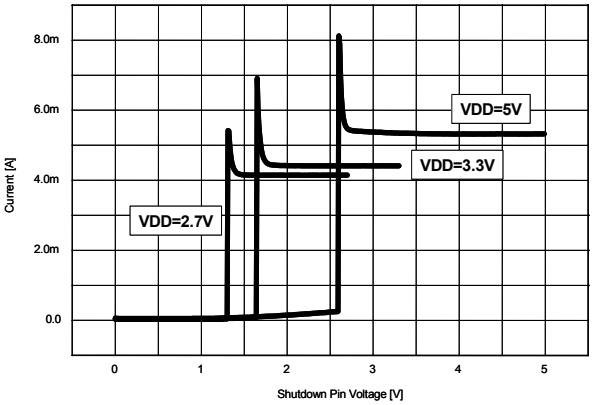


Figure 30. IDD vs. Shutdown Pin Voltage

Performance Characteristics(Continued)

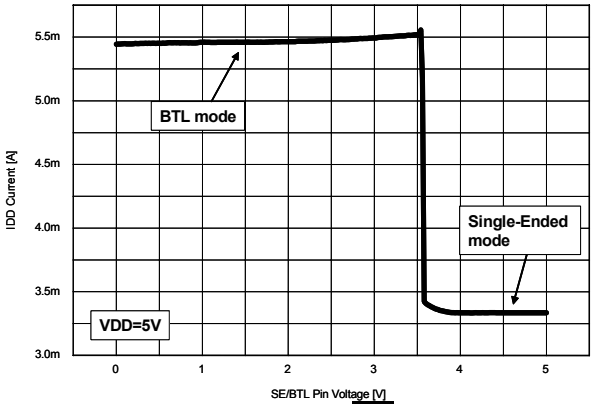


Figure 31. IDD vs. SE/BTL Pin Voltage

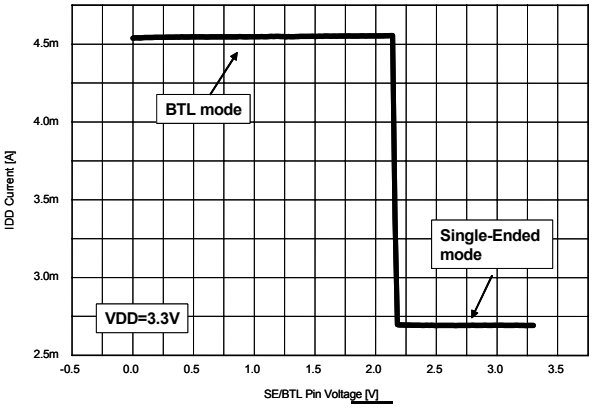


Figure 32. IDD vs. SE/BTL Pin Voltage

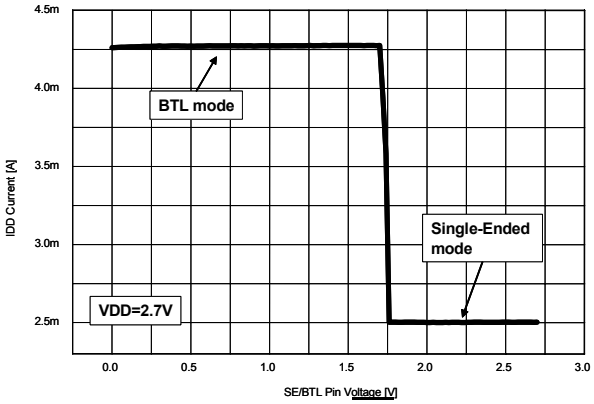


Figure 33. IDD vs. SE/BTL Pin Voltage

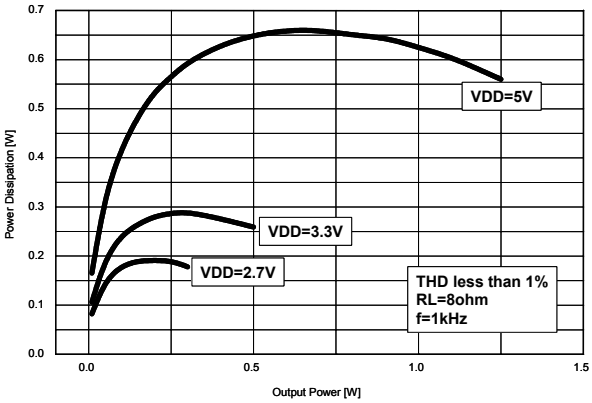


Figure 34. Power Dissipation vs. Output Power

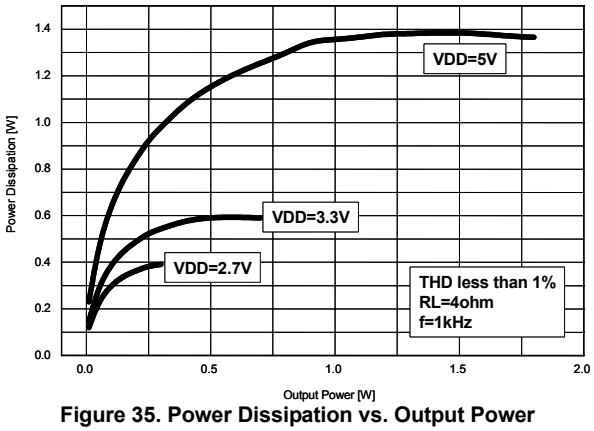


Figure 35. Power Dissipation vs. Output Power

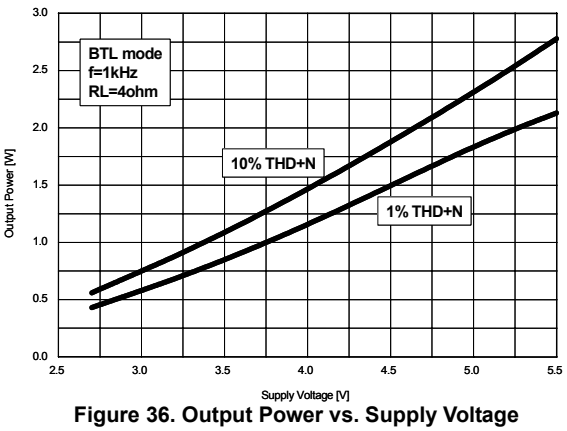


Figure 36. Output Power vs. Supply Voltage

Performance Characteristics(Continued)

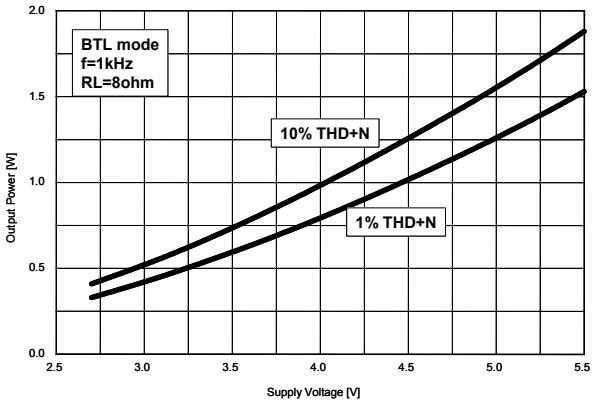


Figure 37. Output Power vs. Supply Voltage

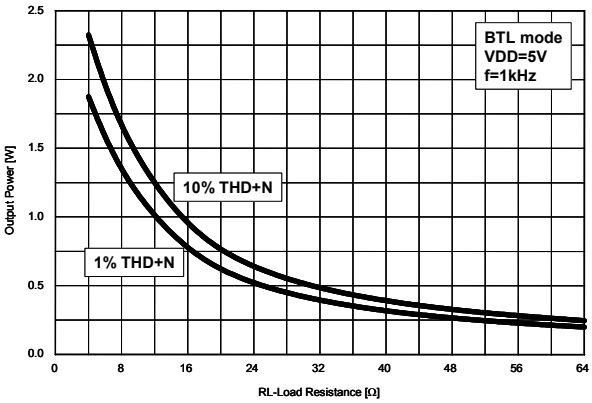


Figure 38. Output Power vs. Load Resistance

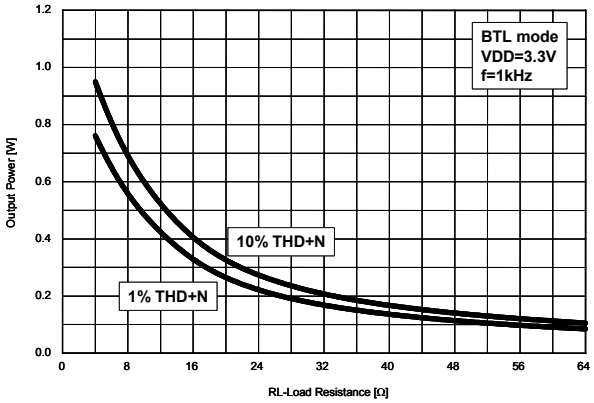


Figure 39. Output Power vs. Load Resistance

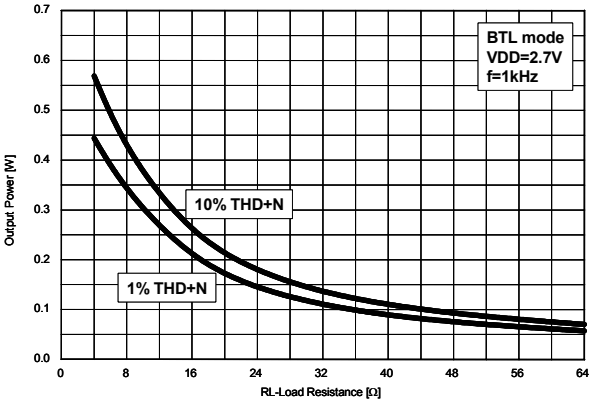


Figure 40. Output Power vs. Load Resistance

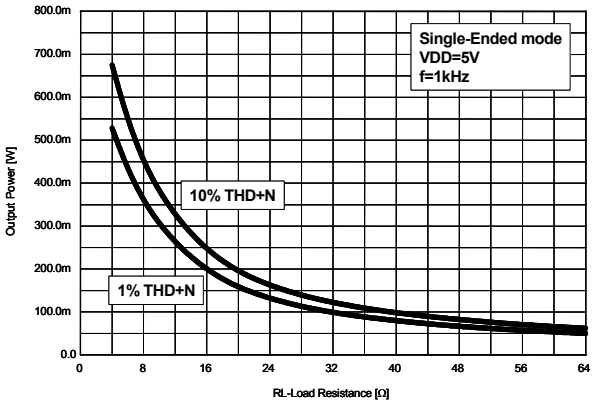


Figure 41. Output Power vs. Load Resistance

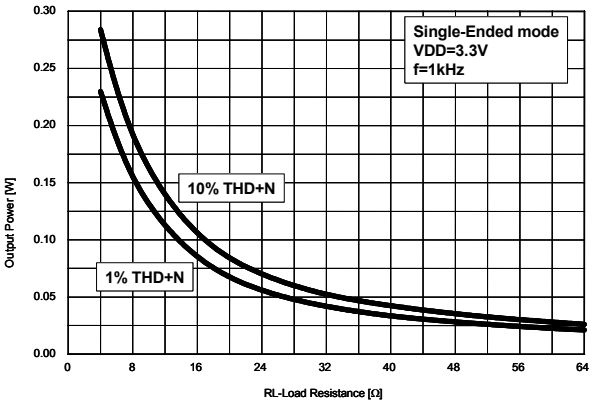


Figure 42. Output Power vs. Load Resistance

Performance Characteristics(Continued)

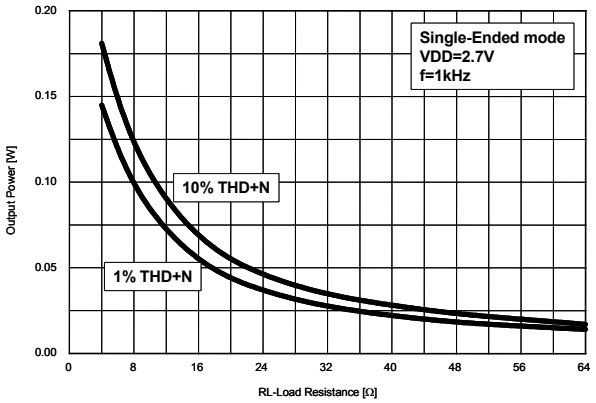


Figure 43. Output Power vs. Load Resistance

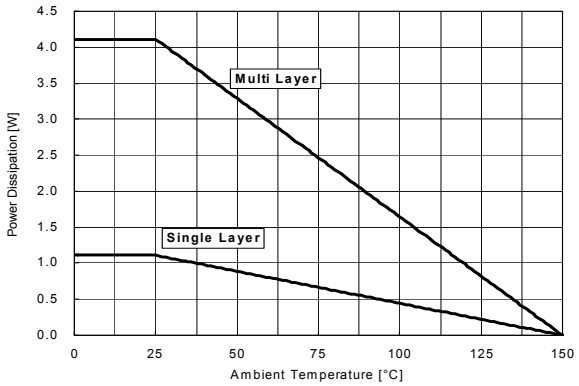
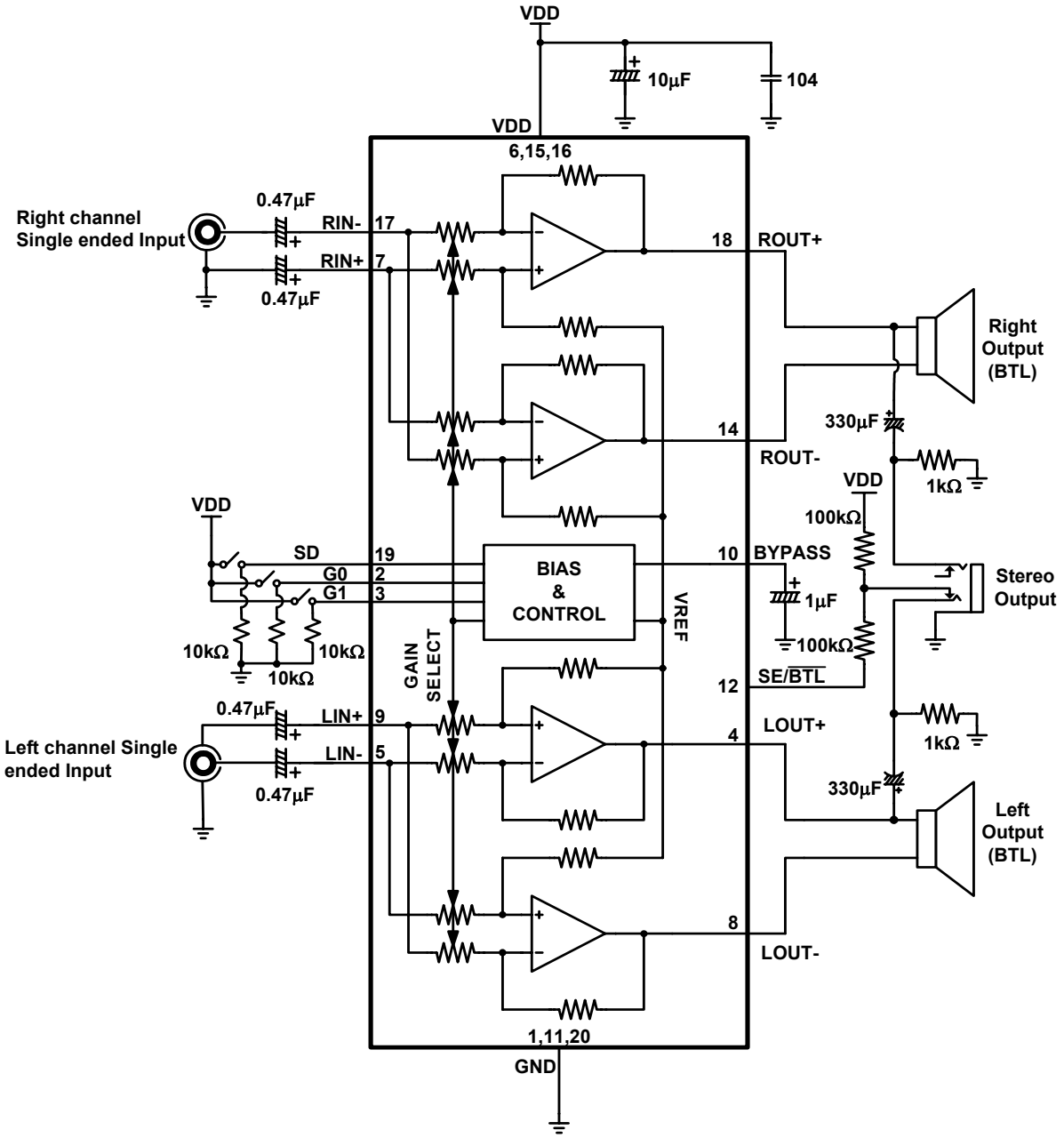


Figure 44. Power Derating Curve

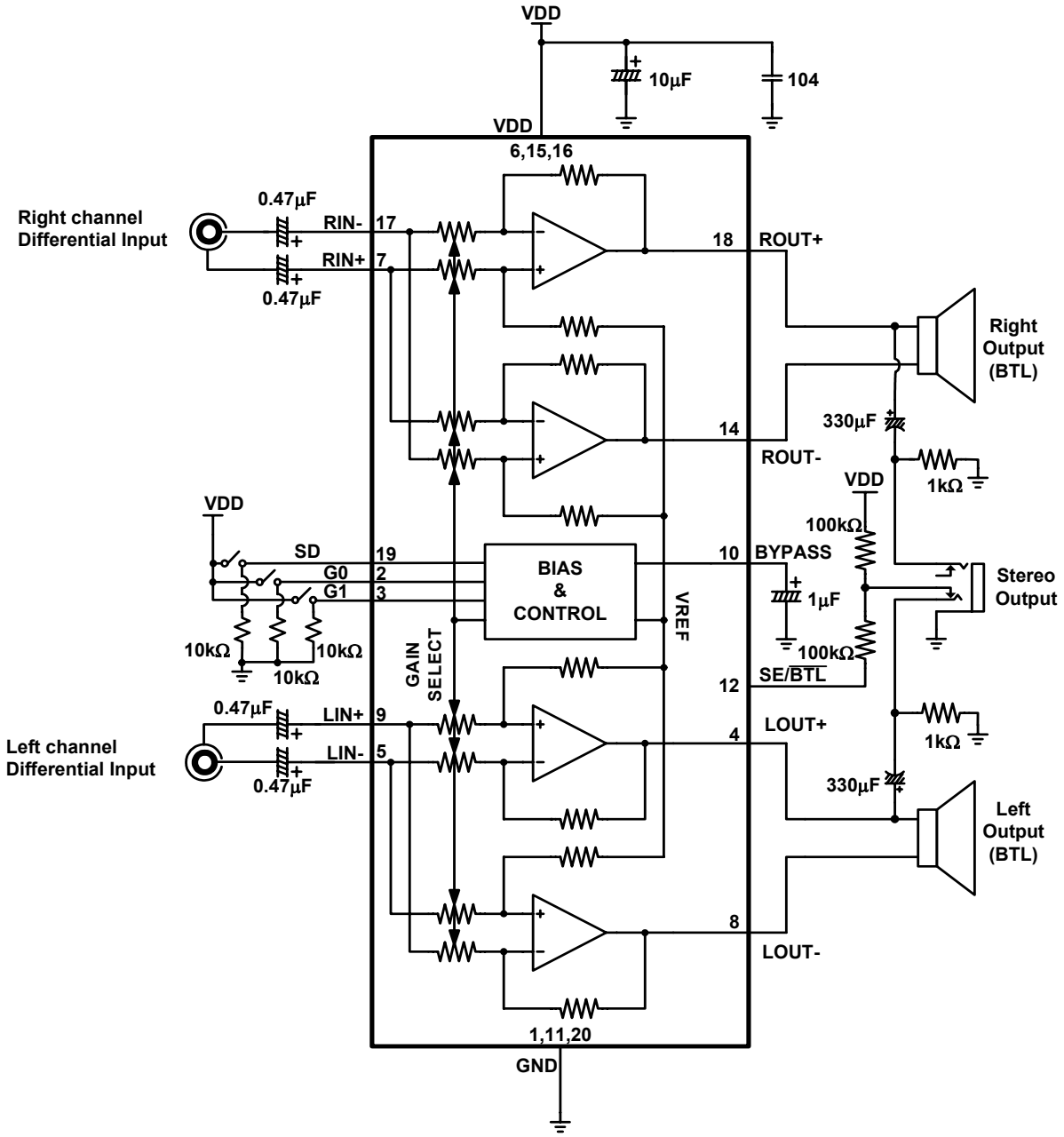
Typical Application Circuits

Single-Ended Inputs



Typical Application Circuits(Continued)

Differential Inputs



Functional Description

The FAN7031 is a stereo 2W amplifier capable of delivering 1.85W continuous RMS power into a 4-ohm load. This device has less than 0.75% THD+N across the entire frequency range at an output power of 1W. A thermally enhanced TSSOP package is used to allow for maximum dissipation of package heat.
Gain selection is achieved by driving G0 and G1 inputs according to the table below.

G0	G1	SE/$\overline{BTL}$	Av	Zin
0	0	0	6dB	90kΩ
0	1	0	10.3dB	55kΩ
1	0	0	15.6dB	30kΩ
1	1	0	21.6dB	15kΩ
X	X	1	4.3dB	55kΩ

Gain select pins are activated only when SE/$\overline{BTL}$ pin is set to low level. If SE/$\overline{BTL}$ pin is high, the amplifier configuration is changed as SE(single-ended) mode and the gain of SE amplifier is fixed to 4.3dB (about 1.64).

Gain is varied by changing the taps on input resistors, and such change in gain will cause variation in the input impedance. Input impedance (Zin) is described in the above table. The impedance variation determines amplifier lowest bandwidth. Thus, input DC decoupling capacitors must be carefully selected.

Applications Information

PCB Layout and Supply Regulation

Metal trace resistance between the BTL output and the parasitic resistance of the power supply line both heavily affect the output power. In order to obtain the maximum power depicted in the performance characteristics figures, outputs, power and ground lines need wide metal trace. The parasitic resistance of the power line increases ripple noise and degrades the THD and PSRR performance. To reduce such unwanted effect, large capacitor must be connected between V_{DD} pin and GND pin as close as possible. To improve power supply regulation performance, use a low ESR capacitor.

Power Supply Bypassing

Selection of proper power supply bypassing capacitor is critical to obtaining lower noise as well as higher power supply rejection. Larger capacitors may help to increase immunity to the supply noise. However, considering economical design, attaching 10μF electrolytic capacitor or tantalum capacitor with 0.1μF ceramic capacitor as close as possible to the VDD pins are enough to get a good supply noise rejection.

Selection of Input Capacitor

Input capacitor blocks DC signal also low frequency input signal. Thus, this capacitor acts as a high pass filter. The -3dB frequency of this filter is determined by input capacitor and input impedance of the amplifier. The frequency is

$$f_{-3dB} = \frac{1}{2\pi \cdot Zin \cdot C}$$

As shown previously, the input impedance is changed by selecting gain. Considering smallest Zin (=15kW), the capacitance which meets f_{-3dB} frequency of 20Hz is 0.53uF. Thus, selecting the capacitance higher than 0.53uF, the lowest frequency of audio signal can be amplified without gain loss.

BLT Mode of Operation vs. Single Ended Mode of Operation

The FAN7031 offers both BTL (Bridge-Tied Load) and SE (Single Ended) operation. When SE/$\overline{BTL}$ pin is low, BTL operation is selected. In BTL operation, maximum output power is increased 4 times comparing with SE operation at the same load, output swing and supply condition because output swing is doubled. Thus, BTL mode is useful to drive a speaker load. On the other hand, when SE/$\overline{BTL}$ pin is high, one amplifier configured BTL driver is turned off and only single amplifier is activated. In this mode, maximum output power is reduced and the quiescent power consumption is saved about half. Thus, SE mode is adequate for head-phone load. The output power of BTL and SE are expressed as follows respectively:

$$P_{BTL} = \frac{Vp^2}{2 \cdot RL},$$

$$P_{SE} = \frac{Vp^2}{8 \cdot RL}.$$

To use the amplifier in SE mode, the output DC voltage must be blocked not to increase power consumption. Thus, the load is tied to output via output DC blocking capacitor. The capacitor size can be chosen using above f_{-3dB} equation. For example, assuming the load impedance is 32W, 249uF capacitor guarantees 20Hz signal transmission to the load without gain reduction.

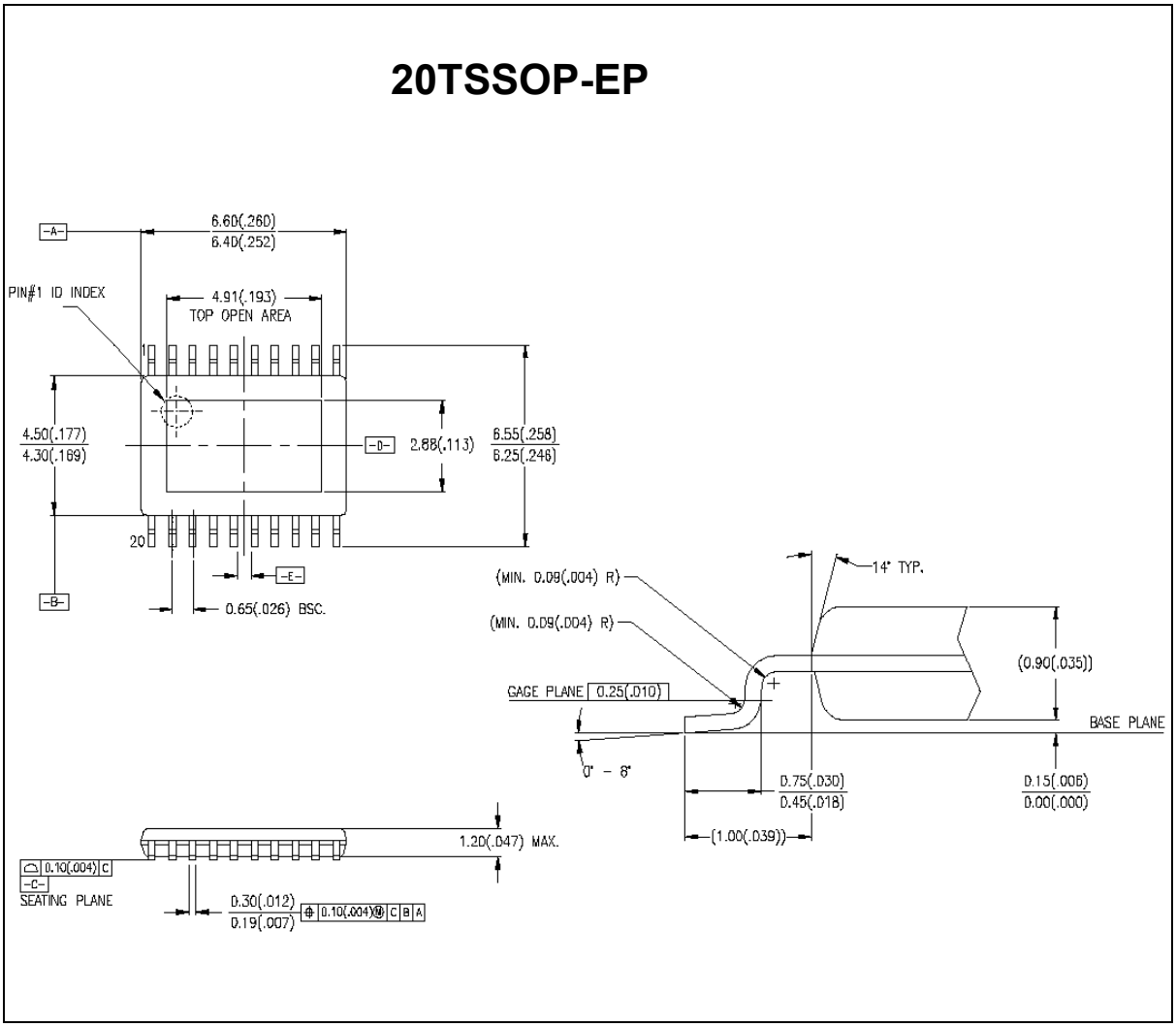
Shutdown Mode

The device moves to a shutdown mode when the shutdown pin is at 0V. For normal operation the shutdown pin should be at V_{DD}. This pin should never be left unconnected.

Mechanical Dimensions

Package

Dimensions in millimeters



Ordering Information

Device	Package	Operating Temperature
FAN7031MTF	20TSSOP-EP	-40°C ~ +85°C