MP6922

Dual Fast Turn-off Intelligent Controller

The Future of Analog IC Technology

DESCRIPTION

The MP6922 is a dual fast turn-off intelligent controller to drive two N-CH power MOSFETs in LLC resonant converters for synchronous rectification.

The IC regulates the forward voltage drop of the power switch to about 70mV and turns it off before the voltage goes negative.

MP6922 has a light-load function to latch-off the gate driver at light load condition, during which only about 600μA quiescent current is consumed.

The fast turn-off speed of MP6922 makes both CCM and DCM driving available. An internal Reverse Current Protection (RCP) function ensures safe operation of the MOSFETs in high frequency CCM condition.

MP6922 requires a minimum number of readily available standard external components and is available in SOIC8E, SOIC8 or SOIC14 package.

FEATURES

- Works with both Standard and Logic Level FETs
- Compatible with Energy Star, 0.5W Standby Requirements
- V_{DD} Range From 8V to 24V
- 70m VDS Regulation Function (1)
- Fast Turn-off Total Delay of 20ns
- Reverse Current Protection Function
- Max 300kHz Switching Frequency
- Light Load Mode Function (1) with <600uA Quiescent Current
- Supports CCM, CrCM and DCM Operation Mode
- Available in SOIC8E, SOIC8 or SOIC14 package

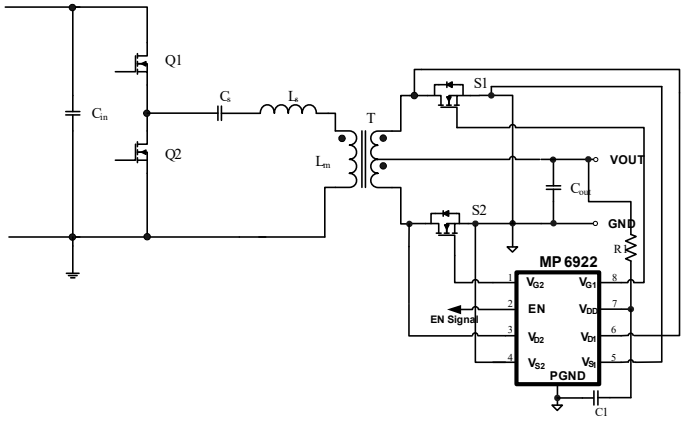
APPLICATIONS

- AC-DC Adapter
- LCD & PDP TV
- Telecom SMPS

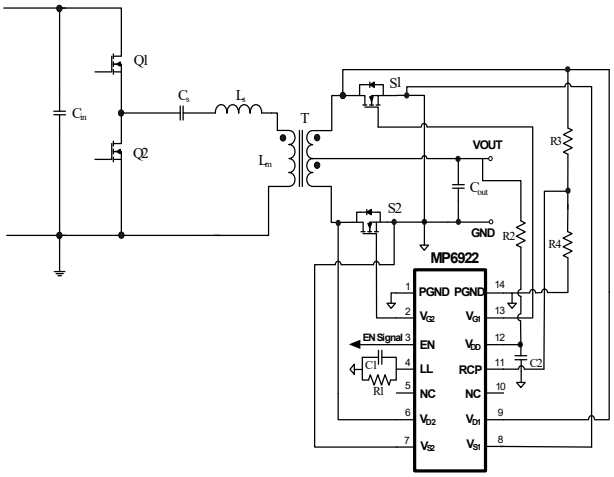
Notes:

1) Related issued patent: US Patent US8,067,973; US8,400,790. CN Patent ZL201010504140.4; ZL200910059751.X. Other patents pending.

TYPICAL APPLICATION



SOIC8E



SOIC14

ORDERING INFORMATION

Part Number	Package	Top Marking
MP6922DN*	SOIC8E	*See Below*
MP6922DS**	SOIC14	*See Below*
MP6922DSE***	SOIC8	*See Below*

*For Tape & Reel, add suffix –Z (e.g. MP6922DN–Z);
For RoHS Compliant Packaging, add suffix –LF; (e.g. MP6922DN–LF–Z)

**For Tape & Reel, add suffix –Z (e.g. MP6922DS–Z);
For RoHS Compliant Packaging, add suffix –LF; (e.g. MP6922DS–LF–Z)

***For Tape & Reel, add suffix –Z (e.g. MP6922DSE–Z);
For RoHS Compliant Packaging, add suffix –LF; (e.g. MP6922DSE–LF–Z)

TOP MARKING (MP6922DN &MP6922DSE)

MP6922
LLLLLLLL
MPSYWW

MPS: MPS prefix
Y: year code
WW: week code
MP6922: part number
LLLLLLLL: lot number

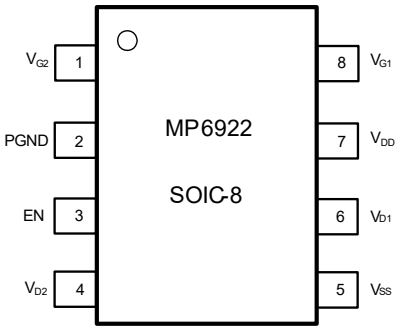
TOP MARKING (MP6922DS)

MPSYYWW
MP6922
LLLLLLLLL

MPS: MPS prefix
YY: year code
WW: week code
MP6922: part number
LLLLLLLLL: lot number

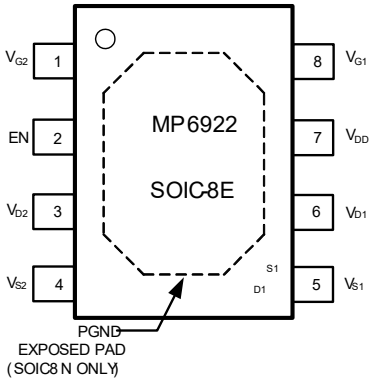
PACKAGE REFERENCE

TOP VIEW



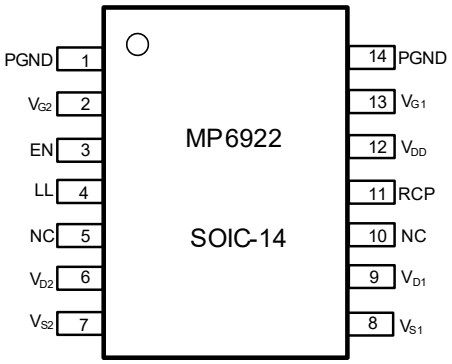
SOIC8

TOP VIEW



SOIC8E

TOP VIEW



SOIC14

ABSOLUTE MAXIMUM RATINGS (2)

V_{DD} to V_{S1},V_{S2}, V_{SS} .....-0.3V to +26V
PGND to V_{S1},V_{S2}, V_{SS}.....-0.3V to +0.3V
V_{G1} to V_{S1}, V_{SS}..... -0.3V to V_{DD}
V_{G2} to V_{S2}, V_{SS}..... -0.3V to V_{DD}
V_{D1} to V_{S1}, V_{SS}.....-0.7V to +180V
V_{D2} to V_{S2}, V_{SS}.....-0.7V to +180V
LL, EN to V_{S1},V_{S2}, V_{SS} .....-0.3V to +6.5V
Maximum Operating Frequency..... 300 kHz
Continuous Power Dissipation.. (T_A = +25°C) (3)
SOIC8E..... 2.5W
SOIC14 ..... 1.5W
SOIC8 ..... 1.4W
Junction Temperature .....150°C
Lead Temperature (Solder).....260°C
Storage Temperature ..... -55°C to +150°C

Recommended Operation Conditions (4)

V_{DD} to V_{S1},V_{S2}, V_{SS}.....8V to 24V
Operating Junction Temp. (T_J).... -40°C to +125°C

Thermal Resistance (4)	θ_{JA}	θ_{JC}	
SOIC8	90	45	°C/W
SOIC8E	50	10	°C/W
SOIC14	86	38	°C/W

Notes:

2) Exceeding these ratings may damage the device.
3) T_A=+25□. The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB. Without heatsink.

ELECTRICAL CHARACTERISTICS

V_{DD} = 12V, T_A= +25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
V_{DD} Voltage Range			8		24	V
V_{DD} UVLO Threshold		Rising	5.0	6.0	7.0	V
		Hysteresis	0.5	1	1.5	V
Quiescent Current	I_q	V_{D1}-V_{S1}=-0.5V, V_{D2}-V_{S2}=-0.5V		4	6	mA
Shutdown Current		V_{DD}=20V, EN=0V			600	μA
Light-load Mode Current					600	μA
Thermal shutdown (6)				150		°C
Thermal Shutdown hysteresis (6)				30		°C
Enable Shutdown Threshold		Rising	1.1	1.5	1.9	V
		Hysteresis		0.2	0.4	V
Enable UVLO Threshold		Rising	2.5	3	3.5	V
		Hysteresis		0.2		V
Internal Pull-up Current on EN				10	15	μA
CONTROL CIRCUITRY SECTION						
$V_{S1,2}$ –$V_{D1,2}$ forward voltage	V_{fwd}		55	70	85	mV
Turn-on delay	T_{Don}	C_{LOAD} = 5nF		150		ns
	T_{Don}	C_{LOAD} = 10nF		250		ns
Input bias current on $V_{D1,2}$ pin		$V_{D1,2}$ = 180V			1	μA
Minimum on-time	T_{MIN}	C_{LOAD} = 5nF		1		μs
Minimum off-time	T_{OFF}			1.6		μs
Light-load-enter delay	$T_{LL\text{-}Delay}$	R_{LL}=100kΩ		120	150	μs
Light-load-enter pulse width	T_{LL}	R_{LL}=100kΩ		2.2		μs
Light-load turn on pulse width hysteresis	$T_{LL\text{-}H}$	R_{LL}=100kΩ		0.2		μs
Light-load-enter off period width	$T_{LL\text{-}OFF}$	R_{LL}=100kΩ		50		μs
Light-load mode exit pulse width threshold ($V_{D1,2}$-$V_{S1,2}$)	$V_{LL\text{-}DS}$		-400	-250		mV
Light-load mode enter pulse width threshold ($V_{G1,2}$-$V_{S1,2}$) (6)	$V_{LL\text{-}GS}$			1.0		V
Reverse Current Protection threshold	V_{RCP}			3		V
Reverse Current Protection latch time	T_{RCP}			100		μs
GATE DRIVER SECTION						
$V_{G1,2}$ (Low)		I_{LOAD}=1mA		0.05	0.1	V
$V_{G1,2}$ (High)		V_{DD} >16V		14		V
		V_{DD} <16V		V_{DD}-2.2		
Turn off threshold ($V_{S1,2}$-$V_{D1,2}$) (6)				-30		mV
Turn-off propagation delay		$V_{D1,2}$=V_{SS}		15		ns
Turn-off total delay	T_{Doff}	$V_{D1,2}$ =V_{SS}, C_{LOAD}=5nF, R_{GATE}=0Ω		35		ns
	T_{Doff}	$V_{D1,2}$ =V_{SS}, C_{LOAD}=10nF, R_{GATE}=0Ω		45		ns
Pull down impedance				1	2	Ω
Pull down current (6)		3V <$V_{G1,2}$<10V		3		A

6) Guaranteed by Design and Characterization

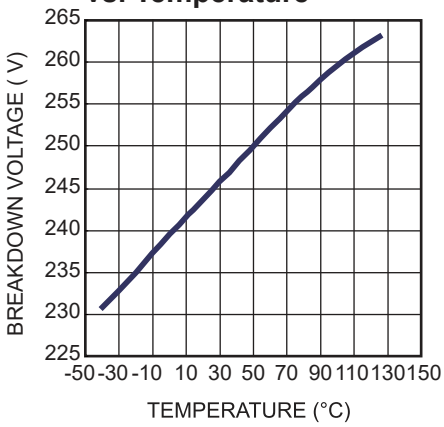
PIN FUNCTIONS

Pin # (SOIC8)	Pin # (SOIC8E)	Pin # (SOIC14)	Name	Description
1	1	2	V_{G2}	FET 2 gate driver output
3	2	3	EN	Enable Pin. When EN pin voltage is larger than EN Shutdown threshold, the internal logic of the IC is start but the gate driver will be latched until the EN pin voltage has exceed the EN UVLO threshold
4	3	6	V_{D2}	FET 2 drain voltage sense
-	4	7	V_{S2}	Source pin used as reference for V_{D2}
-	5	8	V_{S1}	Source pin used as reference for V_{D1}
6	6	9	V_{D1}	FET 1 drain voltage sense
7	7	12	V_{DD}	Supply Voltage
8	8	13	V_{G1}	FET 1 gate driver output
2	EXPOSED PAD	1,14	PGND	Power Ground, return for power switch
-	-	5,10	NC	No Connection
-	-	4	LL	Light load timing setting. Connect a resistor to set the light load timing
-	-	11	RCP	Reverse Protection function, internal 5V reference.
5	-	-	V_{SS}	Common source pin used as reference for both channels

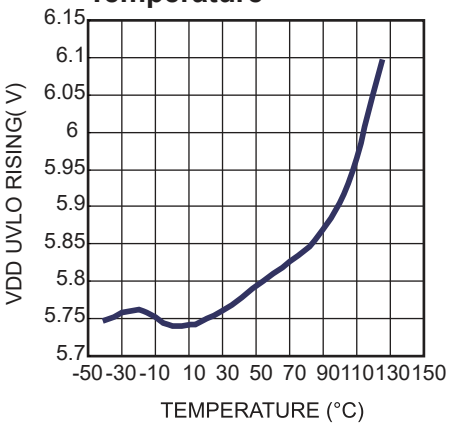
TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD} = 12V, unless otherwise noted.

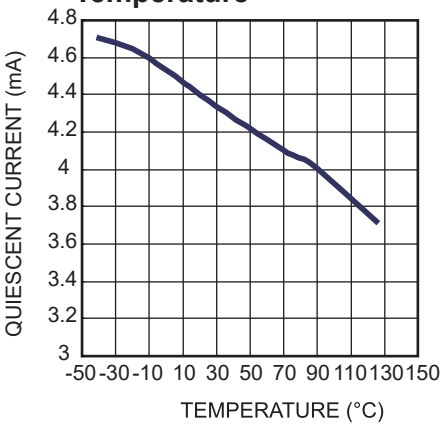
$V_{D1,2}$ Breakdown Voltage vs. Temperature



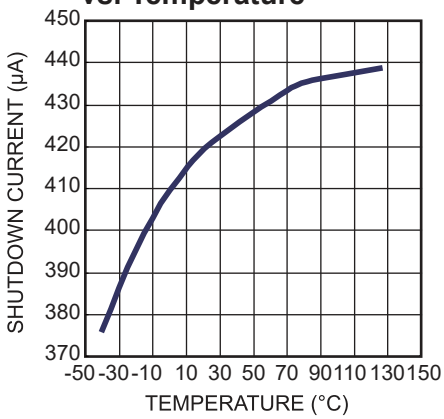
VDD UVLO Rising vs. Temperature



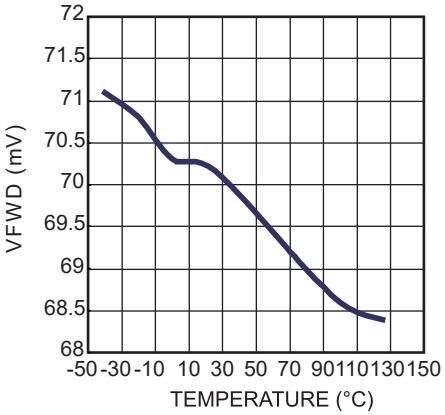
Quiescent Current vs. Temperature



Shutdown Current (VDD=20V) vs. Temperature



Vfwd vs. Temperature

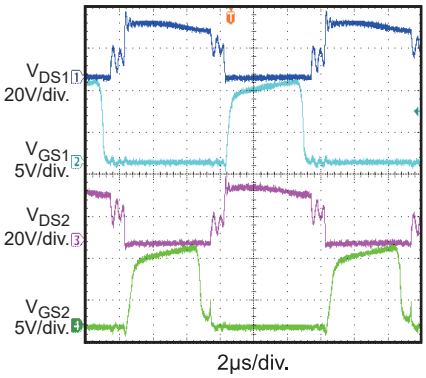


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{DD} = 12V, unless otherwise noted.

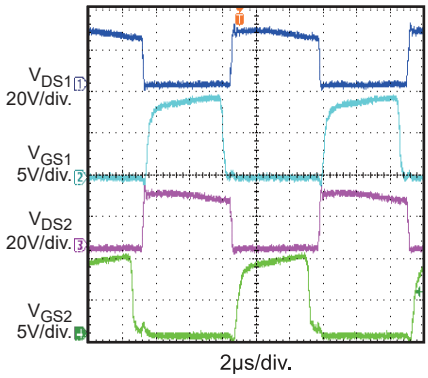
Operation in 180W LLC Converter

V_{IN}=220Vac, V_{OUT}=12V, I_{OUT}=15A



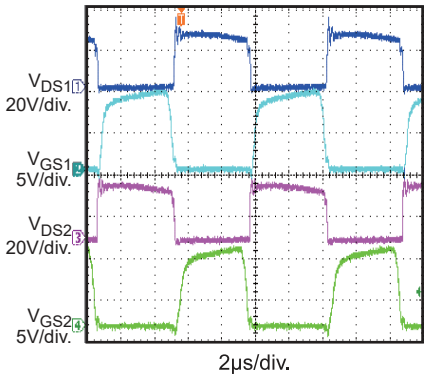
Operation in 180W LLC Converter

V_{IN}=240Vac, V_{OUT}=12V, I_{OUT}=15A



Operation in 180W LLC Converter

V_{IN}=260Vac, V_{OUT}=12V, I_{OUT}=15A



BLOCK DIAGRAM

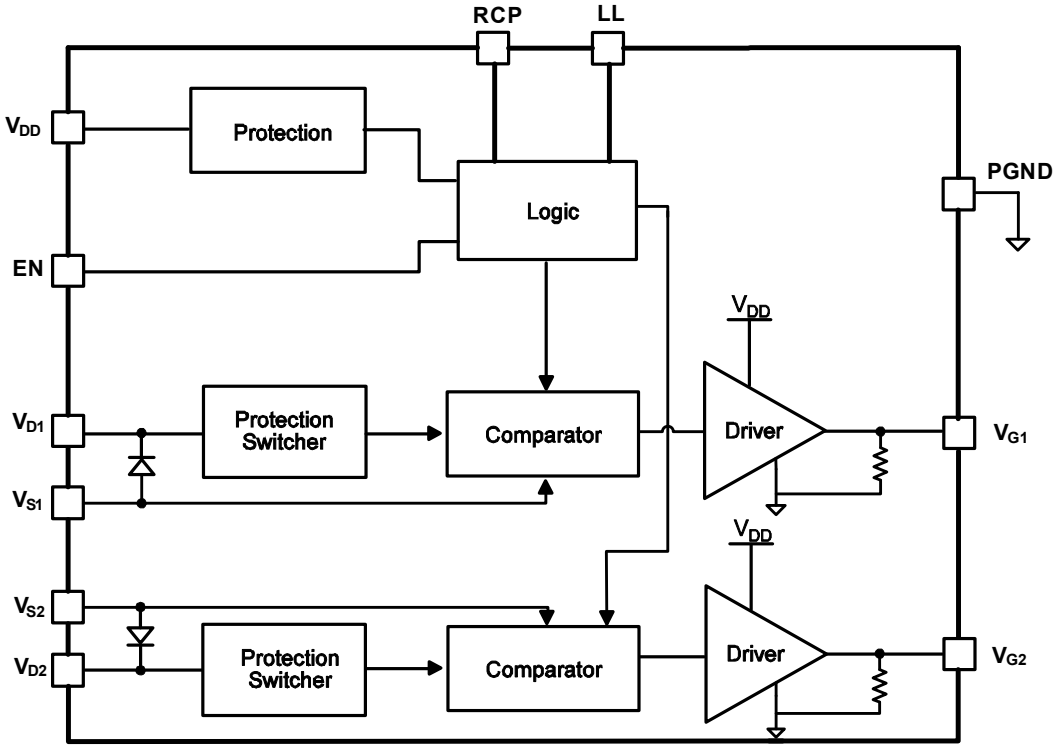


Figure 1—Functional Block Diagram

OPERATION

The MP6922 supports operation in DCM, CCM and CrCM condition. Operating in either a DCM or CrCM condition, the control circuitry controls the gate in forward mode and will turn the gate off when the MOSFET current is fairly low. In CCM operation, the control circuitry turns off the gate when very fast transients occur.

Blanking

The control circuitry contains blanking function. When it pulls the MOSFET on/off, it makes sure that the on/off state at least lasts for some time. The turn on blanking time is ~1us, which determines the minimum on-time. During the turn on blanking period, the turn off threshold is not totally blanked, but changed to ~+100mV (instead of 30mV). This assures that the part can always be turned off even during the turn on blanking period. (Albeit slower, so it is not recommended to set the synchronous period less than 1μs at CCM condition in LLC converter, otherwise shoot through may occur)

VD Clamp

Because $V_{D1,2}$ can go as high as 180V, a High-Voltage JFET is used at the input. To avoid excessive currents when Vg goes below -0.7V, a small resistor is recommended between $V_{D1,2}$ pin and the drain of the external MOSFET.

Under-Voltage Lockout (UVLO)

When V_{DD} is below UVLO threshold, the part falls into sleep mode and Vg is pulled down by a 10kΩ resistor.

Enable pin

If EN is pulled low, the part is in sleep mode.

Thermal shutdown

If the junction temperature of the IC exceeds 150°C, Vg will be pulled low and the part

stops switching. The part will return to normal operation after the junction temperature has dropped to 120°C.

Turn-on Phase

When the switch current flows through the body diode of the MOSFET, there will be a negative V_{DS} (V_D-V_{SS}) across it (<-500mV), the V_{DS} is much lower than the turn on threshold of the control circuitry (-70mV), which then turns on the MOSFET after 200ns turn-on delay (defined in Fig.2).

As soon as the turn on threshold (-70mV) is triggered, a blanking time (Minimum on-time: ~1us) will be added during which the turn off threshold will be changed from 0mV to +50mV. This blanking time can help to avoid error trigger on turn off threshold caused by the turn on ringing of the synchronous power switch.

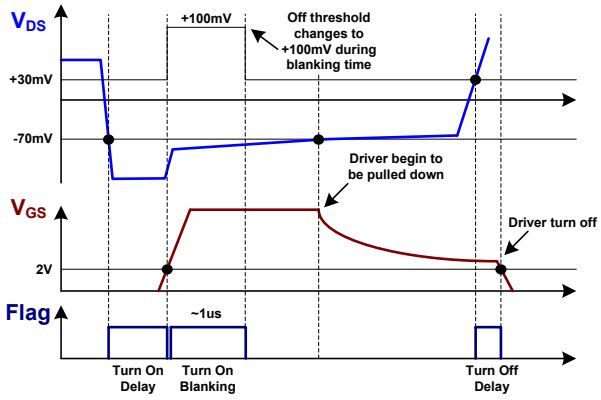


Figure 2—Turn on and Turn off delay

Conducting Phase

When the MOSFET is turned on, V_{DS} (-I_{SD} X $r_{DS(ON)}$) becomes to rise according to the drop of the switch current (I_{SD}) , as soon as V_{DS} rises above the turn on threshold (-70mV), the control circuitry stops pulling up the gate driver and the driver voltage of the MOSFET dropped, which makes the on resistance $r_{DS(ON)}$ of the MOSFET becomes larger. By doing that, V_{DS} (-I_{SD} x $r_{DS(ON)}$) is adjusted to be around -70mV even when the switch current I_{SD} is fairly small, this function can make the turn off threshold (0mV) of the internal driver never triggered until the current through the MOSFET has dropped to near zero.

Turn-off Phase

When V_{DS} rises to trigger the turn off threshold (30mV), the driver voltage of the switch is pulled to low after about 20ns turn off delay (defined in Fig.4) by the control circuitry. Similar with turn-on phase, a 1.6us blanking time is added after the switch is turned off, during which the MOSFET is never turned on to avoid error trigger.

Fig.3 show the MP6922 operation at heavy load condition. Due to the high current, the driver voltage will be saturated at first. After V_{DS} goes to above -70mV, driver voltage decreases to adjust the V_{DS} to typical -70mV.

Fig.4 show the MP6922 operation at light load condition. Due to the low current, the driver voltage never saturates but begins to decrease as soon as the synchronous power switch is turned on and adjust the V_{DS}.

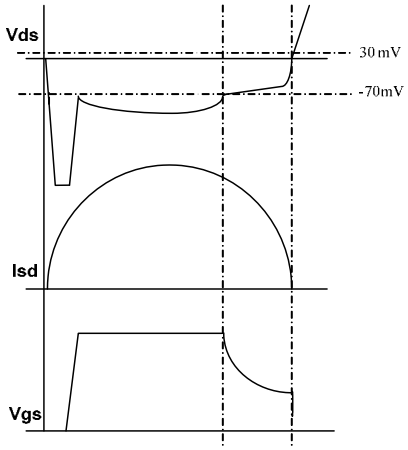


Figure 3—Synchronous Rectification Operation at heavy load

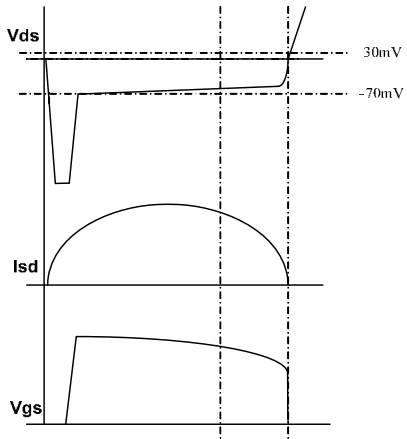


Figure 4—Synchronous Rectification Operation at light load

Light-load Latch-off Function

The gate driver of MP6922 is latched to save the driver loss at light-load condition to improve light load efficiency.

Latch off during Normal Operation

When the MOSFET conducting period during each switching cycle keeps lower than 2.2us (T_{LL}), the MP6922 falls into light-load mode and latches off the MOSFET after 120us delay (light-load-enter delay, $T_{LL\text{-}Delay}$)

After falling into light-load mode, MP6922 monitors the MOSFET's body diode conducting period by sensing V_{DS} (when V_{DS} exceeds -250mV ($V_{LL\text{-}DS}$), MP6922 considers the MOSFET's body diode conducting period finishes). If the MOSFET's body diode conducting period is longer than ~2.4us (T_{LL}+$T_{LL\text{-}H}$), the light-load mode is finished and the MOSFET is unlatched to restart the synchronous rectification.

For SOIC14 package MP6922 with LL pin, the T_{LL} could be adjusted by an external resistor:

$$T_{LL} = 2.2\mu s \cdot \frac{R_{LL}}{100k\Omega}$$

Latch off during Burst Operation

The IC also monitors the synchronous MOSFET off period, if the off period is longer than the light-load-enter off period width ($T_{LL\text{-}OFF}$), MP6922 enters light-load mode and latches off the gate driver.

The gate driver is unlatched when the drain-source voltage of the synchronous MOSFET V_{DS} drops below -70mV.

Reverse Current Protection Function

When the LLC system operates in CCM with very high frequency, the synchronous current may get reverse before the IC turns off the gate driver which leads to shoot through (in center-tapped output with full-wave rectification topology). MP6922 has protection function to latch off the gate driver when the current reverses before the driver signal is pulled low.

When the synchronous current reverses, the high spike can be observed between Drain-Source of MOSFET. The MP6922 monitors the voltage by RCP pin through a voltage divider. When the voltage of RCP pin exceeds V_{RCP}, MP6922 will latch the driver signal of both channels for ~100us (T_{RCP}) to protect the synchronous MOSFET. At the end of T_{RCP}, MP6922 restarts the synchronous rectification.

TYPICAL APPLICATION CIRCUIT

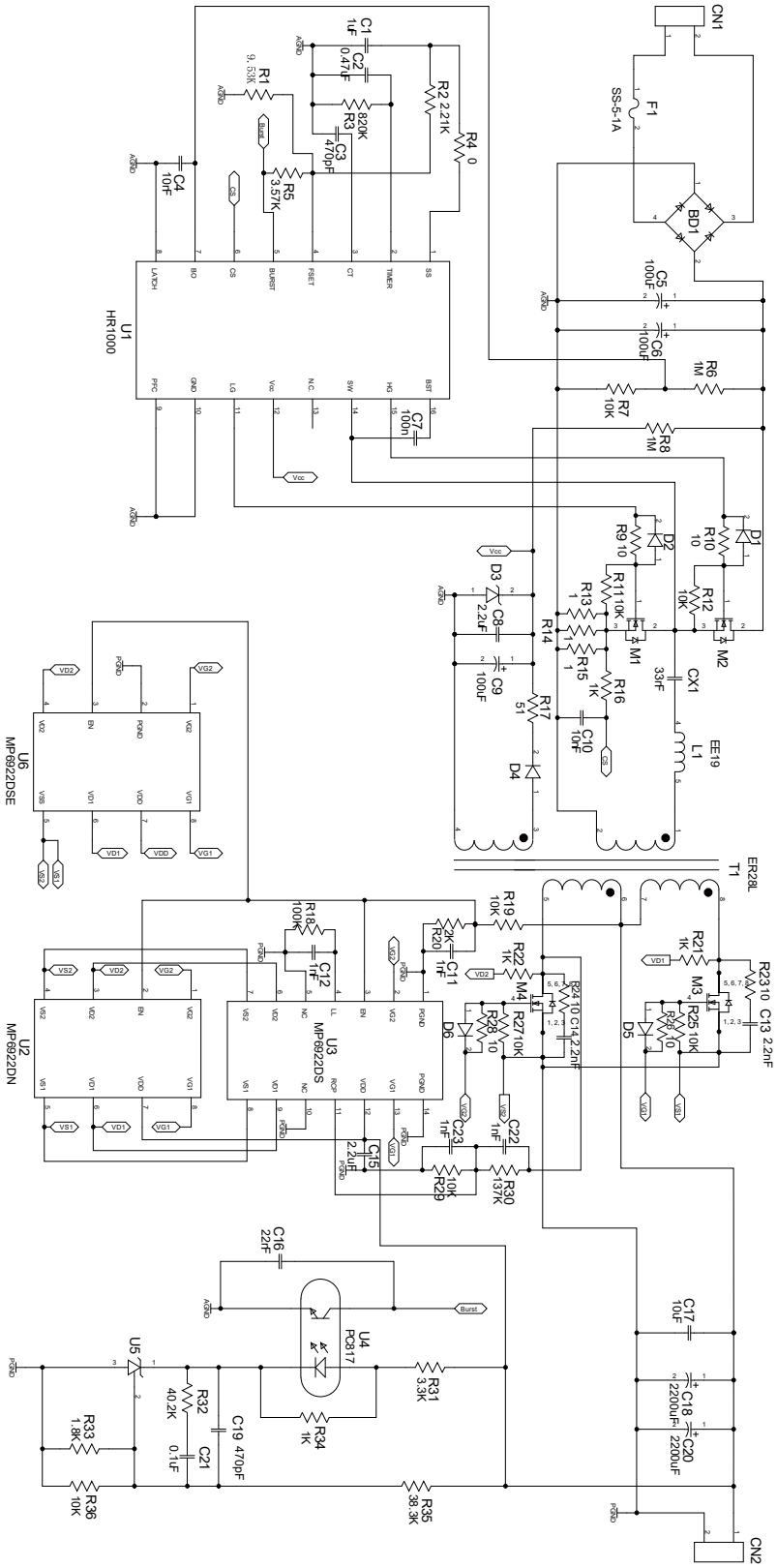
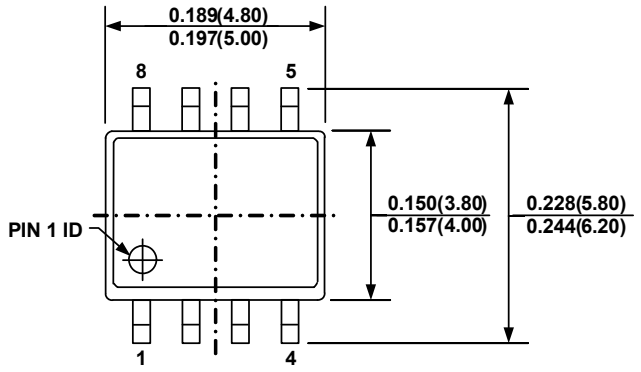


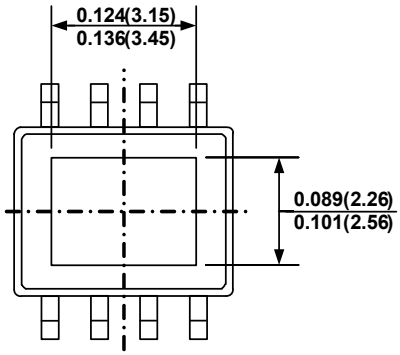
Figure 5—Synchronous Rectification in LLC with MP6922

PACKAGE INFORMATION

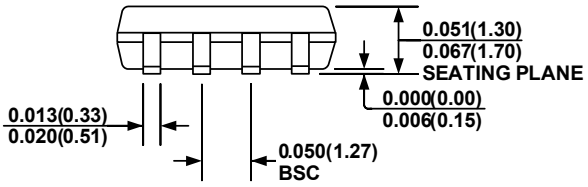
SOIC8E (EXPOSED PAD)



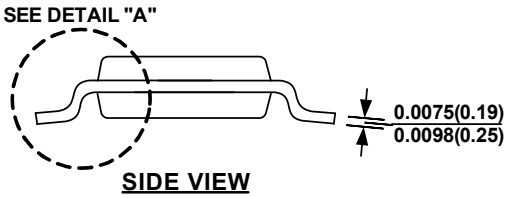
TOP VIEW



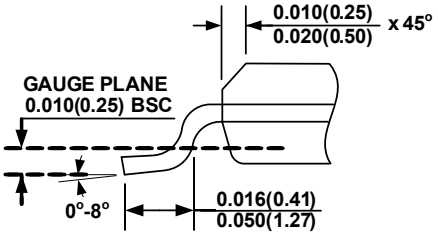
BOTTOM VIEW



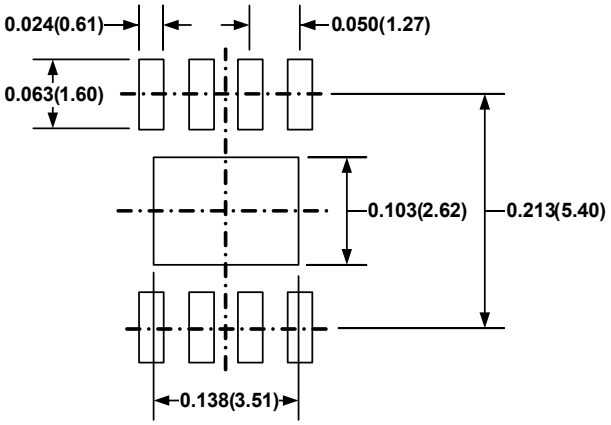
FRONT VIEW



SIDE VIEW



DETAIL "A"

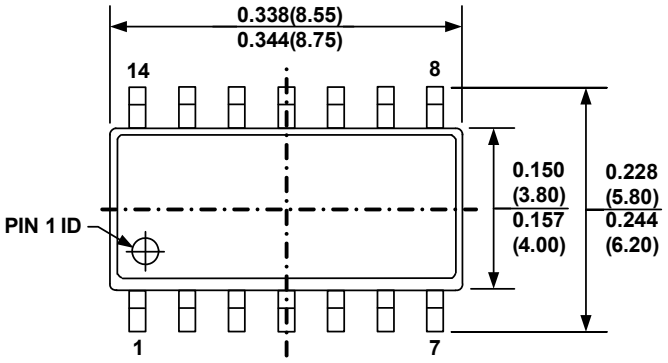


RECOMMENDED LAND PATTERN

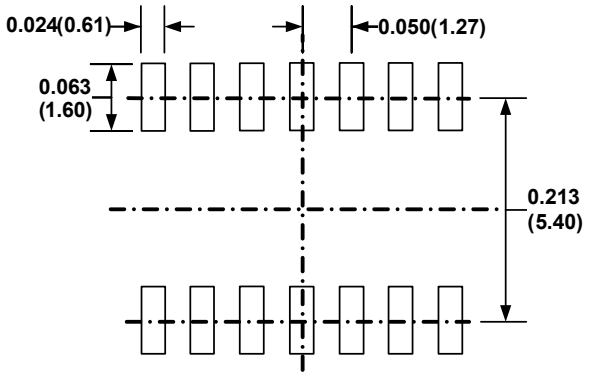
NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY(BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6) DRAWING IS NOT TO SCALE.

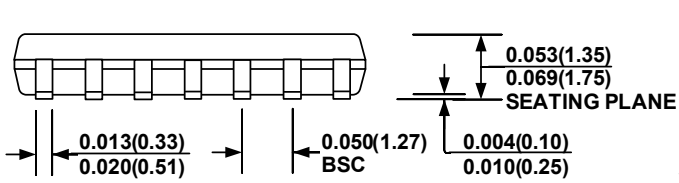
SOIC14



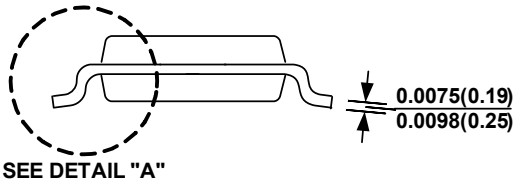
TOP VIEW



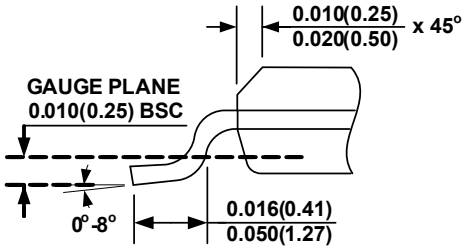
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW

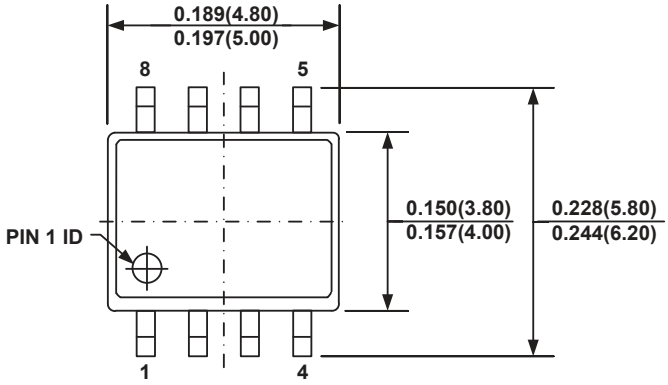


DETAIL "A"

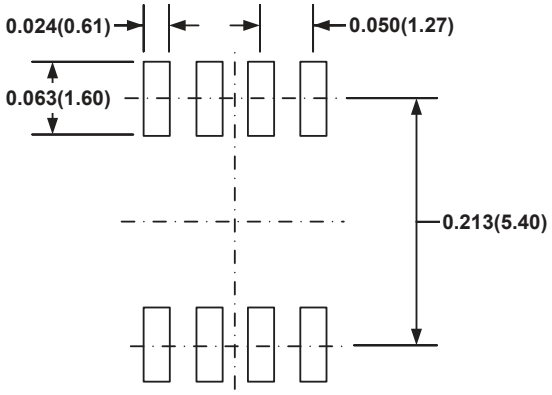
NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY(BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AB.
6) DRAWING IS NOT TO SCALE

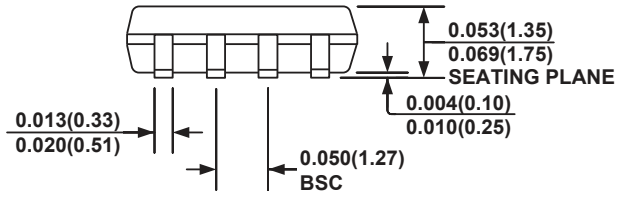
SOIC8



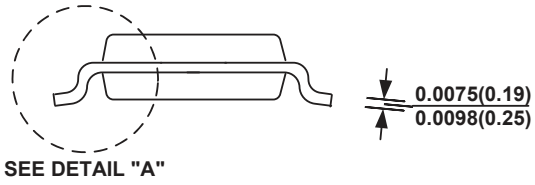
TOP VIEW



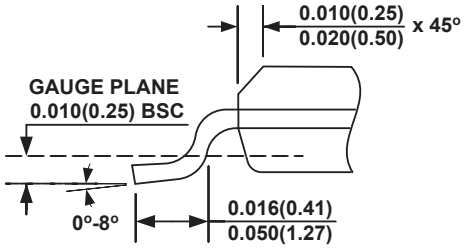
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

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4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.