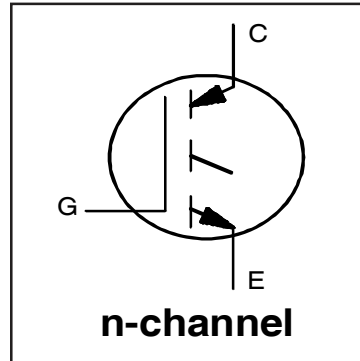


**INSULATED GATE BIPOLAR TRANSISTOR**

**IRGP4063PbF**  
**IRGP4063-EPbF**

**Features**

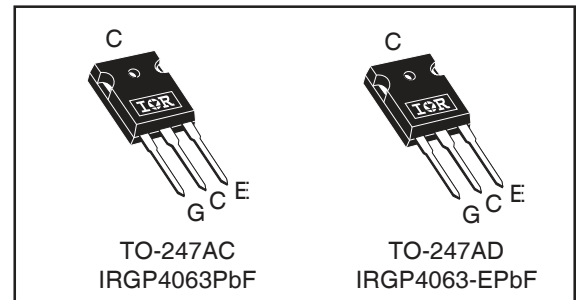
- Low  $V_{CE(ON)}$  Trench IGBT Technology
- Low switching losses
- Maximum Junction temperature 175 °C
- 5  $\mu$ S short circuit SOA
- Square RBSOA
- 100% of the parts tested for  $I_{LM}$  ①
- Positive  $V_{CE(ON)}$  Temperature co-efficient
- Tight parameter distribution
- Lead Free Package



$V_{CES} = 600V$
$I_C = 48A, T_C = 100^\circ C$
$t_{SC} \geq 5\mu s, T_{J(max)} = 175^\circ C$
$V_{CE(on)} \text{ typ.} = 1.65V$

**Benefits**

- High Efficiency in a wide range of applications
- Suitable for a wide range of switching frequencies due to Low  $V_{CE(ON)}$  and Low Switching losses
- Rugged transient Performance for increased reliability
- Excellent Current sharing in parallel operation
- Low EMI



<b>G</b>	<b>C</b>	<b>E</b>
Gate	Collector	Emitter

**Absolute Maximum Ratings**

	Parameter	Max.	Units
$V_{CES}$	Collector-to-Emitter Voltage	600	V
$I_C @ T_C = 25^\circ C$	Continuous Collector Current	96 ②	A
$I_C @ T_C = 100^\circ C$	Continuous Collector Current	48	
$I_{CM}$	Pulse Collector Current, $V_{GE} = 15V$	144	A
$I_{LM}$	Clamped Inductive Load Current, $V_{GE} = 20V$ ①	192	A
$V_{GE}$	Continuous Gate-to-Emitter Voltage	$\pm 20$	V
	Transient Gate-to-Emitter Voltage	$\pm 30$	
$P_D @ T_C = 25^\circ C$	Maximum Power Dissipation	330	W
$P_D @ T_C = 100^\circ C$	Maximum Power Dissipation	170	
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to +175	°C
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting Torque, 6-32 or M3 Screw	10 lbf-in (1.1 N·m)	

**Thermal Resistance**

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$ (IGBT)	Thermal Resistance Junction-to-Case-(each IGBT)	—	—	0.45	°C/W
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink (flat, greased surface)	—	0.24	—	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (typical socket mount)	—	—	40	

## Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)

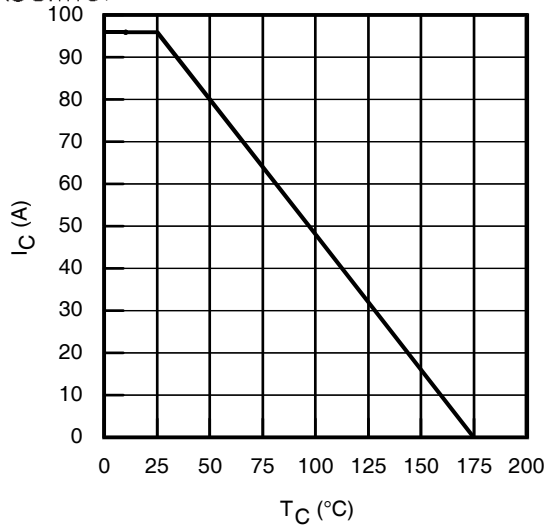
	Parameter	Min.	Typ.	Max.	Units	Conditions	Ref.Fig
V <sub>(BR)CES</sub>	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V <sub>GE</sub> = 0V, I <sub>C</sub> = 150μA ④	CT6
ΔV <sub>(BR)CES</sub> /ΔT <sub>J</sub>	Temperature Coeff. of Breakdown Voltage	—	0.30	—	V/°C	V <sub>GE</sub> = 0V, I <sub>C</sub> = 1mA (25°C-175°C)	CT6
V <sub>CE(on)</sub>	Collector-to-Emitter Saturation Voltage	—	1.65	2.14	V	I <sub>C</sub> = 48A, V <sub>GE</sub> = 15V, T <sub>J</sub> = 25°C	5,6,7
		—	2.0	—		I <sub>C</sub> = 48A, V <sub>GE</sub> = 15V, T <sub>J</sub> = 150°C	8,9,10
		—	2.05	—		I <sub>C</sub> = 48A, V <sub>GE</sub> = 15V, T <sub>J</sub> = 175°C	
V <sub>GE(th)</sub>	Gate Threshold Voltage	4.0	—	6.5	V	V <sub>CE</sub> = V <sub>GE</sub> , I <sub>C</sub> = 1.4mA	8,9
ΔV <sub>GE(th)</sub> /ΔT <sub>J</sub>	Threshold Voltage temp. coefficient	—	-21	—	mV/°C	V <sub>CE</sub> = V <sub>GE</sub> , I <sub>C</sub> = 1.0mA (25°C - 175°C)	10,11
g <sub>fe</sub>	Forward Transconductance	—	32	—	S	V <sub>CE</sub> = 50V, I <sub>C</sub> = 48A, PW = 80μs	
I <sub>CES</sub>	Collector-to-Emitter Leakage Current	—	1.0	150	μA	V <sub>GE</sub> = 0V, V <sub>CE</sub> = 600V	
		—	450	1000		V <sub>GE</sub> = 0V, V <sub>CE</sub> = 600V, T <sub>J</sub> = 175°C	
I <sub>GES</sub>	Gate-to-Emitter Leakage Current	—	—	±100	nA	V <sub>GE</sub> = ±20V	

## Switching Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)

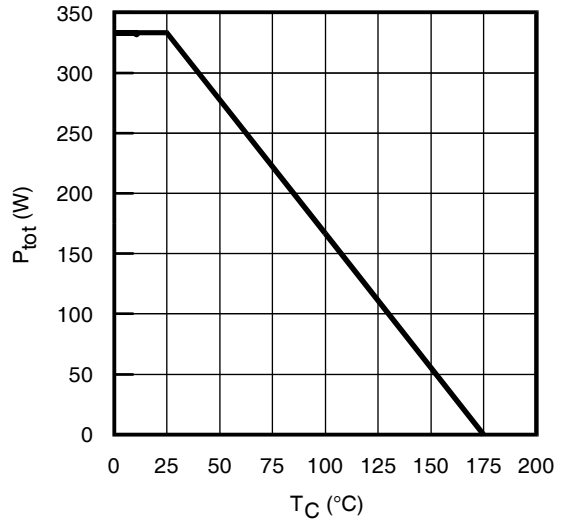
	Parameter	Min.	Typ.	Max.	Units	Conditions	Ref.Fig
Q <sub>g</sub>	Total Gate Charge (turn-on)	—	95	140	nC	I <sub>C</sub> = 48A	18
Q <sub>ge</sub>	Gate-to-Emitter Charge (turn-on)	—	28	42		V <sub>GE</sub> = 15V	CT1
Q <sub>gc</sub>	Gate-to-Collector Charge (turn-on)	—	35	53		V <sub>CC</sub> = 400V	
E <sub>on</sub>	Turn-On Switching Loss ⑤	—	625	1141	μJ	I <sub>C</sub> = 48A, V <sub>CC</sub> = 400V, V <sub>GE</sub> = 15V	CT4
E <sub>off</sub>	Turn-Off Switching Loss	—	1275	1481		R <sub>G</sub> = 10Ω, L = 200μH, L <sub>S</sub> = 150nH, T <sub>J</sub> = 25°C	
E <sub>total</sub>	Total Switching Loss	—	1900	2622		Energy losses include tail & diode reverse recovery	
t <sub>d(on)</sub>	Turn-On delay time	—	60	78		I <sub>C</sub> = 48A, V <sub>CC</sub> = 400V, V <sub>GE</sub> = 15V	CT4
t <sub>r</sub>	Rise time	—	40	56	ns	R <sub>G</sub> = 10Ω, L = 200μH, L <sub>S</sub> = 150nH, T <sub>J</sub> = 25°C	
t <sub>d(off)</sub>	Turn-Off delay time	—	145	176			
t <sub>f</sub>	Fall time	—	35	46			
E <sub>on</sub>	Turn-On Switching Loss ⑤	—	1625	—		μJ	I <sub>C</sub> = 48A, V <sub>CC</sub> = 400V, V <sub>GE</sub> = 15V
E <sub>off</sub>	Turn-Off Switching Loss	—	1585	—	R <sub>G</sub> = 10Ω, L = 200μH, L <sub>S</sub> = 150nH, T <sub>J</sub> = 175°C ④		CT4
E <sub>total</sub>	Total Switching Loss	—	3210	—	Energy losses include tail & diode reverse recovery		WF1, WF2
t <sub>d(on)</sub>	Turn-On delay time	—	55	—	I <sub>C</sub> = 48A, V <sub>CC</sub> = 400V, V <sub>GE</sub> = 15V		13, 15
t <sub>r</sub>	Rise time	—	45	—	ns	R <sub>G</sub> = 10Ω, L = 200μH, L <sub>S</sub> = 150nH	CT4
t <sub>d(off)</sub>	Turn-Off delay time	—	165	—		T <sub>J</sub> = 175°C	WF1
t <sub>f</sub>	Fall time	—	45	—			WF2
C <sub>ies</sub>	Input Capacitance	—	3025	—		pF	V <sub>GE</sub> = 0V
C <sub>oes</sub>	Output Capacitance	—	245	—	V <sub>CC</sub> = 30V		
C <sub>res</sub>	Reverse Transfer Capacitance	—	90	—	f = 1.0Mhz		
RBSOA	Reverse Bias Safe Operating Area	FULL SQUARE				T <sub>J</sub> = 175°C, I <sub>C</sub> = 192A V <sub>CC</sub> = 480V, V <sub>p</sub> = 600V R <sub>G</sub> = 10Ω, V <sub>GE</sub> = +15V to 0V	4 CT2
SCSOA	Short Circuit Safe Operating Area	5	—	—	μs	V <sub>CC</sub> = 400V, V <sub>p</sub> = 600V R <sub>G</sub> = 10Ω, V <sub>GE</sub> = +15V to 0V	16, CT3 WF3

### Notes:

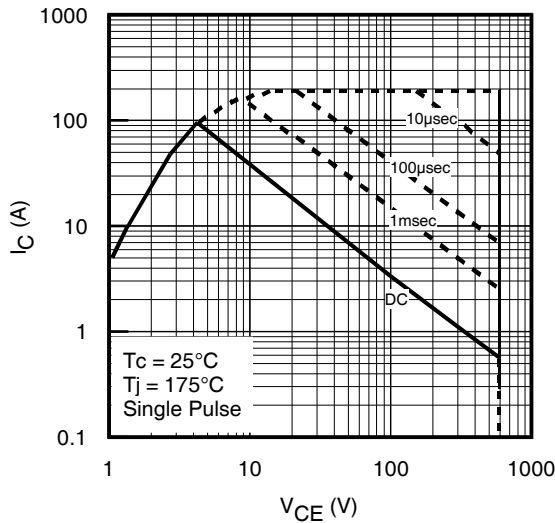
- ① V<sub>CC</sub> = 80% (V<sub>CES</sub>), V<sub>GE</sub> = 20V, L = 200μH, R<sub>G</sub> = 10Ω.
- ② This is only applied to TO-247AC package.
- ③ Pulse width limited by max. junction temperature.
- ④ Refer to AN-1086 for guidelines for measuring V<sub>(BR)CES</sub> safely.
- ⑤ Turn-on energy is measured using the same co-pak diode as IRGP4063DPbF.
- ⑥ Calculated continuous current based on maximum allowable junction temperature.  
Bond wire current limit is 80A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements.



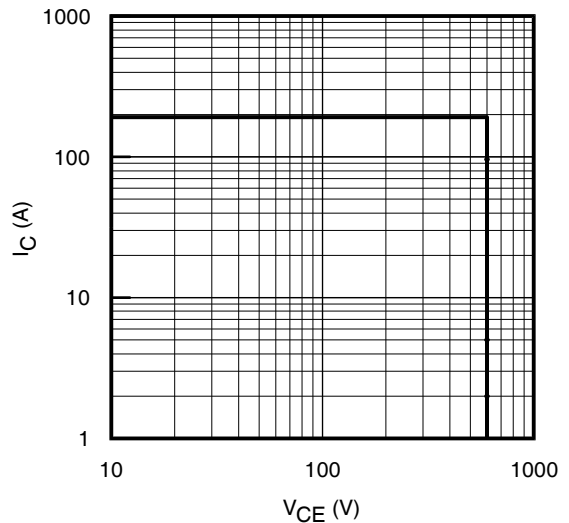
**Fig. 1 - Maximum DC Collector Current vs. Case Temperature**



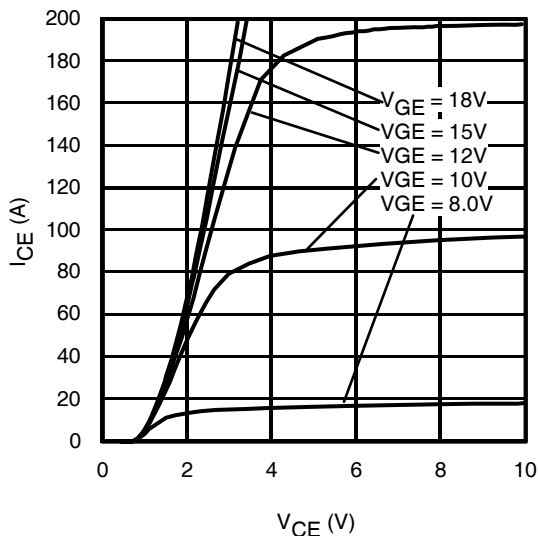
**Fig. 2 - Power Dissipation vs. Case Temperature**



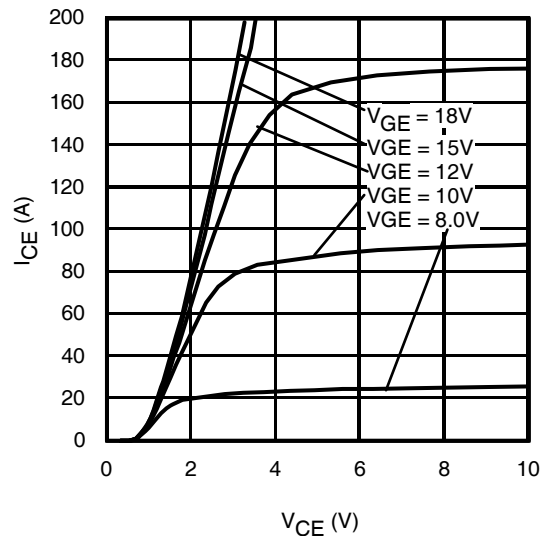
**Fig. 3 - Forward SOA**  
 $T_C = 25^\circ\text{C}$ ,  $T_J \leq 175^\circ\text{C}$ ;  $V_{GE} = 15\text{V}$



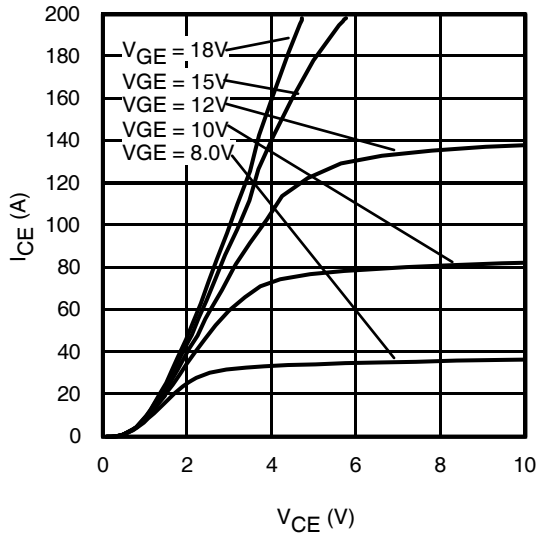
**Fig. 4 - Reverse Bias SOA**  
 $T_J = 175^\circ\text{C}$ ;  $V_{GE} = 15\text{V}$



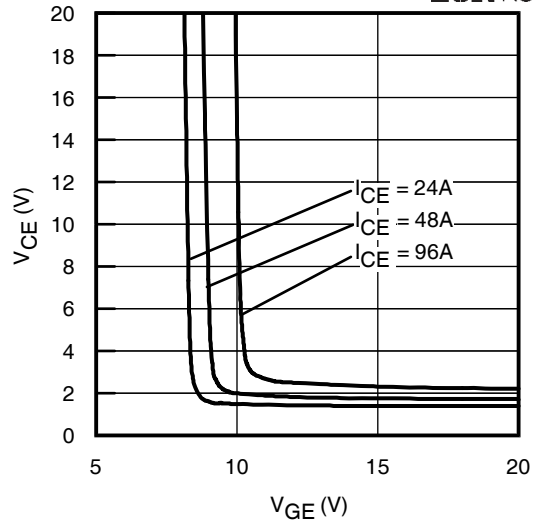
**Fig. 5 - Typ. IGBT Output Characteristics**  
 $T_J = -40^\circ\text{C}$ ;  $t_p = 80\mu\text{s}$



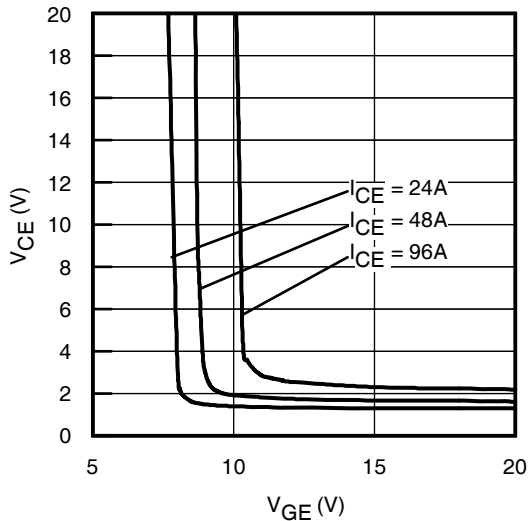
**Fig. 6 - Typ. IGBT Output Characteristics**  
 $T_J = 25^\circ\text{C}$ ;  $t_p = 80\mu\text{s}$



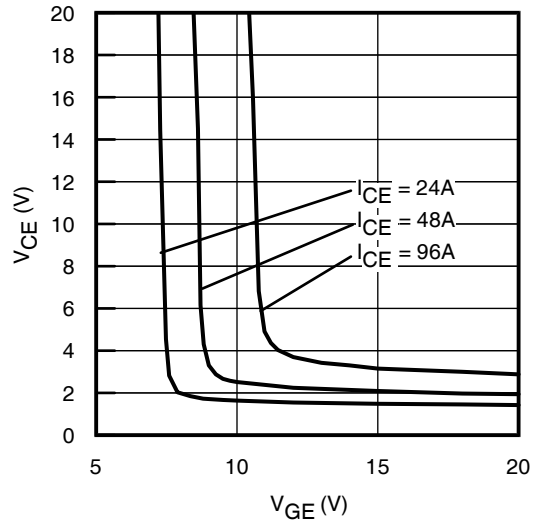
**Fig. 7** - Typ. IGBT Output Characteristics  
 $T_J = 175^\circ\text{C}$ ;  $t_p = 80\mu\text{s}$



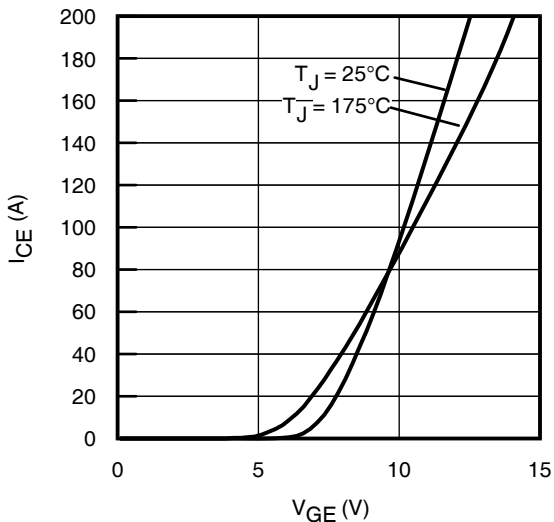
**Fig. 8** - Typical  $V_{CE}$  vs.  $V_{GE}$   
 $T_J = -40^\circ\text{C}$



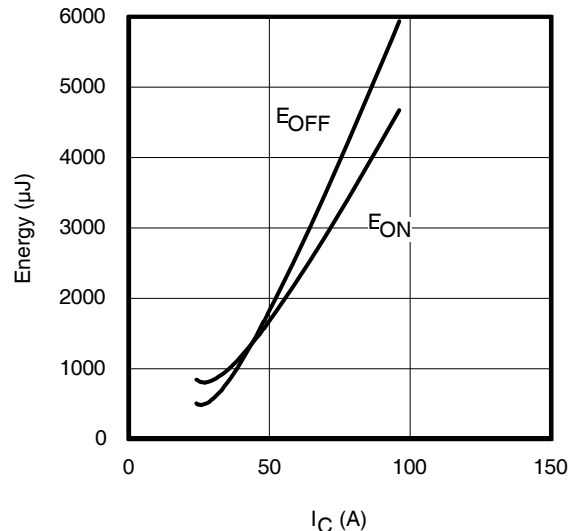
**Fig. 9** - Typical  $V_{CE}$  vs.  $V_{GE}$   
 $T_J = 25^\circ\text{C}$



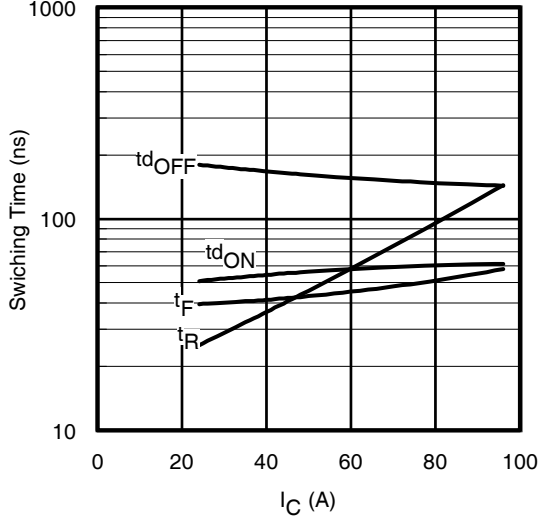
**Fig. 10** - Typical  $V_{CE}$  vs.  $V_{GE}$   
 $T_J = 175^\circ\text{C}$



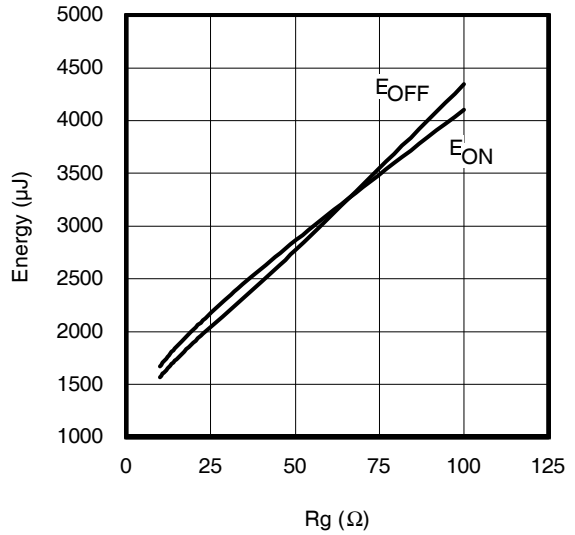
**Fig. 11** - Typ. Transfer Characteristics  
 $V_{CE} = 50\text{V}$ ;  $t_p = 10\mu\text{s}$



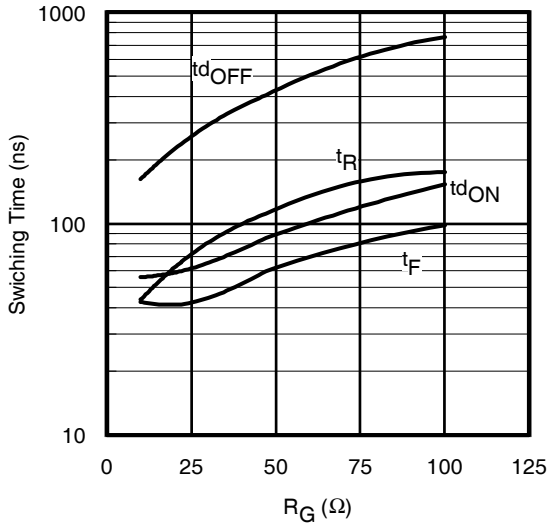
**Fig. 12** - Typ. Energy Loss vs.  $I_C$   
 $T_J = 175^\circ\text{C}$ ;  $L = 200\mu\text{H}$ ;  $V_{CE} = 400\text{V}$ ;  $R_G = 10\Omega$ ;  $V_{GE} = 15\text{V}$



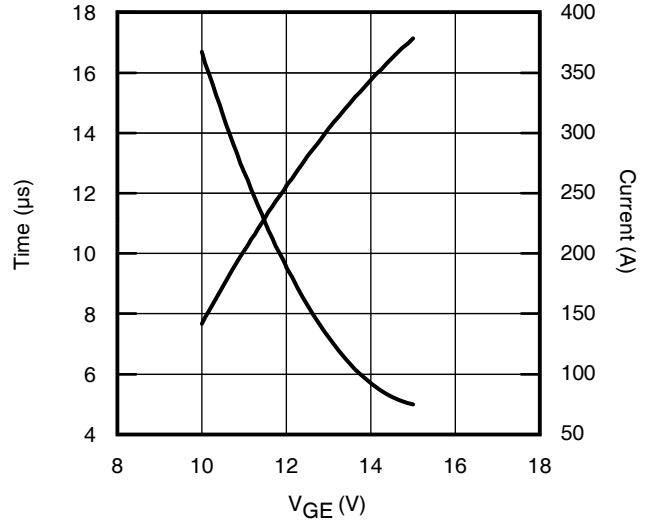
**Fig. 13 - Typ. Switching Time vs.  $I_C$**   
 $T_J = 175^\circ\text{C}$ ;  $L = 200\mu\text{H}$ ;  $V_{CE} = 400\text{V}$ ;  $R_G = 10\Omega$ ;  $V_{GE} = 15\text{V}$



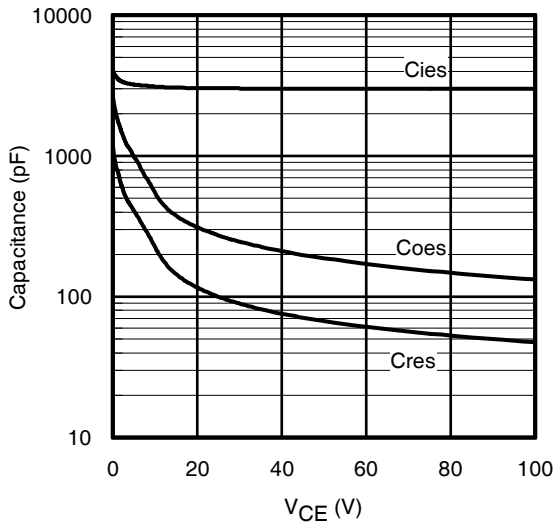
**Fig. 14 - Typ. Energy Loss vs.  $R_G$**   
 $T_J = 175^\circ\text{C}$ ;  $L = 200\mu\text{H}$ ;  $V_{CE} = 400\text{V}$ ;  $I_{CE} = 48\text{A}$ ;  $V_{GE} = 15\text{V}$



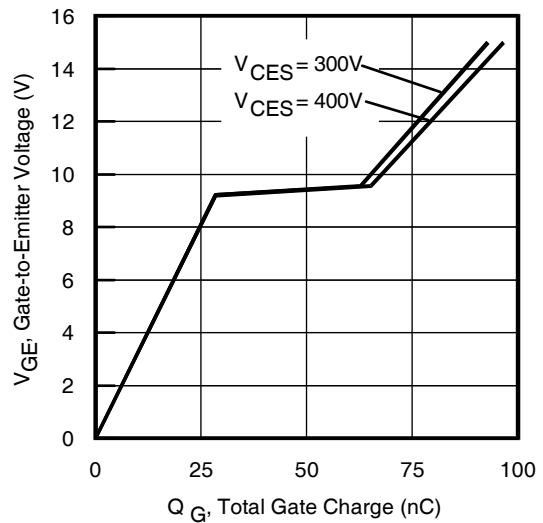
**Fig. 15 - Typ. Switching Time vs.  $R_G$**   
 $T_J = 175^\circ\text{C}$ ;  $L = 200\mu\text{H}$ ;  $V_{CE} = 400\text{V}$ ;  $I_{CE} = 48\text{A}$ ;  $V_{GE} = 15\text{V}$



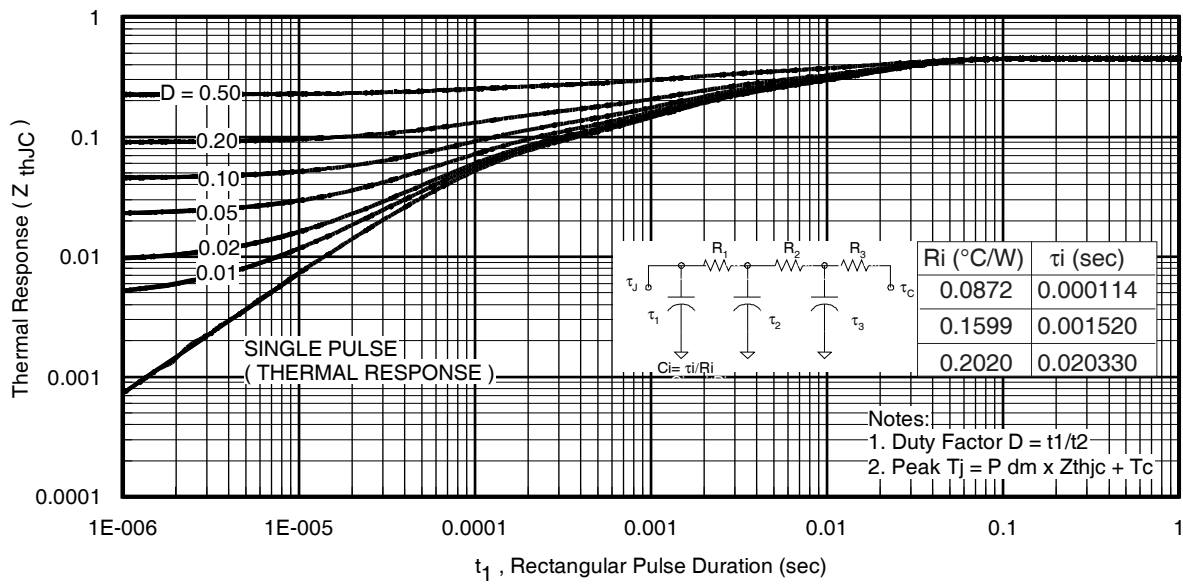
**Fig. 16 -  $V_{GE}$  vs. Short Circuit Time**  
 $V_{CC} = 400\text{V}$ ;  $T_C = 25^\circ\text{C}$



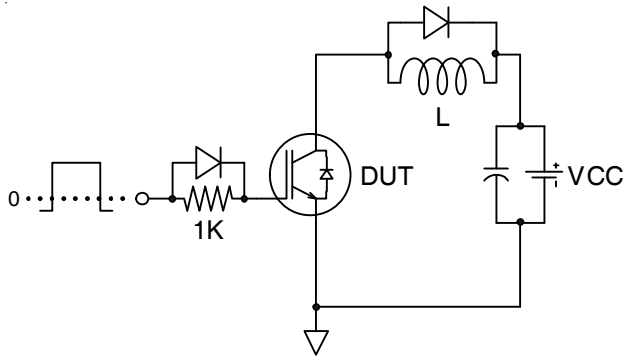
**Fig. 17 - Typ. Capacitance vs.  $V_{CE}$**   
 $V_{GE} = 0\text{V}$ ;  $f = 1\text{MHz}$



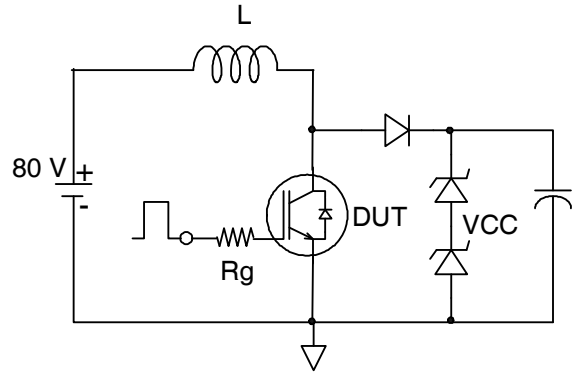
**Fig. 18 - Typical Gate Charge vs.  $V_{GE}$**   
 $I_{CE} = 48\text{A}$ ;  $L = 600\mu\text{H}$



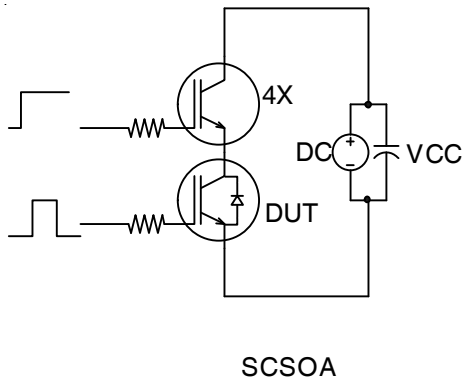
**Fig 19.** Maximum Transient Thermal Impedance, Junction-to-Case (IGBT)



**Fig.C.T.1** - Gate Charge Circuit (turn-off)

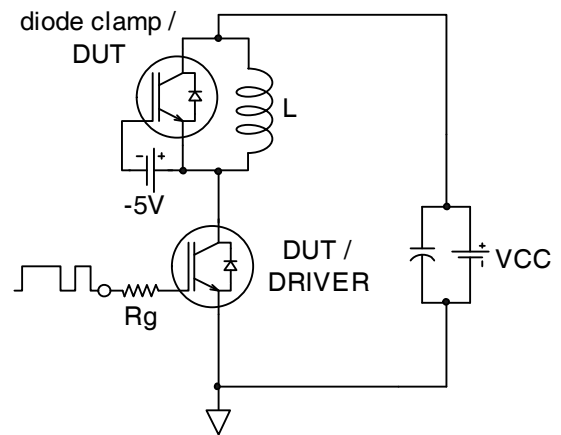


**Fig.C.T.2** - RBSOA Circuit

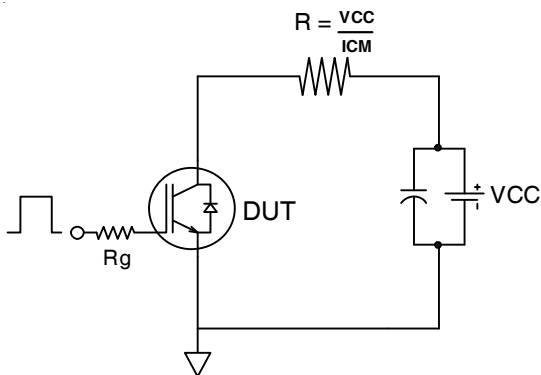


SCSOA

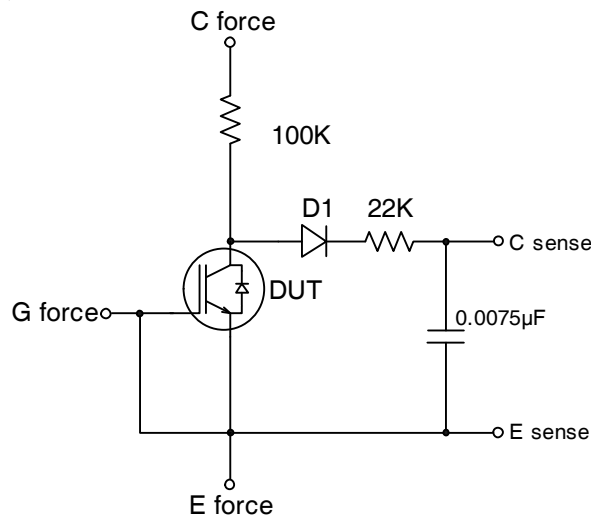
**Fig.C.T.3** - S.C. SOA Circuit



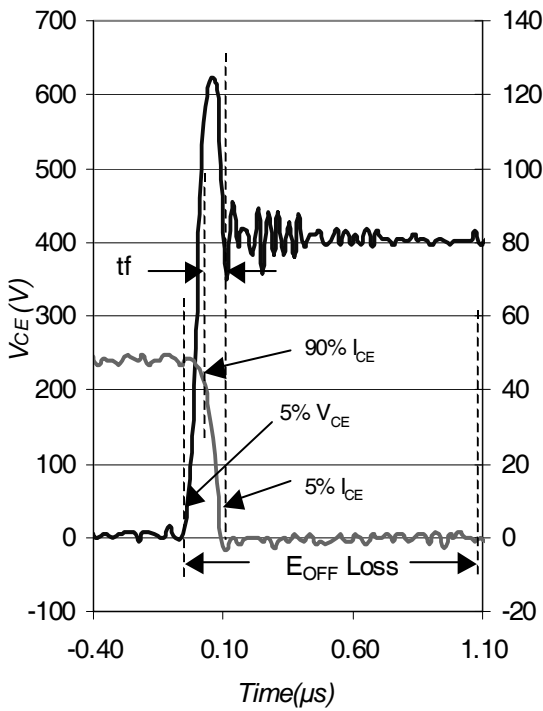
**Fig.C.T.4** - Switching Loss Circuit



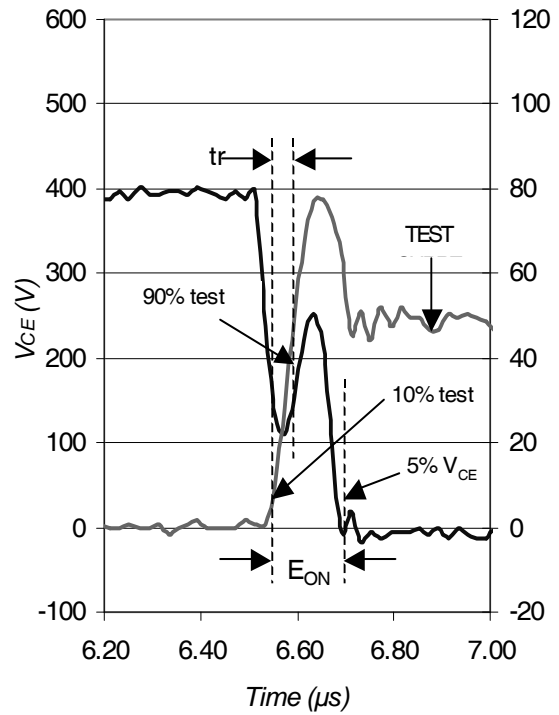
**Fig.C.T.5** - Resistive Load Circuit



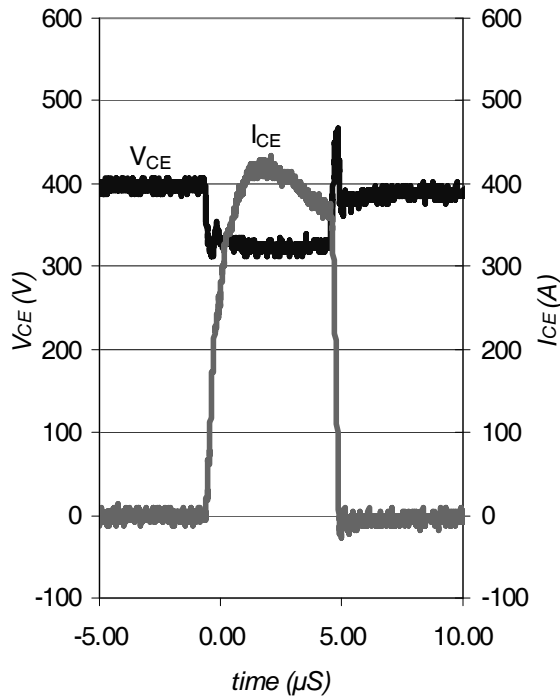
**Fig.C.T.6** - BVCES Filter Circuit



**Fig. WF1** - Typ. Turn-off Loss Waveform  
@  $T_J = 175^\circ\text{C}$  using Fig. CT.4



**Fig. WF2** - Typ. Turn-on Loss Waveform  
@  $T_J = 175^\circ\text{C}$  using Fig. CT.4

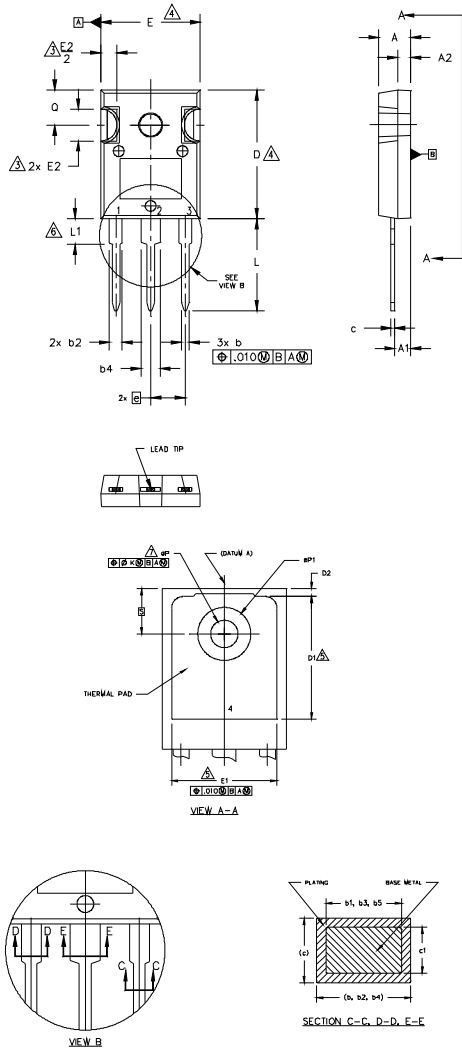


**Fig. WF3** - Typ. S.C. Waveform  
@  $T_J = 25^\circ\text{C}$  using Fig. CT.3



## TO-247AC Package Outline

Dimensions are shown in millimeters (inches)



**NOTES:**

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M 1994.
2. DIMENSIONS ARE SHOWN IN INCHES.
3. CONTOUR OF SLOT OPTIONAL.
4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
6. LEAD FINISH UNCONTROLLED IN L1.
7.  $\phi P$  TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154 INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247AC .

SYMBOL	DIMENSIONS				NOTES
	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	.183	.209	4.65	5.31	
A1	.087	.102	2.21	2.59	
A2	.059	.098	1.50	2.49	
b	.039	.055	0.99	1.40	
b1	.039	.053	0.99	1.35	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.34	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
c	.015	.035	0.38	0.89	
c1	.015	.033	0.38	0.84	
D	.776	.815	19.71	20.70	4
D1	.515	-	13.08	-	5
D2	.020	.053	0.51	1.35	
E	.602	.625	15.29	15.87	4
E1	.530	-	13.46	-	
E2	.178	.216	4.52	5.49	
e	.215 BSC		5.46 BSC		
$\phi k$	.010		0.25		
L	.559	.634	14.20	16.10	
L1	.146	.169	3.71	4.29	
$\phi P$	.140	.144	3.56	3.66	
$\phi P1$	-	.291	-	7.39	
Q	.209	.224	5.31	5.69	
S	.217 BSC		5.51 BSC		

LEAD ASSIGNMENTS

HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

IGBTs, CoPACK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

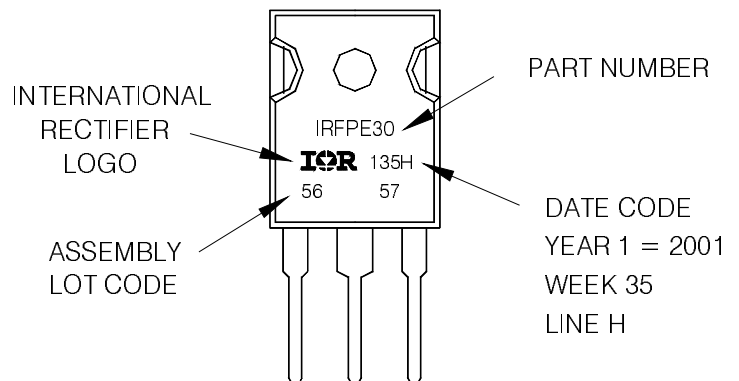
DIODES

- 1.- ANODE/OPEN
- 2.- CATHODE
- 3.- ANODE

## TO-247AC Part Marking Information

EXAMPLE: THIS IS AN IRFPE30  
WITH ASSEMBLY  
LOT CODE 5657  
ASSEMBLED ON WW 35, 2001  
IN THE ASSEMBLY LINE "H"

Note: "P" in assembly line position  
indicates "Lead-Free"



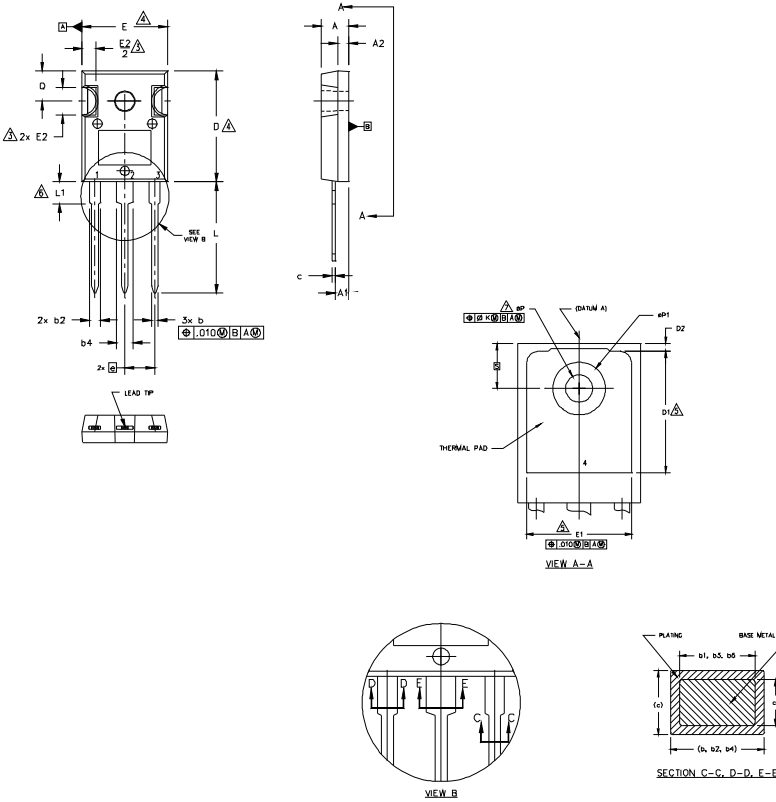
TO-247AC package is not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

# IRGP4063PbF/IRGP4063-EPbF

## TO-247AD Package Outline

Dimensions are shown in millimeters (inches)



**NOTES:**

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M 1994.
2. DIMENSIONS ARE SHOWN IN INCHES.
3. CONTOUR OF SLOT OPTIONAL.
4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
6. LEAD FINISH UNCONTROLLED IN L1.
7. ϕP TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5 ° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154 INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247AD.

SYMBOL	DIMENSIONS				NOTES
	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	.183	.209	4.65	5.31	
A1	.087	.102	2.21	2.59	
A2	.059	.098	1.50	2.49	
b	.039	.055	0.99	1.40	
b1	.039	.053	0.99	1.35	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.34	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
c	.015	.035	0.38	0.89	
c1	.015	.033	0.38	0.84	
D	.776	.815	19.71	20.70	4
D1	.515	-	13.08	-	5
D2	.020	.053	0.51	1.35	
E	.602	.625	15.29	15.87	4
E1	.530	-	13.46	-	
E2	.178	.216	4.52	5.49	
e	.215 BSC		5.46 BSC		
ϕk	.010		0.25		
L	.780	.827	19.57	21.00	
L1	.146	.169	3.71	4.29	
ϕP	.140	.144	3.56	3.66	
ϕP1	-	.291	-	7.39	
Q	.209	.224	5.31	5.69	
S	.217 BSC		5.51 BSC		

**LEAD ASSIGNMENTS**

**HEXFET**

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

**IGBTs, CoPACK**

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

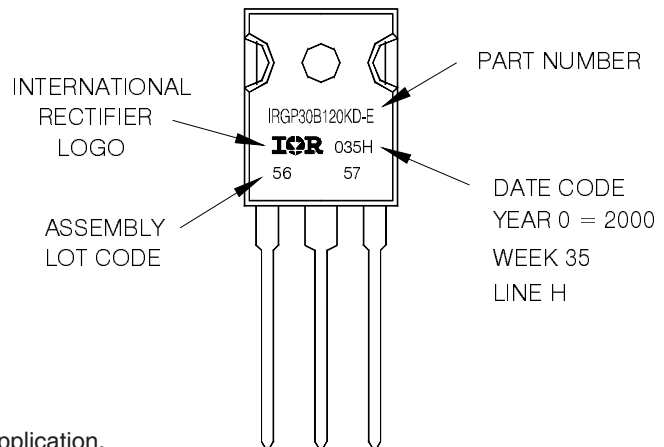
**DIODES**

- 1.- ANODE/OPEN
- 2.- CATHODE
- 3.- ANODE

## TO-247AD Part Marking Information

EXAMPLE: THIS IS AN IRGP30B120KD-E  
WITH ASSEMBLY  
LOT CODE 5657  
ASSEMBLED ON WW 35, 2000  
IN THE ASSEMBLY LINE "H"

Note: "P" in assembly line position  
indicates "Lead-Free"



TO-247AD package is not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Data and specifications subject to change without notice.  
This product has been designed and qualified for Industrial market.  
Qualification Standards can be found on IR's Web site.