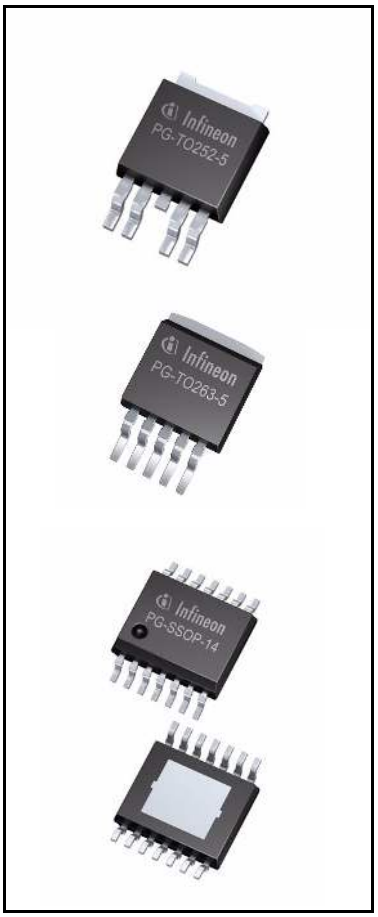
# OPTIREG™ linear TLE42754

## Low dropout linear voltage regulator

AEC Qualified

RoHS




## Features

- Output voltage 5 V ± 2%
- Ouput current up to 450 mA
- Very low current consumption
- Power-on and undervoltage reset with programmable delay time
- Reset low down to $V_Q$ = 1 V
- Very low dropout voltage
- Output current limitation
- Reverse polarity protection
- Overtemperature protection
- Suitable for use in automotive electronics
- Wide temperature range from -40°C up to 150°C
- Input voltage range from -42 V to 45 V
- Green Product (RoHS compliant)

## Potential applications

General automotive applications.

## Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.

## Description

The OPTIREG™ linear TLE42754 is a monolithic integrated low-dropout voltage regulator in a 5-pin TO-package, especially designed for automotive applications. An input voltage up to 42 V is regulated to an output voltage of 5.0 V. The component is able to drive loads up to 450 mA. It is short-circuit proof by the implemented current limitation and has an integrated overtemperature shutdown. A reset signal is generated for an output voltage $V_{Q,rt}$ of typically 4.65 V. The power-on reset delay time can be programmed by the external delay capacitor.

| Type | Package | Marking |
|---|---|---|
| TLE42754D | PG-TO252-5 | 42754D |
| TLE42754G | PG-TO263-5 | TLE42754 |
| TLE42754E | PG-SSOP-14 exposed pad | 42754E |

### Dimensioning information on external components

An input capacitor $C_I$ is recommended for compensation of line influences. An output capacitor $C_Q$ is necessary for the stability of the control loop.

### Circuit description

The control amplifier compares a reference voltage to a voltage that is proportional to the output voltage and drives the base of the series transistor via a buffer. Saturation control as a function of the load current prevents any oversaturation of the power element. The component also has a number of internal circuits for protection against:

- Overload
- Overtemperature
- Reverse polarity

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# 1 Block diagram

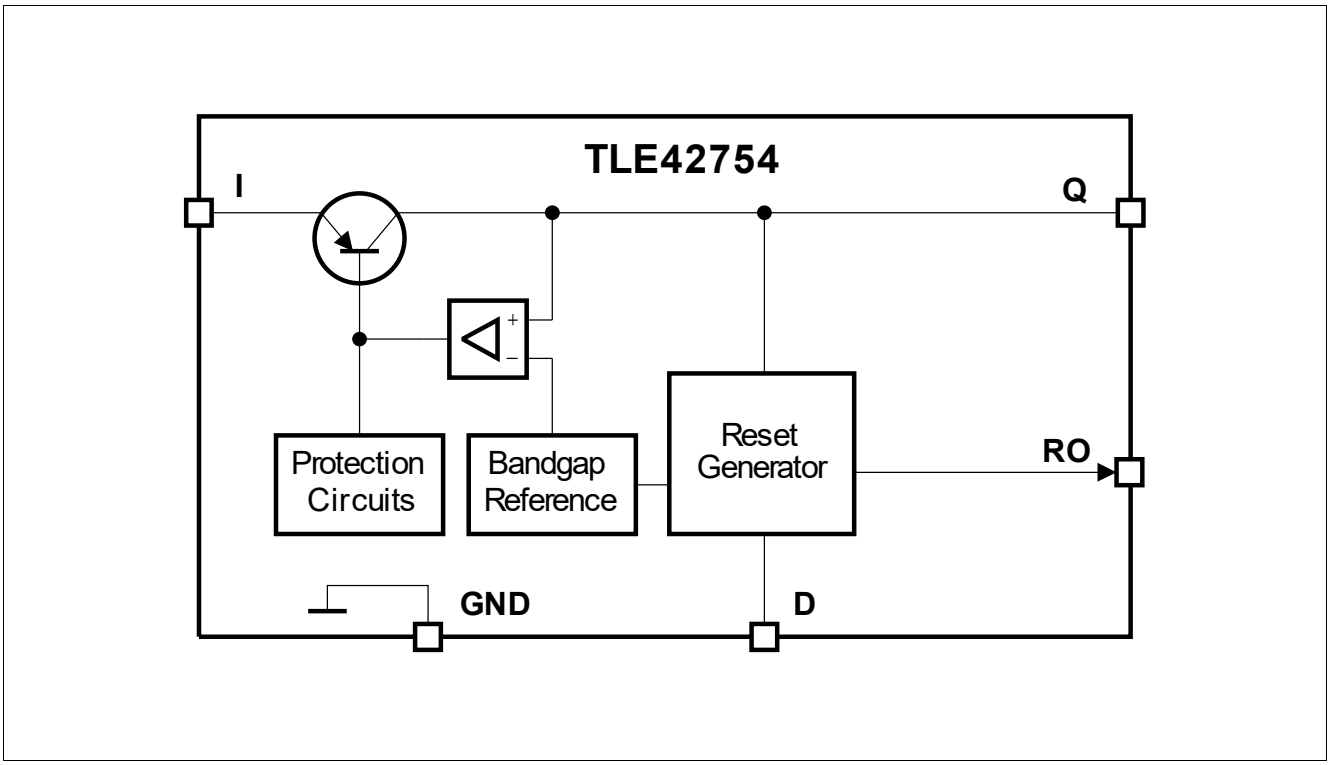



**Figure 1 Block diagram**

# 2 Pin configuration

## 2.1 Pin assignment TLE42754D (PG-TO252-5) and TLE42754G (PG-TO263-5)

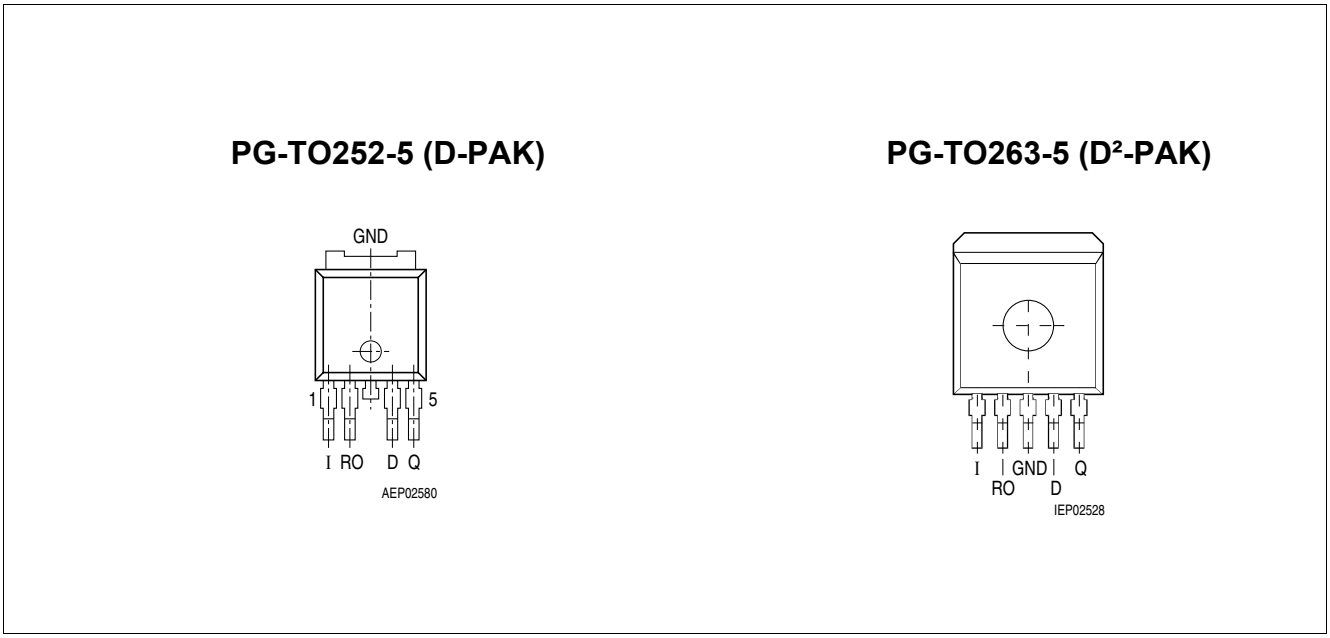



**Figure 2 Pin configuration (top view)**

## 2.2 Pin definitions and functions TLE42754D (PG-TO252-5) and TLE42754G (PG-TO263-5)

| Pin | Symbol | Function |
|---|---|---|
| 1 | I | **Input**<br>For compensating line influences, a capacitor to GND close to the IC terminals is recommended. |
| 2 | RO | **Reset output**<br>Open collector output; external pull-up resistor to a positive potential required; leave open if the reset function is not needed. |
| 3 | GND | **TLE42754G (PG-TO263-5) only: ground**<br>Internally connected to tab. |
| 4 | D | **Reset delay timing**<br>Connect a ceramic capacitor to GND for adjusting the reset delay time; leave open if the reset function is not needed. |
| 5 | Q | **Output**<br>Block to GND with a capacitor close to the IC terminals, respecting the values given for its capacitance $C_Q$ and ESR in the table **“Functional range” on Page 8**. |
| TAB | GND | **Ground**<br>Connect to heatsink area. |

## 2.3 Pin assignment TLE42754E (PG-SSOP-14 exposed pad)

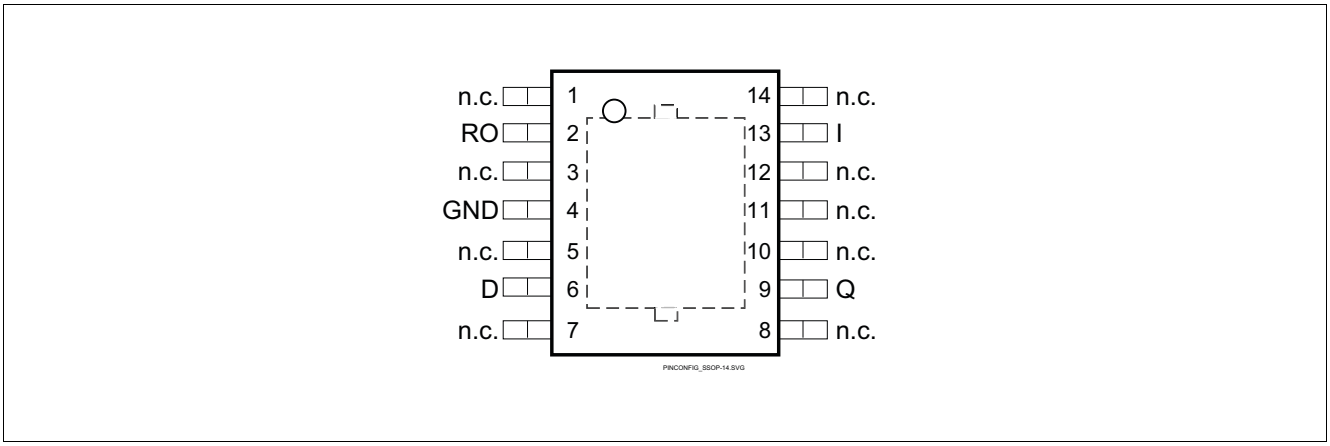



**Figure 3 Pin configuration (top view)**

## 2.4 Pin definitions and functions TLE42754E (PG-SSOP-14 exposed pad)

| Pin | Symbol | Function |
|---|---|---|
| 1,3,5,7 | n.c. | **Not connected**<br>Leave open or connect to GND. |
| 2 | RO | **Reset output**<br>Open collector output; external pull-up resistor to a positive potential required; leave open if the reset function is not needed. |
| 4 | GND | **Ground** |
| 6 | D | **Reset delay timing**<br>Connect a ceramic capacitor to GND for adjusting the reset delay time; leave open if the reset function is not needed. |
| 8,10,11,12, 14 | n.c. | **Not connected**<br>Leave open or connect to GND. |
| 9 | Q | **Output**<br>Block to GND with a capacitor close to the IC terminals, respecting the values given for its capacitance $C_Q$ and ESR in the table **“Functional range” on Page 8**. |
| 13 | I | **Input**<br>For compensating line influences, a capacitor to GND close to the IC terminals is recommended. |
| Pad | – | **Exposed pad**<br>Connect to heatsink area; connect with GND on PCB. |

# 3 General product characteristics

## 3.1 Absolute maximum ratings

**Table 1 Absolute maximum ratings[1)]**

$T_j$ = -40°C to 150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Input** | | | | | | | |
| Voltage | $V_I$ | -42 | – | 45 | V | – | P_4.1.1 |
| **Output** | | | | | | | |
| Voltage | $V_Q$ | -0.3 | – | 7 | V | – | P_4.1.2 |
| **Reset output** | | | | | | | |
| Voltage | $V_{RO}$ | -0.3 | – | 25 | V | – | P_4.1.3 |
| **Reset delay** | | | | | | | |
| Voltage | $V_D$ | -0.3 | – | 7 | V | – | P_4.1.4 |
| **Temperature** | | | | | | | |
| Junction temperature | $T_j$ | -40 | – | 150 | °C | – | P_4.1.5 |
| Storage temperature | $T_{stg}$ | -50 | – | 150 | °C | – | P_4.1.6 |
| **ESD absorption** | | | | | | | |
| ESD absorption | $V_{ESD,HBM}$ | -2 | – | 2 | kV | Human Body Model (HBM)[2)] | P_4.1.7 |
| ESD absorption | $V_{ESD,CDM}$ | -500 | – | 500 | V | Charge Device Model (CDM)[3)] | P_4.1.8 |
| ESD absorption | $V_{ESD,CDM}$ | -750 | – | 750 | V | Charge Device Model (CDM)[3)] at corner pins | P_4.1.9 |

1) Not subject to production test, specified by design.
2) ESD HBM test according AEC-Q100-002 - JESD22-A114.
3) ESD CDM test according ESDA STM5.3.1.

**Notes**

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

## 3.2 Functional range

**Table 2 Functional range**

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Input voltage | $V_I$ | 5.5 | – | 42 | V | – | P_4.2.1 |
| Output capacitor's requirements for stability | $C_Q$ | 22 | – | – | µF | –[1)] | P_4.2.2 |
| Output capacitor's requirements for stability | $ESR(C_Q)$ | – | – | 3 | Ω | –[2)] | P_4.2.3 |
| Junction temperature | $T_j$ | -40 | – | 150 | °C | – | P_4.2.4 |

1) The minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 30%.
2) Relevant ESR value at $f$ = 10 kHz.

*Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.*

## 3.3 Thermal resistance

**Table 3 Thermal resistance**

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **TLE42754D (PG-TO252-5)** | | | | | | | |
| Junction to case[1)] | $R_{thJC}$ | – | 3.7 | – | K/W | – | P_4.3.1 |
| Junction to ambient[1)] | $R_{thJA}$ | – | 27 | – | K/W | FR4 2s2p board[2)] | P_4.3.2 |
| Junction to ambient[1)] | $R_{thJA}$ | – | 110 | – | K/W | FR4 1s0p board, footprint only[3)] | P_4.3.3 |
| Junction to ambient[1)] | $R_{thJA}$ | – | 57 | – | K/W | FR4 1s0p board, 300 mm$^2$ heatsink area on PCB[3)] | P_4.3.4 |
| Junction to ambient[1)] | $R_{thJA}$ | – | 42 | – | K/W | FR4 1s0p board, 600 mm$^2$ heatsink area on PCB[3)] | P_4.3.5 |
| **TLE42754G (PG-TO263-5)** | | | | | | | |
| Junction to case[1)] | $R_{thJC}$ | – | 3.7 | – | K/W | – | P_4.3.6 |
| Junction to ambient[1)] | $R_{thJA}$ | – | 22 | – | K/W | FR4 2s2p board[2)] | P_4.3.7 |
| Junction to ambient[1)] | $R_{thJA}$ | – | 70 | – | K/W | FR4 1s0p board, footprint only[3)] | P_4.3.8 |
| Junction to ambient[1)] | $R_{thJA}$ | – | 42 | – | K/W | FR4 1s0p board, 300 mm$^2$ heatsink area on PCB[3)] | P_4.3.9 |
| Junction to ambient[1)] | $R_{thJA}$ | – | 33 | – | K/W | FR4 1s0p board, 600 mm$^2$ heatsink area on PCB[3)] | P_4.3.10 |
| **TLE42754E (PG-SSOP-14 exposed pad)** | | | | | | | |
| Junction to case[1)] | $R_{thJC}$ | – | 7 | – | K/W | – | P_4.3.11 |
| Junction to ambient[1)] | $R_{thJA}$ | – | 43 | – | K/W | FR4 2s2p board[2)] | P_4.3.12 |
| Junction to ambient[1)] | $R_{thJA}$ | – | 120 | – | K/W | FR4 1s0p board, footprint only[3)] | P_4.3.13 |
| Junction to ambient[1)] | $R_{thJA}$ | – | 59 | – | K/W | FR4 1s0p board, 300 mm$^2$ heatsink area on PCB[3)] | P_4.3.14 |
| Junction to ambient[1)] | $R_{thJA}$ | – | 49 | – | K/W | FR4 1s0p board, 600 mm$^2$ heatsink area on PCB[3)] | P_4.3.15 |

1) Not subject to production test, specified by design.

2) Specified $R_{thJA}$ value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm$^3$ board with 2 inner copper layers (2 × 70 µm Cu, 2 × 35µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

3) Specified $R_{thJA}$ value is according to JEDEC JESD 51-3 at natural convection on FR4 1s0p board; The Product (Chip+Package) was simulated on a 76.2 × 114.3 × 1.5 mm$^3$ board with 1 copper layer (1 × 70 µm Cu).

# 4 Block description and electrical characteristics

## 4.1 Voltage regulator

The output voltage $V_Q$ is controlled by comparing a portion of it to an internal reference and driving a PNP pass transistor accordingly. The control loop stability depends on the output capacitor $C_Q$, the load current, the chip temperature and the poles/zeros introduced by the integrated circuit. To ensure stable operation, the output capacitor's capacitance and its equivalent series resistor ESR requirements given in the table **"Functional range" on Page 8** have to be maintained. For details see also the typical performance graph **"Output capacitor series resistor ESR(CQ) versus output current IQ" on Page 13**. As the output capacitor also has to buffer load steps it should be sized according to the application's needs.

An input capacitor $C_I$ is strongly recommended to compensate line influences. Connect the capacitors close to the component's terminals.

A protection circuitry prevent the IC as well as the application from destruction in case of catastrophic events. These safeguards contain an output current limitation, a reverse polarity protection as well as a thermal shutdown in case of overtemperature.

In order to avoid excessive power dissipation that could never be handled by the pass element and the package, the maximum output current is decreased at input voltages above $V_I$ = 28 V.

The thermal shutdown circuit prevents the IC from immediate destruction under fault conditions (e.g. output continuously short-circuited) by switching off the power stage. After the chip has cooled down, the regulator restarts. This leads to an oscillatory behaviour of the output voltage until the fault is removed. However, junction temperatures above 150°C are outside the maximum ratings and therefore significantly reduce the IC's lifetime.

The TLE42754 allows a negative supply voltage. In this fault condition, small currents are flowing into the IC, increasing its junction temperature. This has to be considered for the thermal design, respecting that the thermal protection circuit is not operating during reverse polarity conditions.

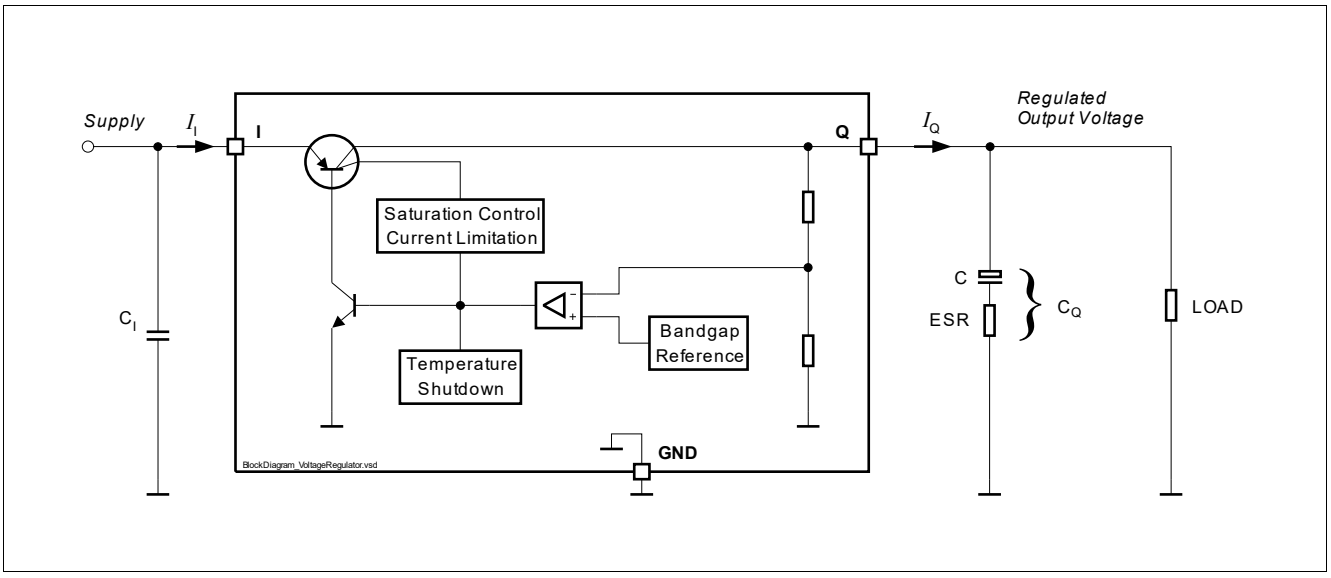



**Figure 4 Voltage regulator**

### Table 4 Electrical characteristics voltage regulator

$V_I$ = 13.5 V, $T_j$ = -40°C to 150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

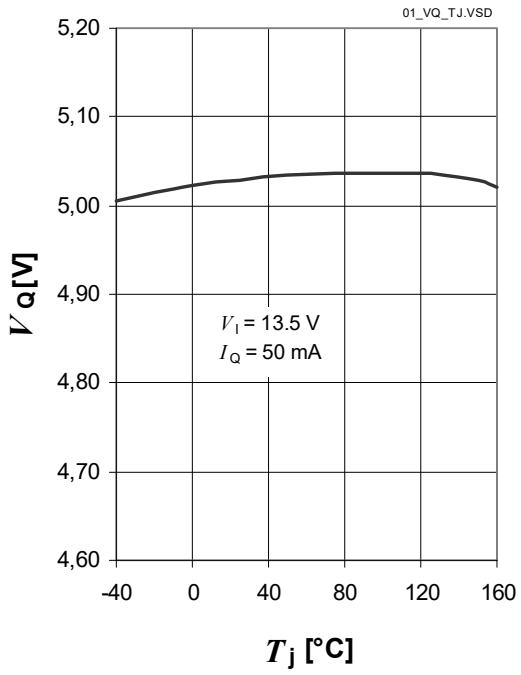
| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Output voltage | $V_Q$ | 4.9 | 5.0 | 5.1 | V | 1 mA < $I_Q$ < 450 mA<br>9 V < $V_I$ < 28 V | P_5.1.1 |
| Output voltage | $V_Q$ | 4.9 | 5.0 | 5.1 | V | 1 mA < $I_Q$ < 400 mA<br>6 V < $V_I$ < 28 V | P_5.1.2 |
| Output voltage | $V_Q$ | 4.9 | 5.0 | 5.1 | V | 1 mA < $I_Q$ < 200 mA<br>6 V < $V_I$ < 40 V | P_5.1.3 |
| Output current limitation | $I_{Q,max}$ | 450 | – | 1100 | mA | $V_Q$ = 4.8V | P_5.1.4 |
| Load regulation steady-state | $\Delta V_{Q,load}$ | -30 | -15 | – | mV | $I_Q$ = 5 mA to 400 mA<br>$V_I$ = 8 V | P_5.1.5 |
| Line regulation steady-state | $\Delta V_{Q,line}$ | – | 5 | 15 | mV | $V_I$ = 8 V to 32 V<br>$I_Q$ = 5 mA | P_5.1.6 |
| Dropout voltage[1)]<br>$V_{dr} = V_I - V_Q$ | $V_{dr}$ | – | 250 | 500 | mV | $I_Q$ = 300 mA | P_5.1.7 |
| Power supply ripple rejection[2)] | *PSRR* | – | 60 | – | dB | $f_{ripple}$ = 100 Hz<br>$V_{ripple}$ = 0.5 Vpp | P_5.1.8 |
| Temperature output voltage drift | $\Delta V_Q/\Delta T$ | – | 0.5 | – | mV/K | – | P_5.1.9 |
| Overtemperature shutdown threshold | $T_{j,sd}$ | 151 | – | 200 | °C | $T_j$ increasing[2)] | P_5.1.10 |
| Overtemperature shutdown threshold hysteresis | $T_{j,sdh}$ | – | 20 | – | °C | $T_j$ decreasing[2)] | P_5.1.11 |

1) Measured when the output voltage $V_Q$ has dropped 100 mV from the nominal value obtained at $V_I$ = 13.5 V.

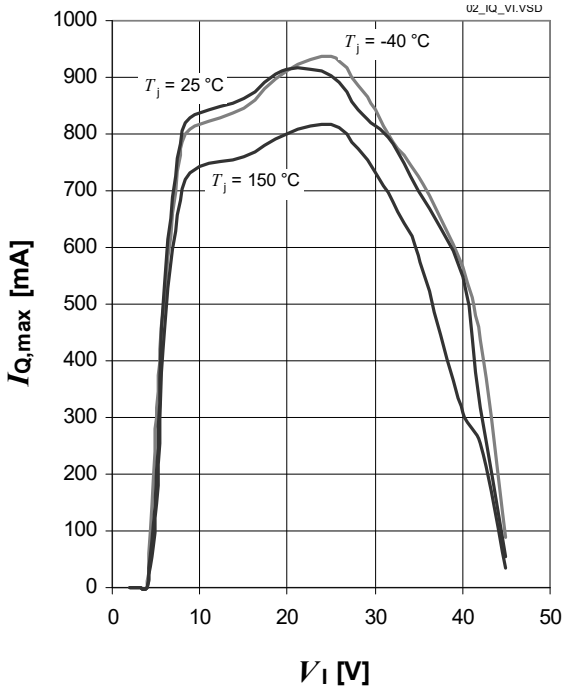
2) Not subject to production test, specified by design.

## Typical performance characteristics voltage regulator

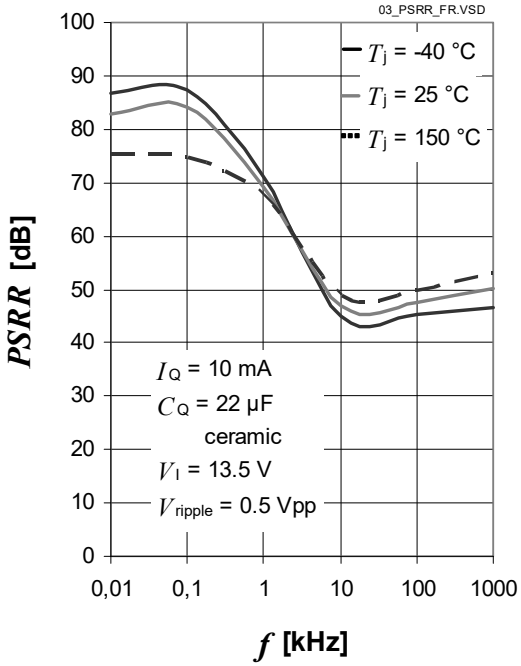
### Output voltage $V_Q$ versus junction temperature $T_j$



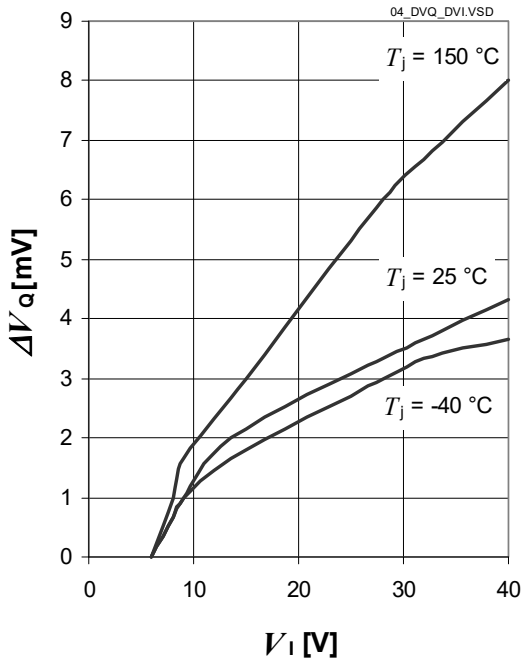

### Output current limitation $I_{Q,max}$ versus input voltage $V_I$



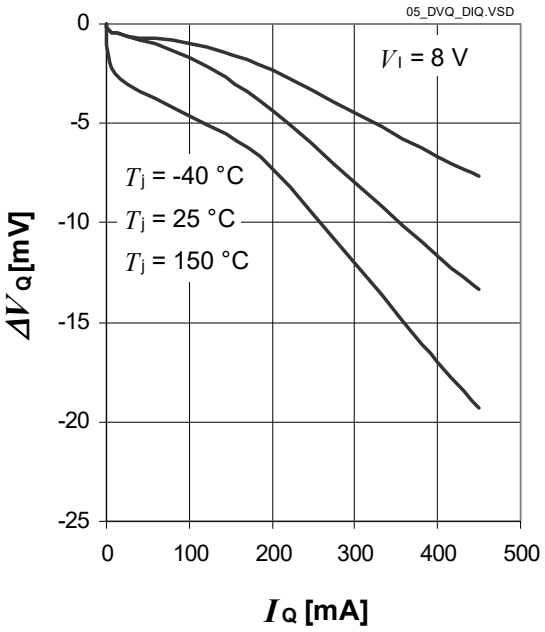

### Power supply ripple rejection *PSRR* versus ripple frequency $f_r$



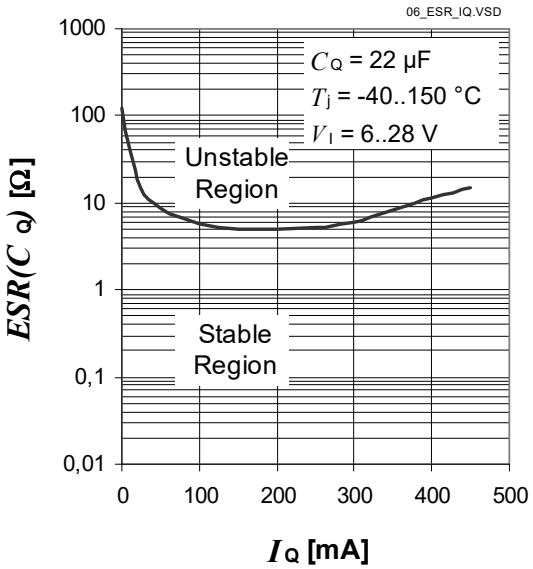

### Line regulation $\Delta V_{Q,line}$ versus input voltage change $\Delta V_I$



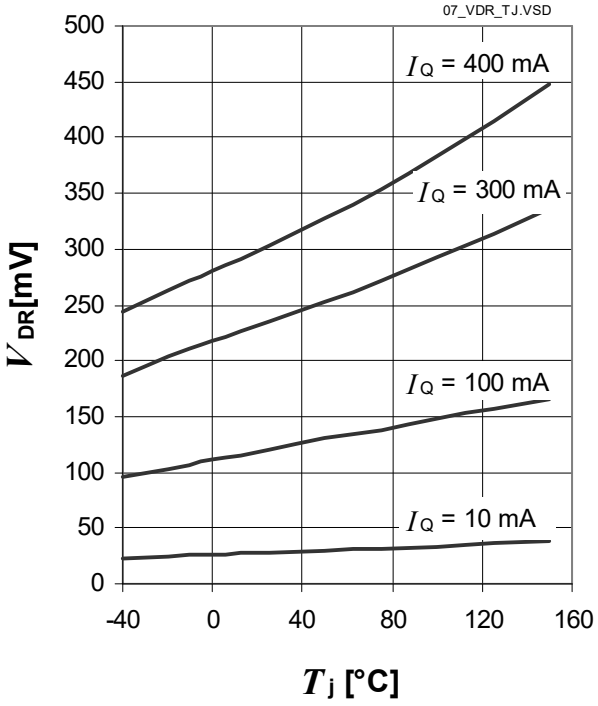
### Load regulation $\Delta V_{Q,load}$ versus output current change $\Delta I_Q$




### Output capacitor series resistor $ESR(C_Q)$ versus output current $I_Q$




### Dropout voltage $V_{dr}$ versus junction temperature $T_j$



## 4.2 Current consumption

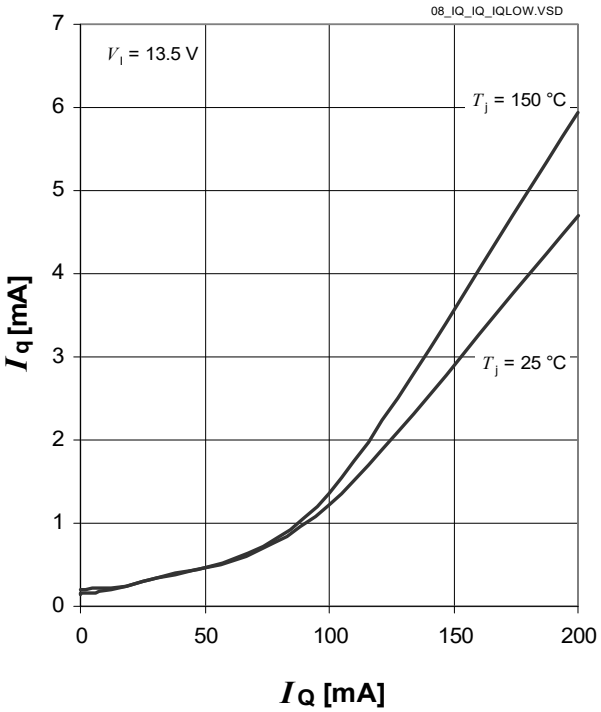
**Table 5 Electrical characteristics current consumption**

$V_I$ = 13.5 V, $T_j$ = -40°C to 150°C, positive current flowing into pin (unless otherwise specified)

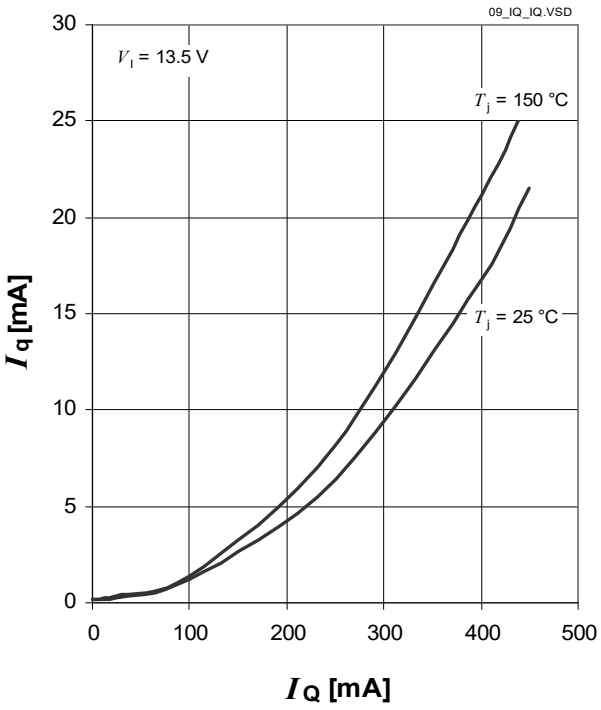
| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Current consumption $I_q = I_I - I_Q$ | $I_q$ | – | 150 | 200 | µA | $I_Q$ = 1 mA<br>$T_j$ = 25°C | P_5.2.1 |
| Current consumption $I_q = I_I - I_Q$ | $I_q$ | – | 150 | 220 | µA | $I_Q$ = 1 mA<br>$T_j$ = 85°C | P_5.2.2 |
| Current consumption $I_q = I_I - I_Q$ | $I_q$ | – | 5 | 10 | mA | $I_Q$ = 250 mA | P_5.2.3 |
| Current consumption $I_q = I_I - I_Q$ | $I_q$ | – | 15 | 25 | mA | $I_Q$ = 400 mA | P_5.2.4 |

## Typical performance characteristics current consumption

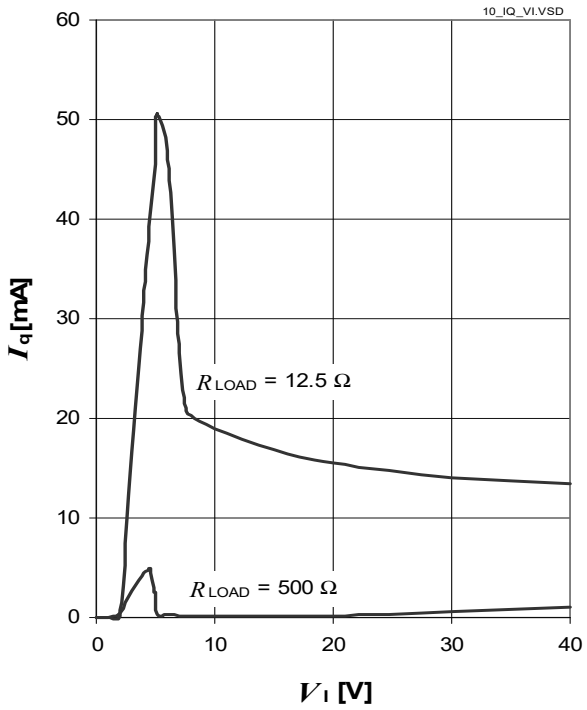
### Current consumption $I_q$ versus output current $I_Q$ ($I_Q$ low)




### Current consumption $I_q$ versus output current $I_Q$




### Current consumption $I_q$ versus input voltage $V_I$



## 4.3 Reset function

The reset function provides several features:

### Output undervoltage reset

An output undervoltage condition is indicated by setting the Reset Output RO to “low”. This signal might be used to reset a microcontroller during low supply voltage.

### Power-on reset delay time

The power-on reset delay time *t*rd allows a microcontoller and oscillator to start up. This delay time is the time frame from exceeding the reset switching threshold $V_{RT}$ until the reset is released by switching the reset output “RO” from “low” to “high”. The power-on reset delay time $t_{rd}$ is defined by an external delay capacitor $C_D$ connected to pin D charged by the delay capacitor charge current $I_{D,ch}$ starting from $V_D$ = 0 V.

If the application needs a power-on reset delay time $t_{rd}$ different from the value given in **Power on reset delay time**, the delay capacitor’s value can be derived from the specified values in **Power on reset delay time** and the desired power-on delay time:

(4.1)

$$C_D = \frac{t_{rd,new}}{t_{rd}} \times 47nF$$

with

- $C_D$: capacitance of the delay capacitor to be chosen
- $t_{rd,new}$: desired power-on reset delay time
- $t_{rd}$: power-on reset delay time specified in this datasheet

For a precise calculation also take the delay capacitor’s tolerance into consideration.

### Reset reaction time

The reset reaction time avoids that short undervoltage spikes trigger an unwanted reset “low” signal. The reset reaction rime $t_{rr}$ considers the internal reaction time $t_{rr,int}$ and the discharge time $t_{rr,d}$ defined by the external delay capacitor $C_D$ (see typical performance graph for details). Hence, the total reset reaction time becomes:

(4.2)

$$t_{rr} = t_{rd,int} + t_{rr,d}$$

with

- $t_{rr}$: reset reaction time
- $t_{rr,int}$: internal reset reaction time
- $t_{rr,d}$: reset discharge

### Reset Output pull-up resistor $R_{RO}$

The Reset Output RO is an open collector output requiring an external pull-up resistor to a voltage $V_{IO}$, e.g. $V_Q$. In **Table 6 "Electrical characteristics reset function" on Page 19** a minimum value for the external resistor $R_{RO}$ is given for the case it is connected to $V_Q$ or to a voltage $V_{IO} < V_Q$. If the pull-up resistor shall be connected to a voltage $V_{IO} > V_Q$, use the following formula:

(4.3)

$$R_{RO} = \frac{5k\Omega}{V_Q} \times V_{IO}$$

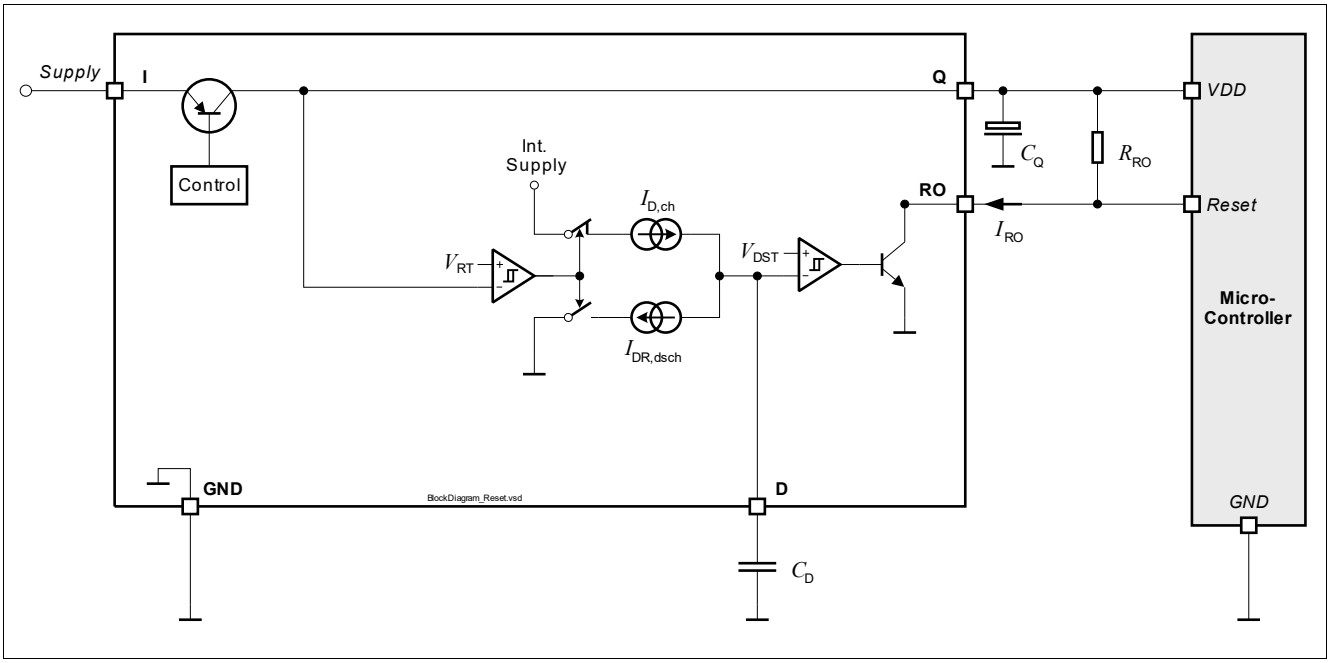



**Figure 5 Block diagram reset function**

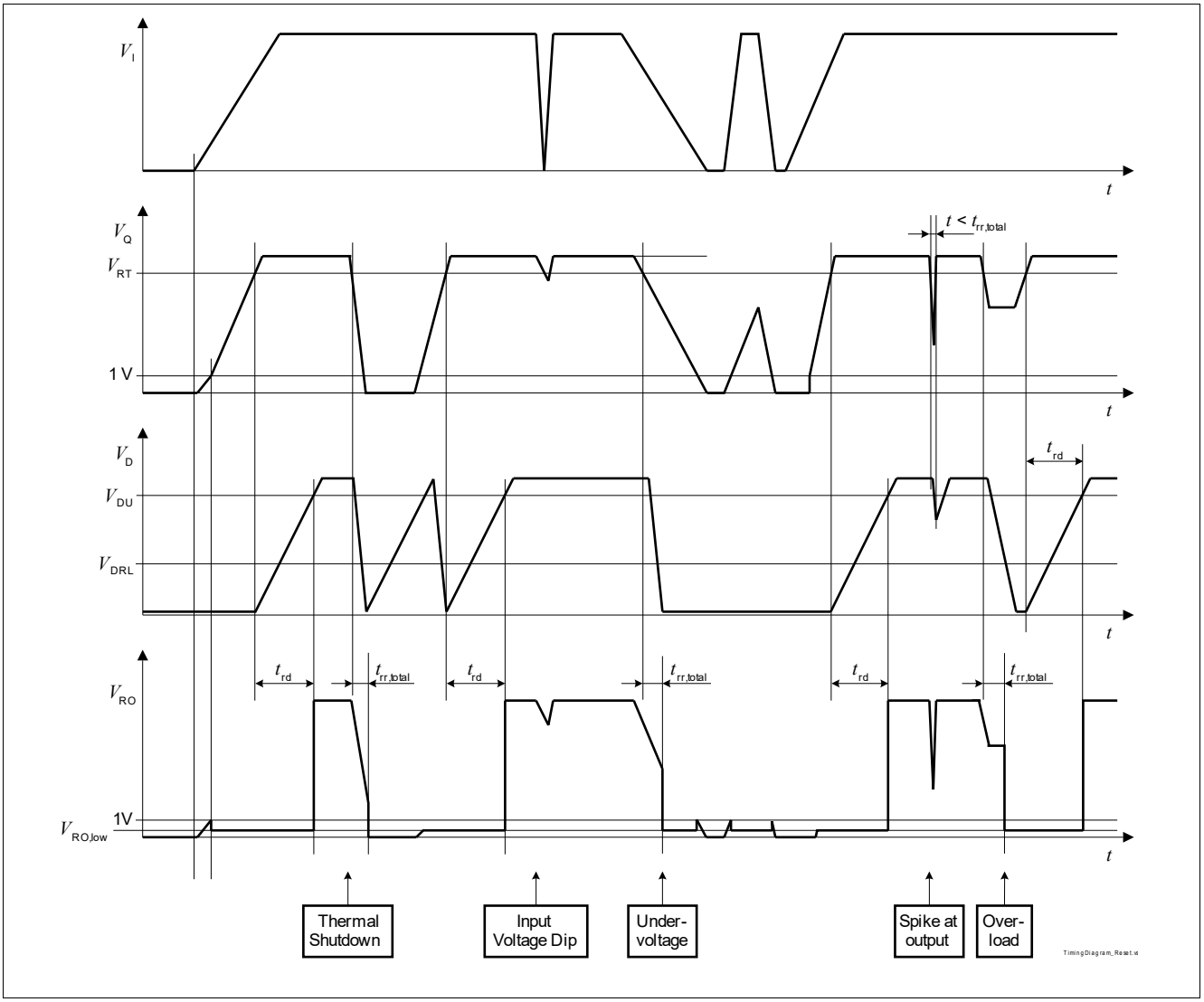



**Figure 6 Timing diagram reset**

### Table 6 Electrical characteristics reset function

$V_I$ = 13.5 V, $T_j$ = -40°C to 150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

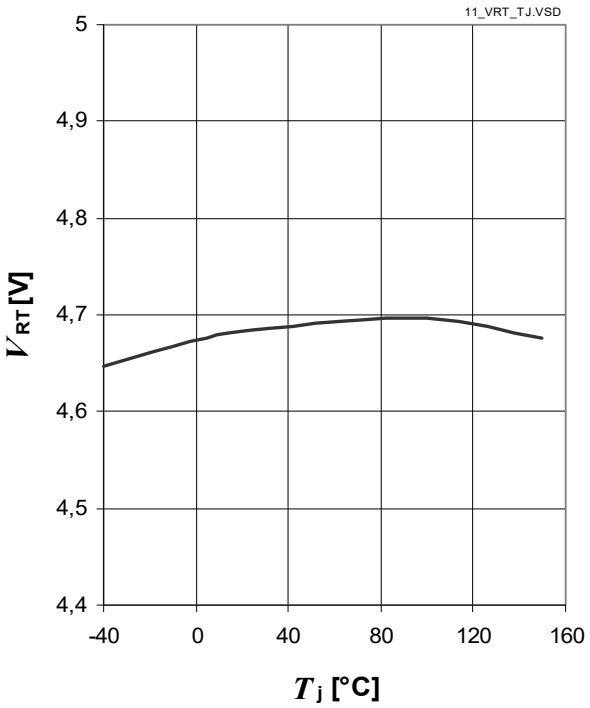
| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Output undervoltage reset** | | | | | | | |
| Output undervoltage reset switching thresholds | $V_{RT}$ | 4.5 | 4.65 | 4.8 | V | $V_Q$ decreasing | P_5.3.1 |
| **Reset output RO** | | | | | | | |
| Reset output low voltage | $V_{RO,low}$ | – | 0.2 | 0.4 | V | $V_Q$ = 1 V to $V_{RT}$ ; $I_{RO}$ = 0.2 mA | P_5.3.2 |
| Reset output sink current capability | $I_{RO,max}$ | 0.2 | – | – | mA | $V_Q$ = 1 V to $V_{RT}$ ; $V_{RO}$ = 5 V | P_5.3.3 |
| Reset output leakage current | $I_{RO,leak}$ | – | 0 | 10 | µA | $V_{RO}$ = 5 V | P_5.3.4 |
| Reset output external pull-up resistor to $V_Q$ | $R_{RO}$ | 5 | – | – | kΩ | $V_Q$ = 1 V to $V_{RT}$ ; $V_{RO}$ ≤ 0.4 V | P_5.3.5 |
| **Reset delay timing** | | | | | | | |
| Power on reset delay time | $t_{rd}$ | 10 | 16 | 22 | ms | $C_D$ = 47 nF | P_5.3.6 |
| Upper delay switching threshold | $V_{DU}$ | – | 1.8 | – | V | – | P_5.3.7 |
| Lower delay switching threshold | $V_{DRL}$ | – | 0.65 | – | V | – | P_5.3.8 |
| Delay capacitor charge current | $I_{D,ch}$ | – | 5.5 | – | µA | $V_D$ = 1 V | P_5.3.9 |
| Delay capacitor reset discharge current | $I_{D,dch}$ | – | 100 | – | mA | $V_D$ = 1 V | P_5.3.10 |
| Delay capacitor discharge time | $t_{rr,d}$ | – | 0.5 | 1 | µs | Calculated Value: $t_{rr,d}$ = $C_D \times (V_{DU} - V_{DRL}) / I_{D,dch}$ $C_D$ = 47 nF | P_5.3.11 |
| Internal reset reaction Time | $t_{rr,int}$ | – | 4 | 7 | µs | $C_D$ = 0 nF[1)] | P_5.3.12 |
| Reset reaction time | $t_{rr,total}$ | – | 4.5 | 8 | µs | Calculated Value: $t_{rr,total} = t_{rr,int} + t_{rr,d}$ $C_D$= 47 nF | P_5.3.13 |

1) Parameter not subject to production test; specified by design.

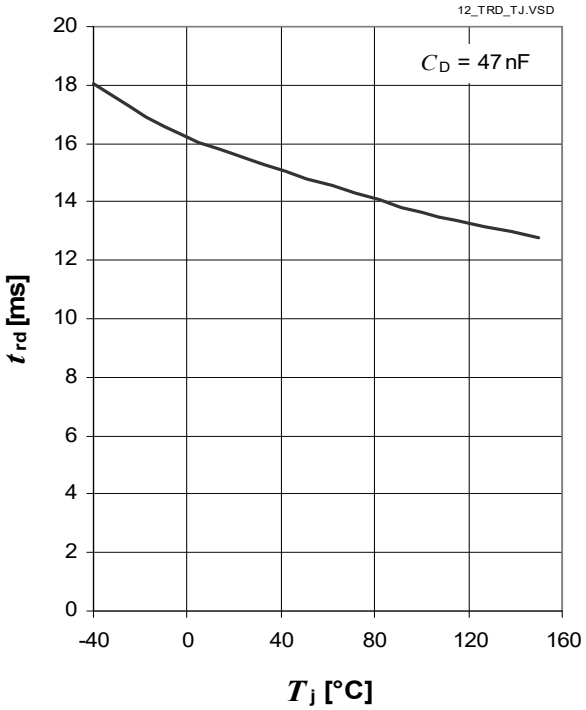
## Block description and electrical characteristics

### Typical performance characteristics

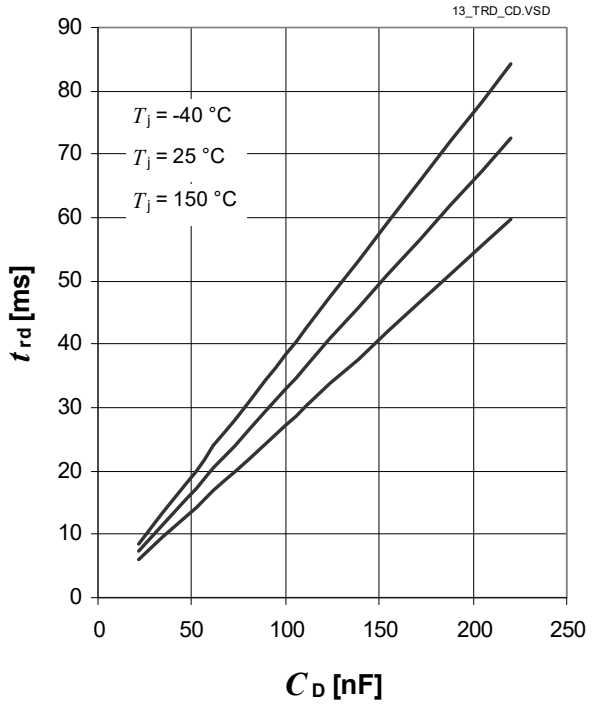
**Undervoltage reset switching threshold $V_{RT}$ versus junction temperature $T_j$**



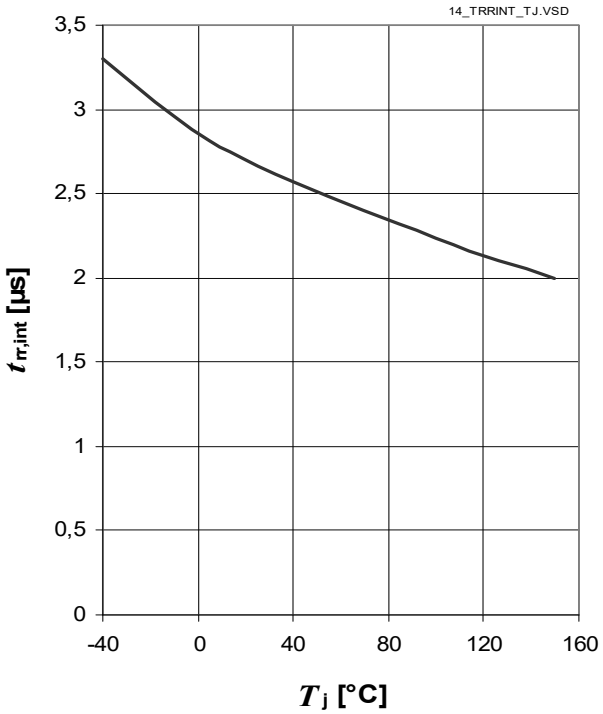

**Power on reset delay time $t_{rd}$ versus junction temperature $T_j$**



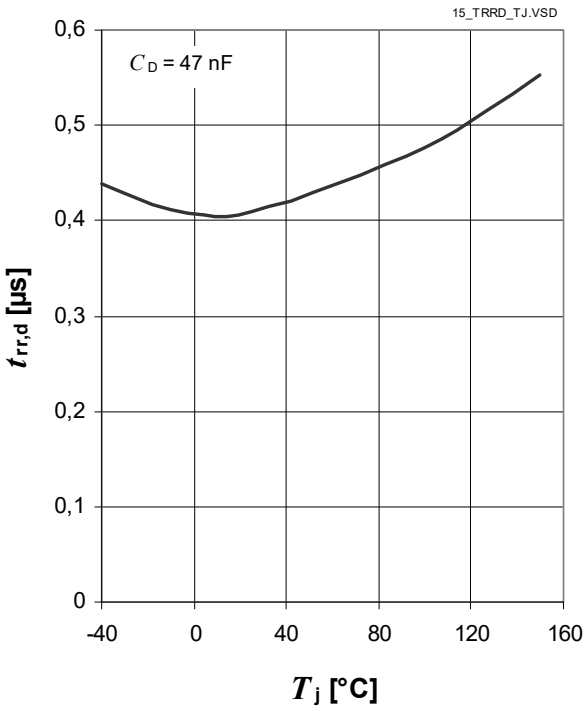

**Power on reset delay time $t_{rd}$ versus capacitance $C_D$**




**Internal reset reaction time $t_{rr,int}$ versus junction temperature $T_j$**



### Delay capacitor discharge time $t_{rr,d}$ versus junction temperature $T_j$



# 5 Application information

*Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.*

## 5.1 Application diagram

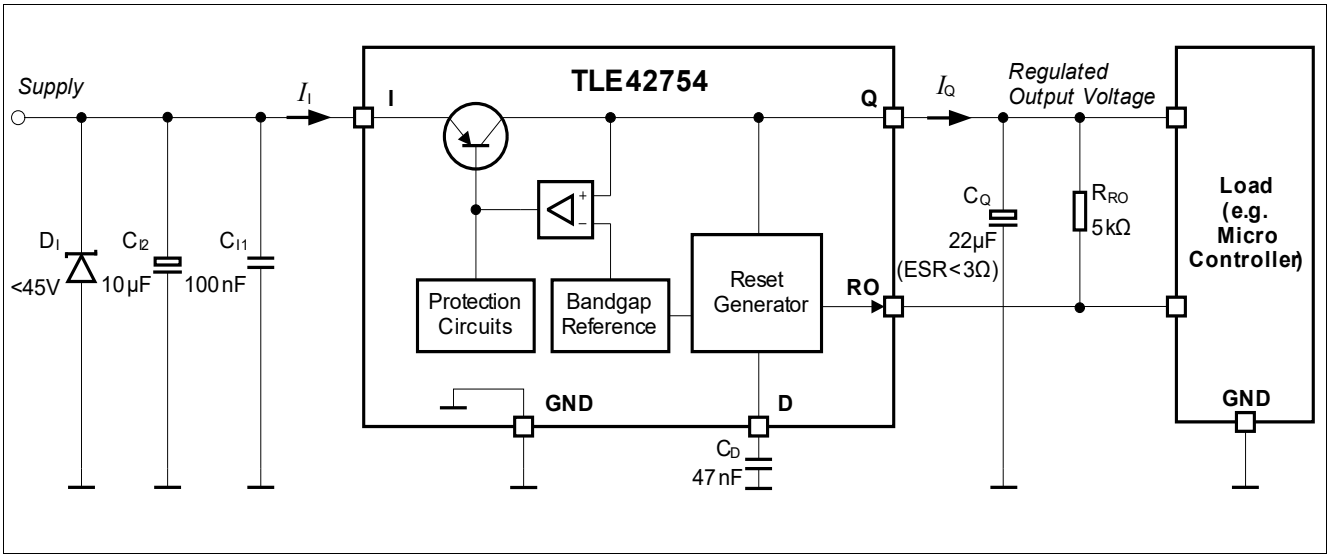



**Figure 7 Application diagram**

## 5.2 Selection of external components

### 5.2.1 Input pin

The typical input circuitry for a linear voltage regulator is shown in the application diagram above.

A ceramic capacitor at the input, in the range of 100 nF to 470 nF, is recommended to filter out the high frequency disturbances imposed by the line e.g. ISO pulses 3a/b. This capacitor must be placed very close to the input pin of the linear voltage regulator on the PCB.

An aluminum electrolytic capacitor in the range of 10 µF to 470 µF is recommended as an input buffer to smooth out high energy pulses, such as ISO pulse 2a. This capacitor should be placed close to the input pin of the linear voltage regulator on the PCB.

An overvoltage suppressor diode can be used to further suppress any high voltage beyond the maximum rating of the linear voltage regulator and protect the device against any damage due to over-voltage.

The external components at the input are not mandatory for the operation of the voltage regulator, but they are recommended in case of possible external disturbances.

### 5.2.2 Output pin

An output capacitor is mandatory for the stability of linear voltage regulators.

The requirement to the output capacitor is given in **“Functional range” on Page 8**. The graph **“Output capacitor series resistor ESR(CQ) versus output current IQ” on Page 13** shows the stable operation range of the device.

TLE42754 is designed to be stable with extremely low ESR capacitors. According to the automotive environment, ceramic capacitors with X5R or X7R dielectrics are recommended.

The output capacitor should be placed as close as possible to the regulator's output and GND pins and on the same side of the PCB as the regulator itself.

In case of rapid transients of input voltage or load current, the capacitance should be dimensioned in accordance and verified in the real application that the output stability requirements are fulfilled.

## 5.3 Thermal considerations

Knowing the input voltage, the output voltage and the load profile of the application, the total power dissipation can be calculated:

$$P_D = (V_I - V_Q) \times I_Q + V_I \times I_q \quad (5.1)$$

with

- $P_D$: continuous power dissipation
- $V_I$: input voltage
- $V_Q$: output voltage
- $I_Q$: output current
- $I_q$: quiescent current

The maximum acceptable thermal resistance $R_{thJA}$ can then be calculated:

$$R_{thJA,\,max} = \frac{T_{j,\,max} - T_a}{P_D} \quad (5.2)$$

with

- $T_{j,max}$: maximum allowed junction temperature
- $T_a$: ambient temperature

Based on the above calculation the proper PCB type and the necessary heat sink area can be determined with reference to the specification in **"Thermal resistance" on Page 9**.

**Example**

Application conditions:

$V_I$ = 13.5 V

$V_Q$ = 5 V

$I_Q$ = 250 mA

$T_a$ = 85°C

Calculation of $R_{thJA,max}$:

$P_D = (V_I - V_Q) \times I_Q + V_I \times I_q$

= (13.5 V – 5 V) × 250 mA + 13.5 V × 10 mA

= 2.125 W + 0.135 W

= 2.26 W

$R_{thJA,max} = (T_{j,max} - T_a) / P_D$
$= (150°C - 85°C) / 2.26\ W$
$= 28.76\ K/W$

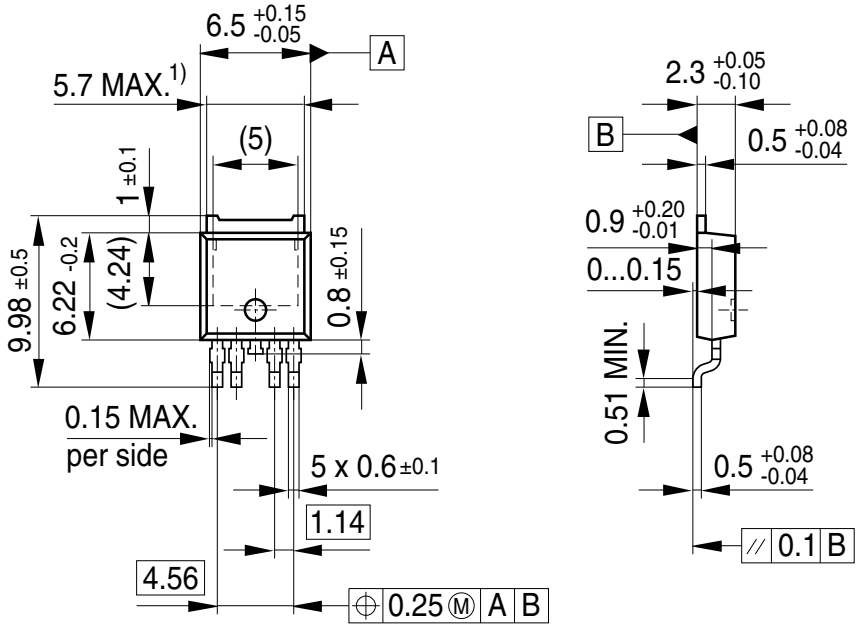
As a result, the PCB design must ensure a thermal resistance $R_{thJA}$ lower than 28.76 K/W. By considering TLE42754G (PG-TO263-5 package) and according to **“Thermal resistance” on Page 9**, only the FR4 2s2p board is applicable.

## 5.4 Reverse polarity protection

TLE42754 is self protected against reverse polarity faults and allows negative supply voltage. External reverse polarity diode is not needed. However, the absolute maximum ratings of the device as specified in **“Absolute maximum ratings” on Page 7** must be kept.

The reverse voltage causes several small currents to flow into the IC hence increasing its junction temperature. As the thermal shut down circuitry does not work in the reverse polarity condition, designers have to consider this in their thermal design.

# 6 Package outlines




1) Includes mold flashes on each side.
All metal surfaces tin plated, except area of cut.

**Figure 8 PG-TO252-5[1)]**

1) Dimensions in mm

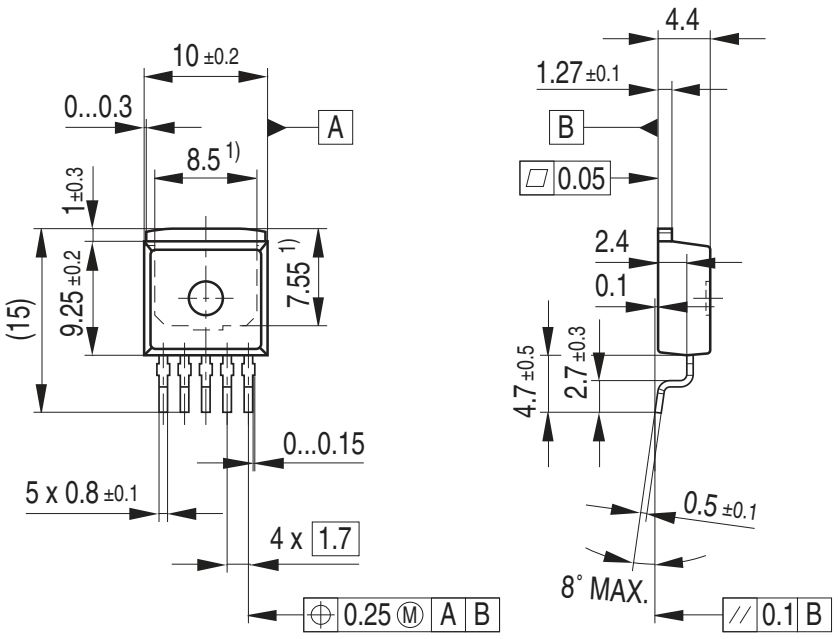



**Figure 9 PG-TO263-5[1)]**

1) Dimensions in mm

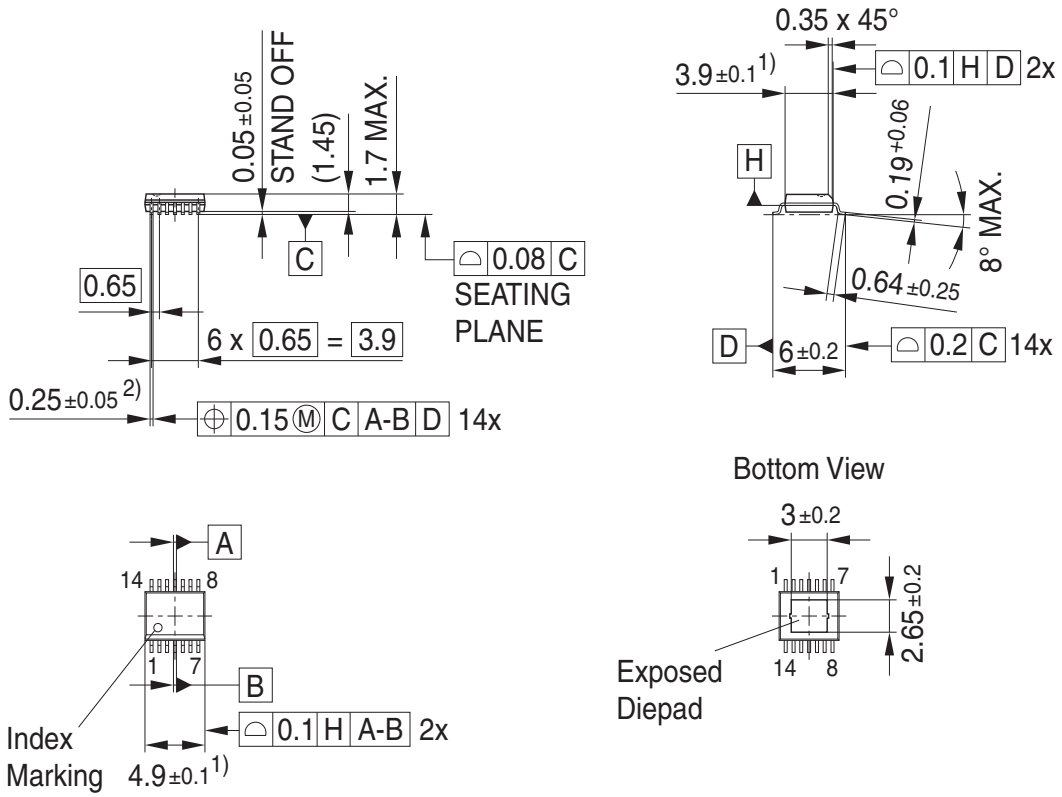



**Figure 10 PG-SSOP-14 exposed pad[1)]**

### Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e. Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

### Further information on packages

**https://www.infineon.com/packages**

1) Dimensions in mm

# 7 Revision history

| Revision | Date | Changes |
|---|---|---|
| 1.3 | 2021-11-25 | Marking changes from TLE42754G to TLE42754<br>Updated layout and structure<br>Editorial changes |
| 1.2 | 2014-07-03 | “Application Information” added<br>PG-SSOP-14 EP package outline updated |
| 1.11 | 2012-01-20 | Condition of Parameter Delay Capacitor Discharge Time, Internal Reset Reaction Time and Reset Reaction Time corrected. Parameters are valid for all package variants. No need to limit the Measurement conditions<br>Coverpage updated |
| 1.1 | 2008-09-24 | Datasheet updated with new package variant in PG-SSOP-14 exposed pad:<br>In “FrontCover” package graphic and sales name with marking added<br>In Table “Thermal Resistance” values for package PG-SSOP-14 exposed pad added<br>In “Package Outlines” Outlines for package PG-SSOP-14 exposed pad added |
| 1.0 | 2008-05-29 | Initial version |

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