5.5V ESD Protection Diodes

Micro−packaged Diodes for ESD Protection

ESDM1051

The ESDM1051 Series is designed to protect voltage sensitive components from ESD. Excellent clamping capability, low leakage, and fast response time provide best in class protection on designs that are exposed to ESD. Because of its small size, it is suited for use in smartphone, smart−watch, or many other portable / wearable applications where board space comes at a premium.

Features

- Low Capacitance (22 pF Typ, I/O to GND)
- Small Body Outline Dimensions − 01005 Size: 0.445 x 0.240 mm
- Protection for the Following IEC Standards:
  IEC 61000−4−2 (Level 4)
- Low ESD Clamping Voltage
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Operating Junction Temperature Range	T_J	−55 to +125	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Lead Solder Temperature − Maximum (10 Seconds)	T_L	260	°C
ESDM1051: IEC 61000−4−2 Contact IEC 61000−4−2 Air	ESD	 ±30 ±30	 kV kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

See Application Note AND8308/D for further description of survivability specs.

ON Semiconductor®

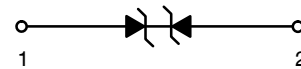**X4DFN2 (01005)**
CASE 718AA

MARKING DIAGRAM

L = Specific Device Code
M = Date Code

PIN CONFIGURATION AND SCHEMATIC

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

March, 2021 − Rev. 0

Publication Order Number:
ESDM1051/D

ESDM1051

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}	I/O Pin to GND			5.5	V
Breakdown Voltage	V_{BR}	I_T = 1 mA, I/O Pin to GND	6.1	6.8	8.2	V
Reverse Leakage Current	I_R	V_{RWM} = 5.5 V, I/O Pin to GND			0.1	μA
Clamping Voltage TLP (Note 1)	V_C	I_{PP} = 8 A } IEC 61000−4−2 Level 2 equivalent (±4 kV Contact, ±8 kV Air)		7.5		V
		I_{PP} = 16 A } IEC 61000−4−2 Level 2 equivalent (±8 kV Contact, ±16 kV Air)		8.4		
Reverse Peak Pulse Current	I_{PP}	IEC61000−4−5 (8x20 μs)	11	13		A
Clamping Voltage	V_C	I_{PP} = 11 A, (8/20 μs pulse)		8.0	8.8	V
Dynamic Resistance	R_{DYN}	100 ns TLP Pulse		0.11		Ω
Junction Capacitance	C_J	V_R = 0 V, f = 1 MHz		22	25	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
1. ANSI/ESD STM5.5.1 − Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model.
   TLP conditions: Z_0 = 50 Ω, t_p = 100 ns, t_r = 1 ns, averaging window; t_1 = 70 ns to t_2 = 90 ns.

ORDERING INFORMATION

Device	Package	Shipping[†]
ESDM1051MX4T5G	X4DFN2 (01005) (Pb−Free)	10,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

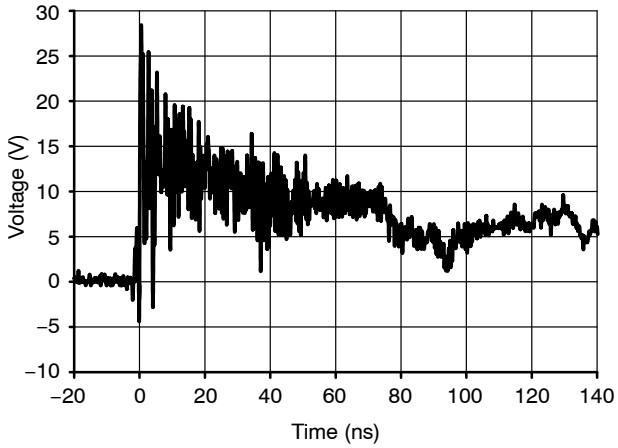# ESDM1051

TYPICAL CHARACTERISTICS

Figure 1. ESD Clamping Voltage
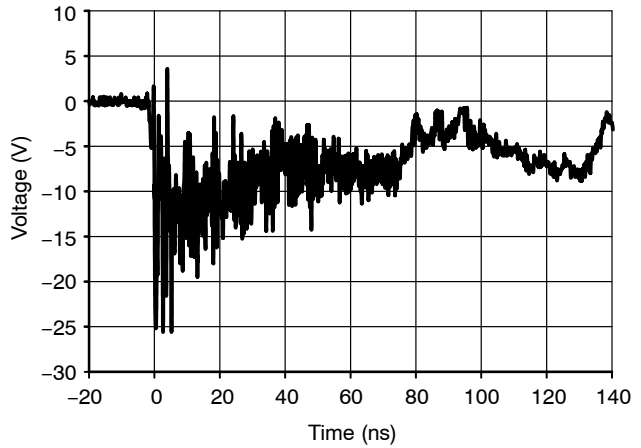Positive 8 kV Contact per IEC61000−4−2

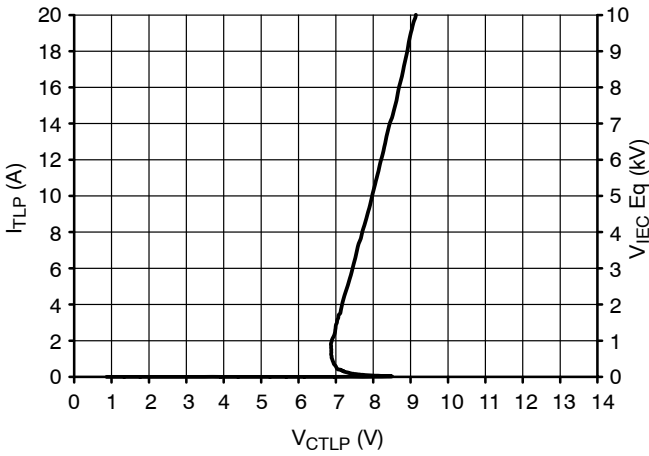Figure 2. ESD Clamping Voltage
Negative 8 kV Contact per IEC61000−4−2
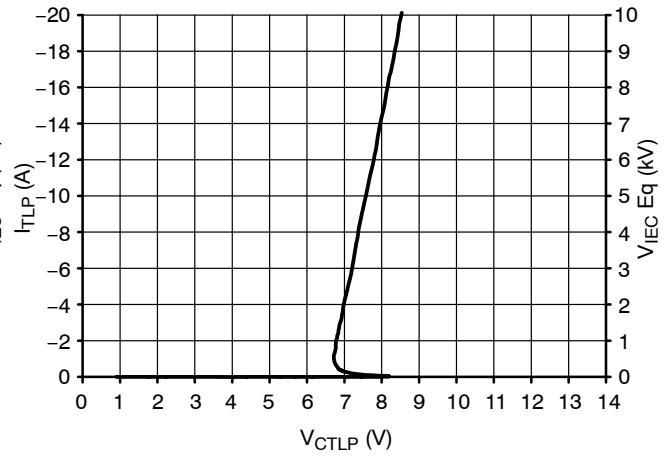

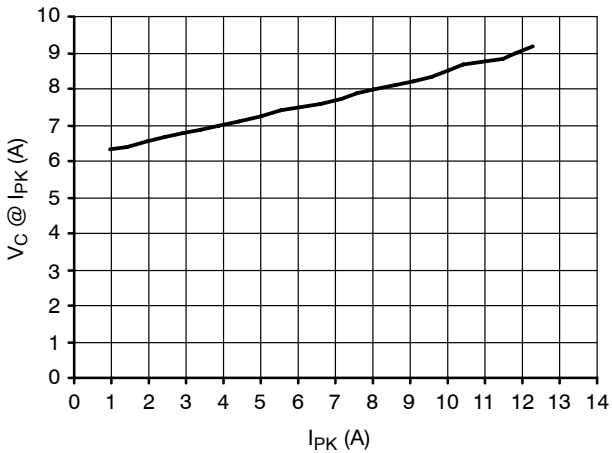Figure 3. Positive TLP I−V Curve

Figure 4. Negative TLP I−V Curve

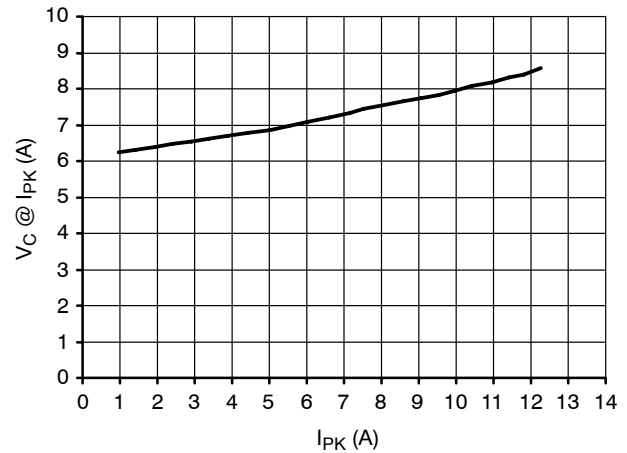Figure 5. Positive Clamping Voltage vs. Peak
Pulse Current (tp = 8/20 μs)

Figure 6. Negative Clamping Voltage vs. Peak
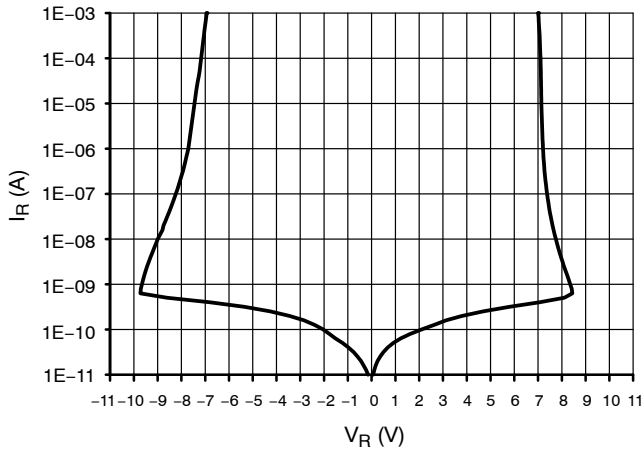Pulse Current (tp = 8/20 μs)
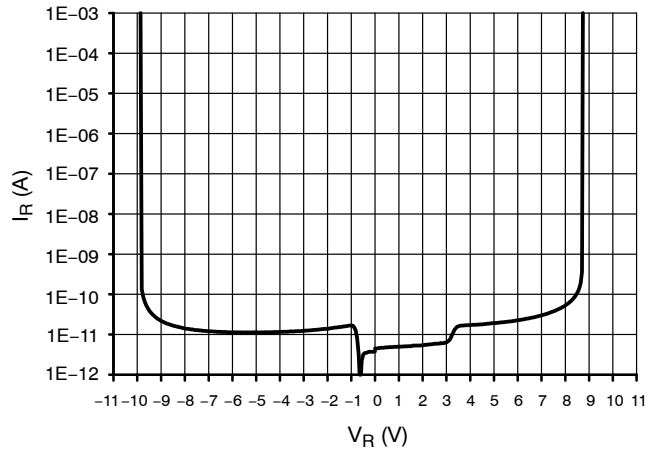
TYPICAL CHARACTERISTICS

Figure 7. Breakdown Voltage

Figure 8. Reverse Leakage Current
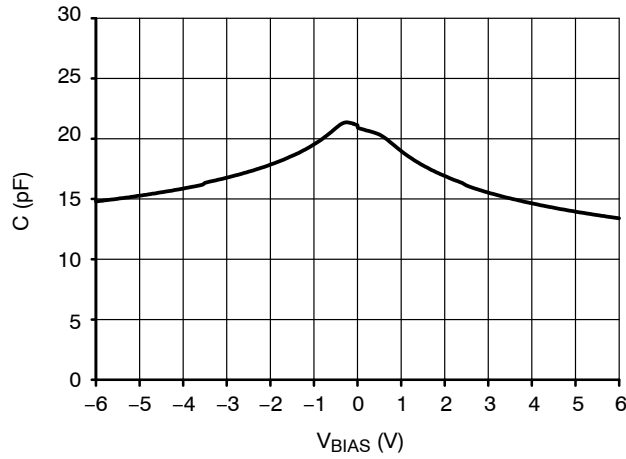
Figure 9. Line Capacitance, f = 1 MHz

Figure 10. Magnitude vs. Frequency

IEC 61000−4−2 Spec.

Level	Test Volt-age (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8
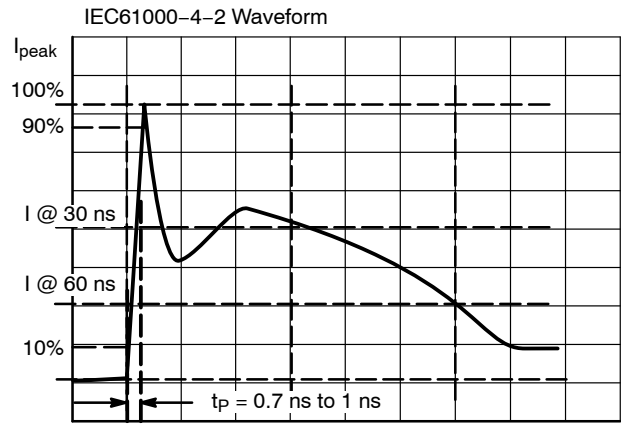
Figure 11. IEC61000−4−2 Spec

Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I−V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 12. TLP I−V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 13 where an 8 kV IEC 61000−4−2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I−V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels.
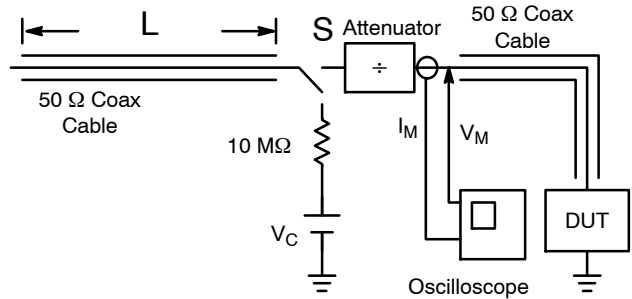
Figure 12. Simplified Schematic of a Typical TLP System
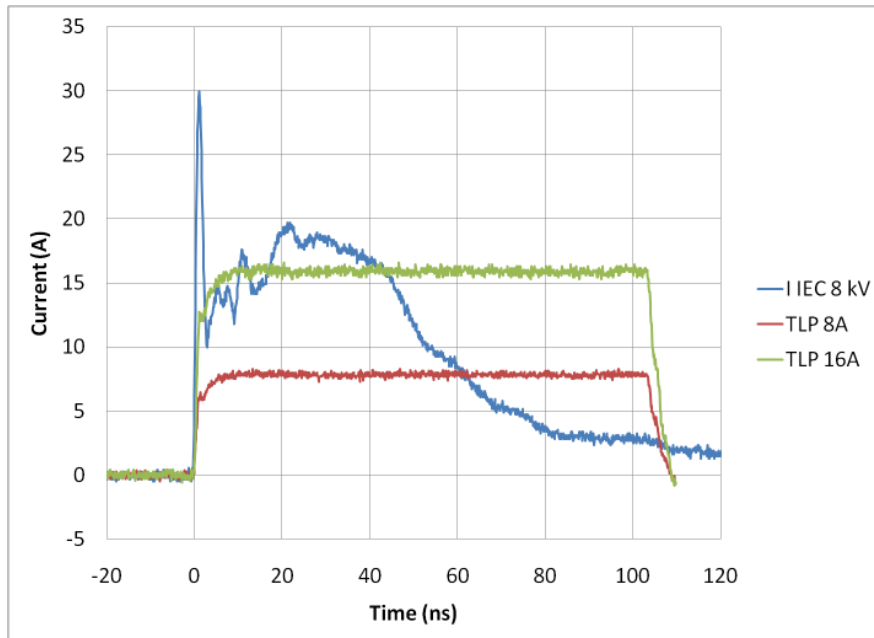
Figure 13. Comparison Between 8 kV IEC 61000−4−2 and 8 A and 16 A TLP Waveforms

X4DFN2, 0.445x0.24, 0.27P
CASE 718AA
ISSUE A

DATE 21 MAR 2017

SCALE 10:1

TOP VIEW

PIN 1 REFERENCE

D → A
B
E

SIDE VIEW

∥ 0.03 C

⌒ 0.03 C

A
A1
C SEATING PLANE

BOTTOM VIEW

e
e/2
2X b
PIN 1
2X L
2X 2

⊕ 0.10 C A B
⊕ 0.05 C   NOTE 3
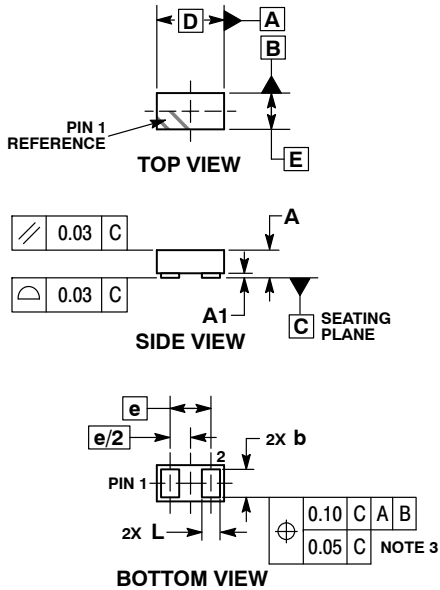
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. EXPOSED COPPER ALLOWED AS SHOWN.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.15	0.18	0.21
A1	---	---	0.03
b	0.170	0.185	0.200
D	0.415	0.445	0.475
E	0.210	0.240	0.270
e	0.270 BSC		
L	0.105	0.120	0.135

GENERIC
MARKING DIAGRAMS*

● X

X
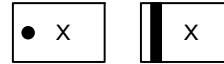
X = Specific Device Code

*This information is generic. Please refer to device data sheet for actual part marking. Some products may not follow the Generic Marking.

RECOMMENDED
MOUNTING FOOTPRINT*

0.27
PITCH
2X 0.21
1
2X 0.13

DIMENSIONS: MILLIMETERS
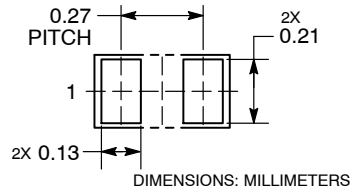
See Application Note AND8398/D for more mounting details

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	X4DFN2, 0.445X0.24, 0.27P		PAGE 1 OF 1

ADDITIONAL INFORMATION

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