ISL70003ASEH

Radiation and SEE Hardened 3V to 13.2V, 9A Buck Regulator

FN8746
Rev.4.01
Dec 12, 2019

The ISL70003ASEH is an improved version of the ISL70003SEH regulator with both tighter load regulation (<0.3% typical) and a higher output current rating of 9A. Operating over an input voltage range of 3.0V to 13.2V with integrated low $r_{DS(ON)}$ MOSFETs makes this monolithic solution highly efficient. Also, a tightly regulated output voltage is possible, which is externally adjustable from 0.6V to ~90% of the input voltage. Continuous output load current capability is 9A for $T_J \leq +125°C$ and 6A for $T_J \leq +150°C$.

The ISL70003ASEH uses voltage mode control architecture with feed-forward and switches at a selectable frequency of 500kHz or 300kHz. Loop compensation is externally adjustable to allow for an optimum balance between stability and output dynamic performance.

The device features two logic-level disable inputs that can be used to inhibit pulses on the phase (LXx) pins to maximize efficiency based on the load current. The ISL70003ASEH also supports DDR applications and contains a buffer amplifier for generating the V_{REF} voltage.

High integration, best-in-class radiation performance and a feature-filled design make the ISL70003ASEH an ideal choice to power many of today's small form-factor applications.

Applications

- FPGA, CPLD, DSP, CPU core, and I/O supply voltages
- DDR memory supply voltages
- Low-voltage, high-density distributed power systems

Related Literature

For a full list of related documents, visit our website:

- ISL70003ASEH device page

Features

- **Acceptance tested to 50krad(Si) (LDR) wafer-by-wafer**
- **±1% reference voltage over line, temperature, and radiation**
- **Integrated MOSFETs 31mΩ PFET/21mΩ NFET**
  - **95% peak efficiency**
- **Externally adjustable loop compensation**
- **Supports DDR applications (V_{TT} tracks $V_{DDQ}/2$)**
  - **Buffer amplifier for generating V_{REF} voltage**
  - **3A current sinking capability**
- Grounded lid eliminates charge build up
- IMON pin for output current monitoring
- Adjustable analog soft-start
- Diode emulation for increased efficiency at light loads
- 500kHz or 300kHz operating frequency
- Monotonic start-up into prebiased load
- Full military temperature range operation
  - T_A = -55°C to +125°C
  - T_J = -55°C to +150°C
- Radiation Acceptance (See TID Report)
  - High dose rate (50-300rad(Si)/s). . . . . 100krad(Si)
  - Low dose rate (0.01rad(Si)/s) . . . . . 50krad(Si)
- SEE hardness (See SEE report)
  - SEB and SEL LET_{TH} . . . . . 86.4MeV•cm^2/mg
  - SET at LET 86.4MeV•cm^2/mg . . . . . <±3% ΔV_{OUT}
  - SEFI LET_{TH} . . . . . 60MeV•cm^2/mg
- Electrically screened to DLA SMD 5962-14203

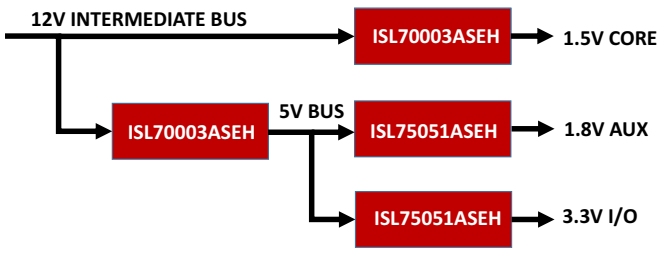

FIGURE 1. POWER DISTRIBUTION SOLUTION FOR RAD HARD LOW POWER FPGAs

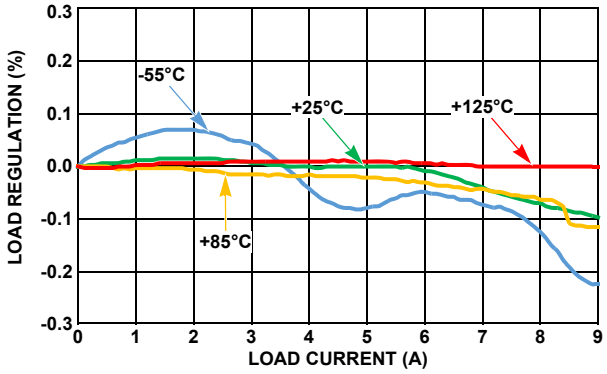

FIGURE 2. TYPICAL LOAD REGULATION, V_{IN} = 12V, V_{OUT} = 3.3V, f_{SW} = 500kHz

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Functional Block Diagram

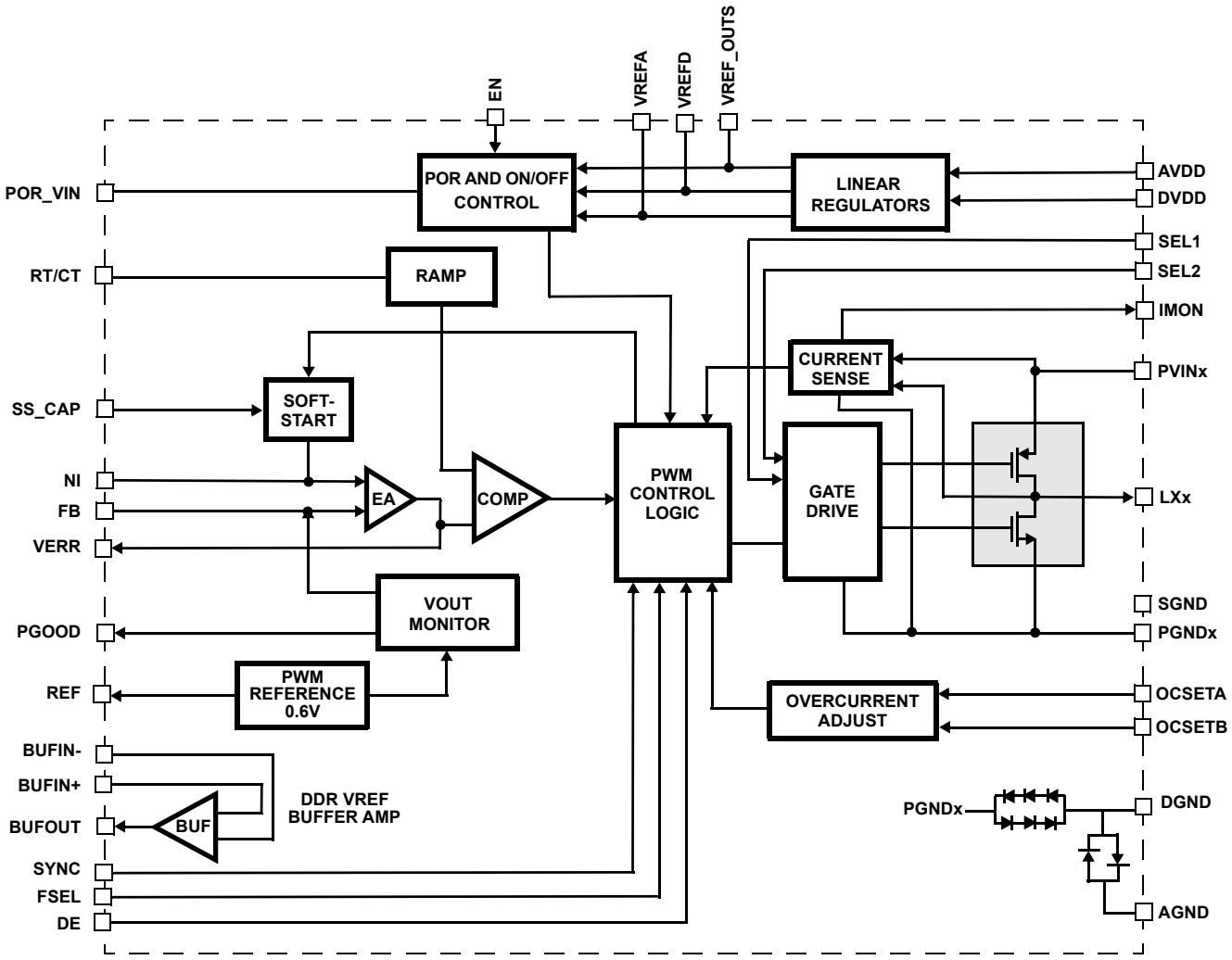


FIGURE 3. BLOCK DIAGRAM

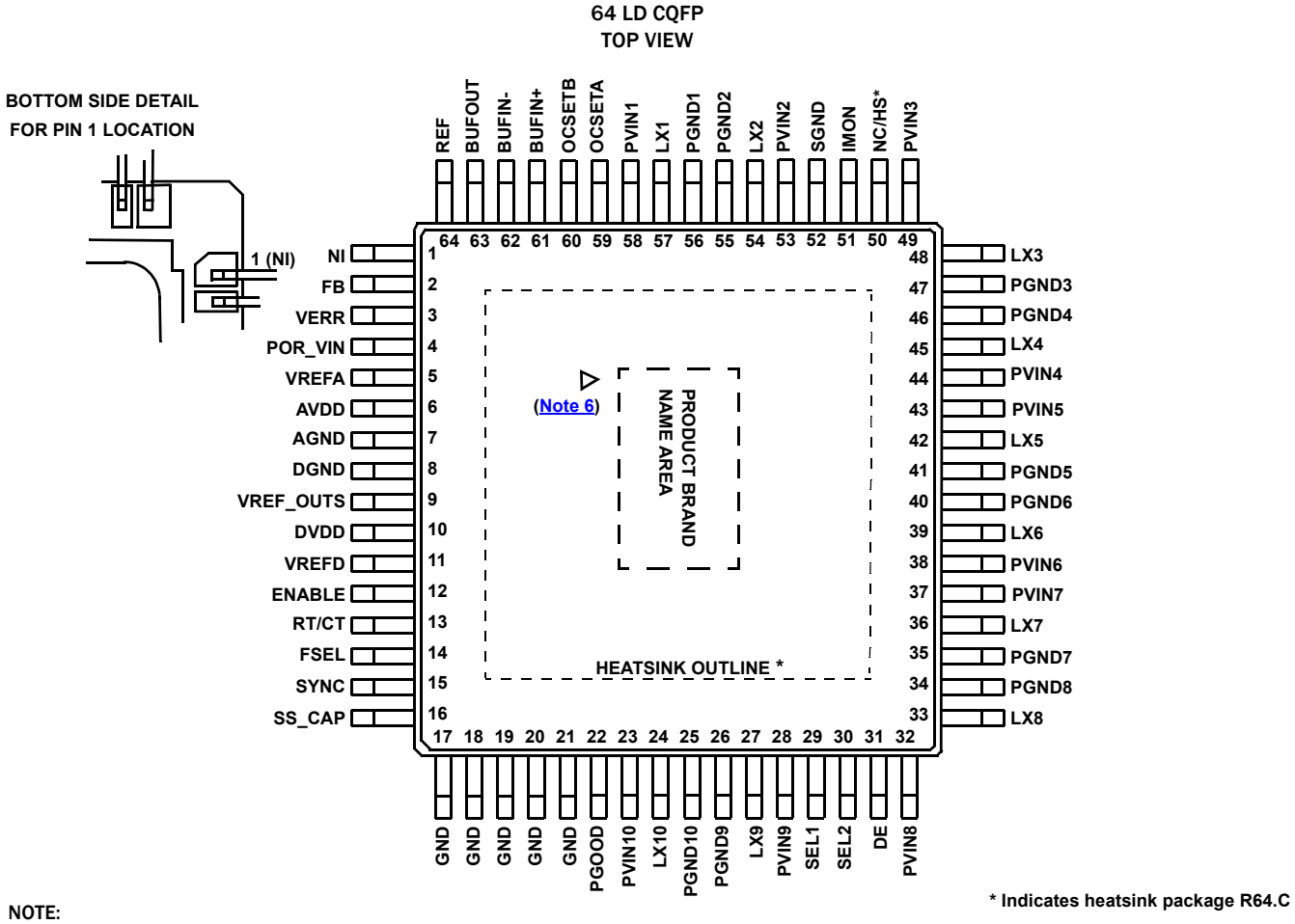
Ordering Information

ORDERING SMD NUMBER (Note 1)	PART NUMBER (Note 2)	RADIATION HARDNESS (Total Ionizing Dose)	TEMPERATURE RANGE (°C)	PACKAGE (RoHS COMPLIANT)	PKG. DWG. #
5962R1420302VYC	ISL70003ASEHVFE	HDR to 100krad(Si), LDR to 50krad(Si)	-55 to +125	64 Ld CQFP with Heatsink	R64.C
5962R1420302V9A	ISL70003ASEHVX (Note 3)	HDR to 100krad(Si), LDR to 50krad(Si)	-55 to +125	Die	
N/A	ISL70003ASEHFE/PROTO (Note 4)		-55 to +125	64 Ld CQFP with Heatsink	R64.C
N/A	ISL70003ASEHX/SAMPLE (Notes 3, 4)		-55 to +125	Die	
N/A	ISL70003ASEHEV1Z (Note 5)	Full Featured Evaluation Board			
N/A	ISL70003ASEHEV2Z (Note 5)	Small Form Factor Evaluation Board			

NOTES:

1. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed must be used when ordering.
2. These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
3. Die product tested at TA = + 25°C. The wafer probe test includes functional and parametric testing sufficient to make the die capable of meeting the electrical performance outlined in ""Electrical Specifications" on page 10.
4. The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across temperature specified in the DLA SMD and are in the same form and fit as the qualified device. The /SAMPLE parts are capable of meeting the electrical limits and conditions specified in the DLA SMD. The /SAMPLE parts do not receive 100% screening across temperature to the DLA SMD electrical limits. These part types do not come with a Certificate of Conformance because they are not DLA qualified devices.
5. Evaluation board uses the /PROTO parts. The /PROTO parts are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity.

Pin Configuration



* Indicates heatsink package R64.C

NOTE:

6. The ESD triangular mark is indicative of Pin #1 location. It is part of the device marking and is placed on the lid in the quadrant where Pin #1 is located.

Pin Descriptions

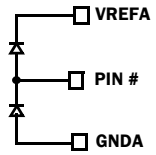
PIN NUMBER	PIN NAME	ESD CIRCUIT	DESCRIPTION
1	NI	1	The noninverting input to the internal error amplifier. Connect this pin to the REF pin for typical applications. For DDR memory power applications, connect NI to the BUFOUT pin.
2	FB	1	The inverting input to the internal error amplifier. Connect an external Type III compensation network between this pin and the VERR pin. The connection between the FB resistor divider and the output inductor should be a Kelvin connection to optimize performance.
3	VERR	1	The output of the internal error amplifier. Connect an external compensation network between this pin and the FB pin.
4	POR_VIN	1	The power-on reset input to the IC. This is a comparator-type input with a rising threshold of 0.6V and programmable hysteresis. Driving this pin above 0.6V enables the IC. Bypass this pin to AGND with a 10nF ceramic capacitor to mitigate SEE.
5	VREFA	3	The output of an internal linear regulator and is the bias supply input to the internal analog control circuitry. The output voltage is ~PVIN when PVIN <5V and is 5V when PVIN ≥5V. Do not use this pin for external circuitry. Locally filter this pin to AGND using a 0.47µF ceramic capacitor as close as possible to the IC.
6	AVDD	5	This pin provides the supply for the internal linear regulator of the ISL70003ASEH. The supply to AVDD should be locally bypassed using a ceramic capacitor. Tie AVDD to the PVINx pins.

Pin Descriptions (Continued)

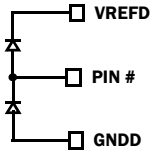
PIN NUMBER	PIN NAME	ESD CIRCUIT	DESCRIPTION
7	AGND	1, 3	The analog ground associated with the internal analog control circuitry. Connect this pin directly to the PCB ground plane.
8	DGND	2, 4	The ground associated with the internal digital control circuitry. Connect this pin directly to the PCB ground plane.
9	VREF_OUTS	4	The output of an internal linear regulator and the supply input to the internal reference circuit. The output voltage is ~PVIN when PVIN <5V and is 5V when PVIN ≥5V. Do not use this pin for external circuitry. Locally filter this pin to AGND using a 0.47µF ceramic capacitor as close as possible to the IC.
10	DVDD	6	This pin provides the supply for the internal linear regulator of the ISL70003ASEH. The supply to DVDD should be locally bypassed using a ceramic capacitor. Tie DVDD to the PVINx pin.
11	VREFD	4	The output of an internal linear regulator and the bias supply input to the internal digital control circuitry. The output voltage is ~PVIN when PVIN <5V and is 5V when PVIN ≥5V. Do not use this pin for external circuitry. Locally filter this pin to DGND using a 0.47µF ceramic capacitor as close as possible to the IC.
12	ENABLE	6	This pin is a logic-level enable input. Pulling this pin low powers down the device by placing it into a very low-power Sleep mode.
13	RT/CT	6	A resistor to VIN and a capacitor to GND provide feed-forward to keep a constant modulator gain of 4.8 as VIN varies.
14	FSEL	2	The oscillator frequency select input. Tie this pin to VREFD to select a 300kHz nominal oscillator frequency. Tie this pin to the PCB ground to select a 500kHz nominal oscillator frequency.
15	SYNC	2	The frequency synchronization input to the IC. Tie this pin to GND to free-run from the internal oscillator or connected to an external clock for external frequency synchronization.
16	SS_CAP	2	The soft-start input. Connect a ceramic capacitor from this pin to the PCB ground plane to set the soft-start output ramp time in accordance with Equation 1: $t_{SS} = C_{SS} \cdot V_{REF} / I_{SS}$ (EQ. 1) where: t_{SS} = soft-start output ramp time C_{SS} = soft-start capacitance V_{REF} = reference voltage (0.6V typical) I_{SS} = soft-start charging current (23µA typical) Soft-start time is adjustable from approximately 2ms to 200ms. The range of the soft-start capacitor should be 82nF to 8.2µF, inclusive.
17, 18, 19, 20, 21	GND	2	Connect these pin to the PCB ground plane.
22	PGOOD	6	The power-good output. This pin is an open-drain logic output that is pulled to DGND when the output voltage is outside a ±11% typical regulation window. This pin can be pulled up to any voltage from 0V to 13.2V, independent of the supply voltage. A nominal 1kΩ to 10kΩ pull-up resistor is recommended. Bypass this pin to the PCB ground plane with a 10nF ceramic capacitor to mitigate SEE.
23, 28, 32, 37, 38, 43, 44, 49, 53, 58	PVINx	7	The power supply inputs to the corresponding internal power blocks. These pins must be connected to a common power supply rail, which should fall in the range of 3V to 13.2V. Bypass these pins directly to PGNDx with ceramic capacitors located as close as possible to the IC. When sinking current or at a no load condition, the inductor valley current is negative. During any time when the inductor valley current is negative and the ISL70003ASEH is exposed to a heavy ion environment, the absolute maximum PVIN voltage must be ≤13.7V.
29	SEL1	2	A logic-level disable (high) input working in conjunction with SEL2. These pins form a 2-bit logic input that set the number of active power blocks. This allows the ISL70003ASEH current capability to be tailored to the load current level the application requires and achieve the highest possible efficiency.
30	SEL2	2	A logic-level disable input. Pulling this pin high inhibits pulses on the LXx outputs. See description of Pin 29, SEL1, for more information.
31	DE	2	The DE pin enables or disables diode emulation. When it is HIGH, diode emulation is allowed. Otherwise, Continuous Conduction mode is forced.
24, 27, 33, 36, 39, 42, 45, 48, 54, 57	LXx		The switch node connections to the internal power blocks. Connect to the output filter inductor. Internally, these pins are connected to the synchronous MOSFET power switches.

Pin Descriptions (Continued)

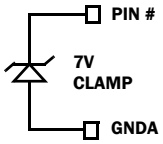
PIN NUMBER	PIN NAME	ESD CIRCUIT	DESCRIPTION
50	HS	N/A	On the R64.C package (heatsink option) this pin is electrically connected to the heatsink on the underside of the package. Connect this pin and/or the heatsink to a thermal plane.
51	IMON	1	IMON is a current source output that is proportional to the sensed current through the regulator. If not used, Renesas recommends tying IMON to VREFA. It is also acceptable to tie IMON to GND through a resistor.
52	SGND	1	This pin is connected to an internal metal trace that serves as a noise shield. Connect this pin to the PCB ground plane.
25, 26, 34, 35, 40, 41, 46, 47, 55, 56	PGNDx	7	The power grounds associated with the corresponding internal power blocks. Connect these pins directly to the PCB ground plane. Connect these pins to the negative terminals of the input and output capacitors as well. The package lid is internally connected to PGNDx.
59	OCSETA	3	The redundant output overcurrent set input. Connect a resistor from this pin to the PCB ground plane to set the output overcurrent threshold.
60	OCSETB	3	The primary output overcurrent set input. Connect a resistor from this pin to the PCB ground plane to set the output overcurrent threshold.
61	BUFIN+	1	The input to the internal unity gain buffer amplifier. For DDR memory power applications, connect the VTT voltage to this pin.
62	BUFIN-	1	The inverting input to the buffer amplifier. For DDR memory power applications, connect BUFOUT to this pin. Bypass this pin to the PCB ground plane with a 0.1µF ceramic capacitor.
63	BUFOUT	3	The output of the buffer amplifier. In DDR power applications, connect this pin to the reference input of the DDR memory. The buffer needs a minimum of 1.0µF load capacitor for stability.
64	REF	1	The output of the internal 600mV reference voltage. Bypass this pin to the PCB ground plane with a 220nF ceramic capacitor located as close as possible to the IC. The bypass capacitor is needed to mitigate SEE.



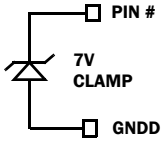
CIRCUIT 1



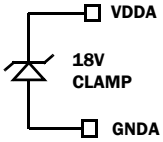
CIRCUIT 2



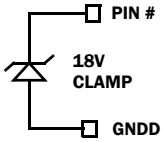
CIRCUIT 3



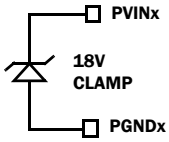
CIRCUIT 4



CIRCUIT 5

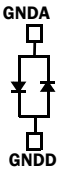


CIRCUIT 6

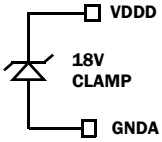


CIRCUIT 7

CIRCUIT 8



CIRCUIT 9



CIRCUIT 10

Typical Application Schematics

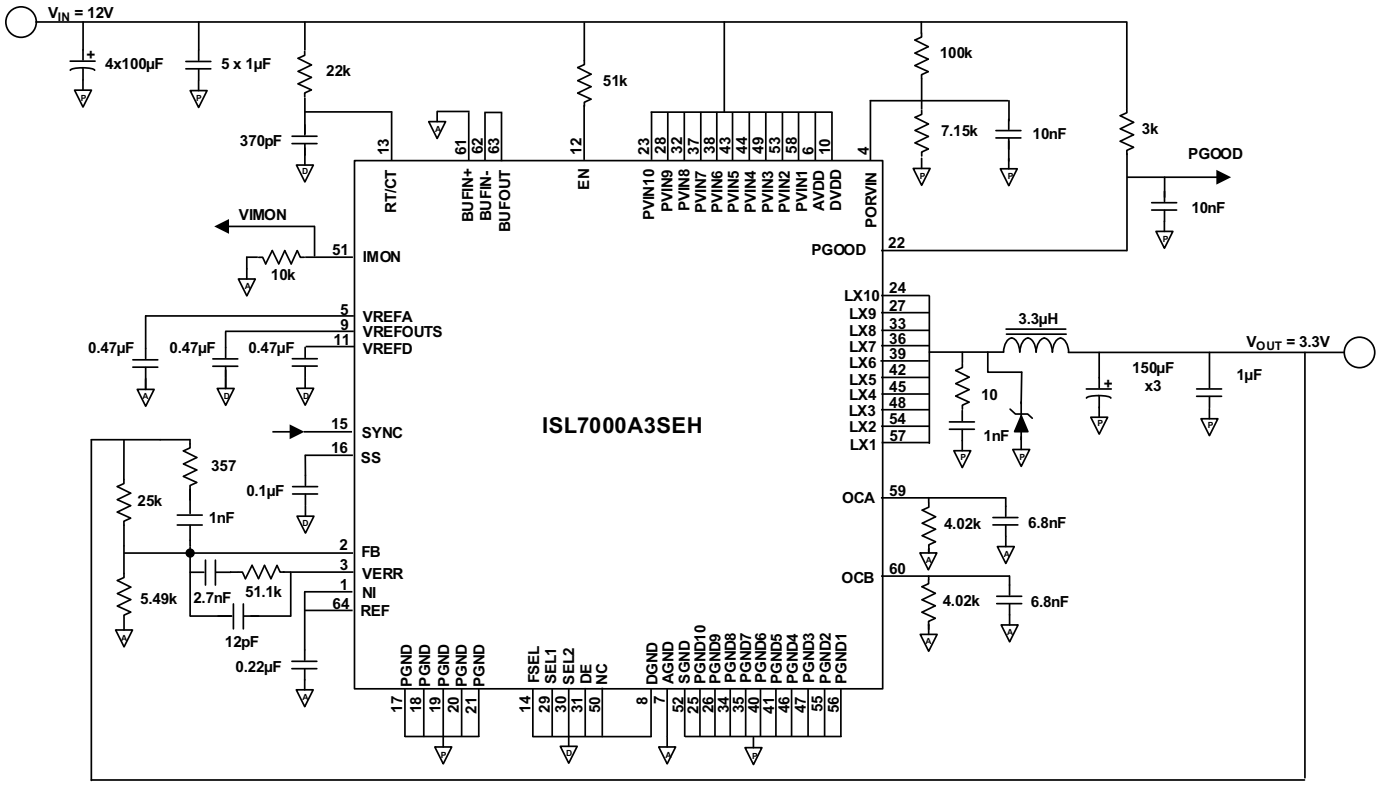


FIGURE 4. ISL70003ASEH SINGLE UNIT OPERATION

Typical Application Schematics (Continued)

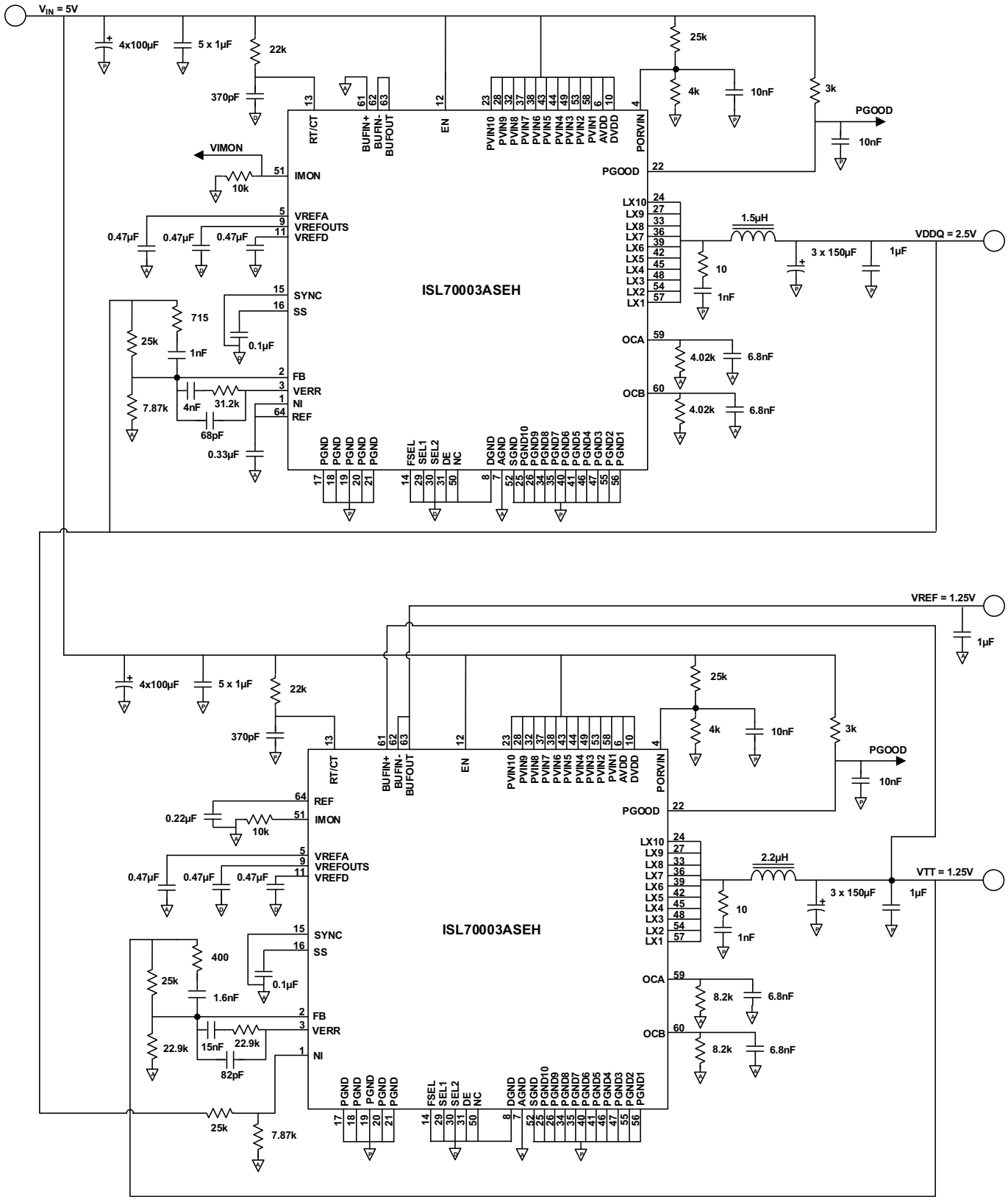


FIGURE 5. ISL70003ASEH DDR MEMORY POWER SOLUTION

Absolute Maximum Ratings

LXx, PVINx . . . . . (PGNDx - 0.3V) to PGNDx + 16V
LXx, PVINx (Note 7) . . . . . (PGNDx - 0.3V) to PGNDx + 14.7V
LXx, PVINx (Note 8) . . . . . (PGNDx - 0.3V) to PGNDx + 13.7V
AVDD - AGND, DVDD - DGND . . . . . PVINx to -0.3V
VREFA . . . . . (GNDA - 0.3V) to GNDA + 5.5V
VREFD, VREF_OUTS . . . . . (GNDD - 0.3V) to GNDD + 5.5V
Signal Pins (Note 11) . . . . . (GNDA - 0.3V) to VREFA + 0.3V
Digital Control Pins (Note 12) . . . . . (GNDD - 0.3V) to VREFD+ 0.3V
SS_CAP . . . . . (DGND - 0.3V) to DGND + 2.5V
PGOOD . . . . . (GNDD - 0.3V) to DVDD
RT/CT . . . . . (GNDD - 0.3V) to DVDD
Sourcing Output DC Current T_J ≤+125°C (All Power Blocks) 11A
Sourcing Output DC Current T_J ≤+150°C (All Power Blocks) 7A
Sinking Output DC Current T_J ≤+125°C (All Power Blocks) . . . . . -4A
ESD Rating
Human Body Model (Tested per MIL-STD-883 TM3015.7) 2kV
Machine Model (Tested per JESD22-A115-A) 200V
Charge Device Model (Tested per JESD22-C101D) 750V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CQFP Package R64.C (Notes 9, 10)	17	0.7

Maximum Junction Temperature . . . . . +150°C
Storage Temperature Range . . . . . -65°C to +150°C

Recommended Operating Conditions

Ambient Temperature . . . . . -55°C to +125°C
PVINx, AVDD, DVDD . . . . . 3.3V ±10% to 12V ±10%
Output DC Current T_J ≤+125°C (All Power Blocks) . . . . . ≤9A
Output DC Current T_J ≤+150°C (All Power Blocks) . . . . . ≤6A

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

NOTES:

7. For operation in a heavy ion environment at LET = 86.4MeV • cm^2/mg at +125°C (T_C) and sourcing 11A load current.
8. For operation in a heavy ion environment at LET = 86.4MeV • cm^2/mg at +125°C (T_C) with any negative inductor current to sinking -4A load current.
9. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with "direct attach" features. See TB379.
10. For θ_{JC}, the "case temp" location is the center of the exposed metal heatsink on the package underside.
11. POR_VIN, FB, NI, VERR, OCSETA, OCSETB, BUFOUT, BUFIN-, BUFIN+, IMON, and REF pins.
12. FSEL, EN, SYNC, SEL1, SEL2, and DE pins.

Electrical Specifications

Unless otherwise noted, PVINx = AVDD = DVDD = 3V - 13.2V; GND = AGND = DGND = PGNDx = SGND = 0V; POR_V_{IN} = 0.65V; SYNC = LXx = Open Circuit; PGOOD is pulled up to VREFD with a 3k resistor; REF is bypassed to GND with a 220nF capacitor; SS is bypassed to GND with a 100nF capacitor; I_{OUT} = 0A; T_A = T_J = +25°C. (Note 7). **Boldface limits apply across the operating temperature range, -55°C to +125°C; over a total ionizing dose of 100krad(Si) with exposure at a high dose rate of 50 to 300rad(Si)/s; or over a total ionizing dose of 50krad(Si) with exposure at a low dose rate of <10mrad(Si)/s.**

PARAMETER	TEST CONDITIONS	MIN (Note 16)	TYP	MAX (Note 16)	UNIT
POWER SUPPLY					
Operating Supply Current	PV_{INx} = 13.2V, FSEL = 1 (300kHz)		80	**125**	mA
	PV_{INx} = 13.2V, FSEL = 0 (500kHz)		80	**125**	mA
	PV_{INx} = 3.0V, FSEL = 1 (300kHz)		30	**60**	mA
	PV_{INx} = 3.0V, FSEL = 0 (500kHz)		30	**60**	mA
Standby Supply Current	PV_{INx} = 13.2V, SEL1 = SEL2 = 5V, FSEL = 1		20	**30**	mA
	PV_{INx} = 13.2V, SEL1 = SEL2 = 5V, FSEL = 0		20	**30**	mA
	PV_{INx} = 3.0V, SEL1 = SEL2 = 5V, FSEL = 1		10	**15**	mA
	PV_{INx} = 3.0V, SEL1 = SEL2 = 5V, FSEL = 0		10	**15**	mA
Shutdown Supply Current	PV_{INx} = 13.2V, EN = GND		1.5	**3.0**	mA
	PV_{INx} = 3.0V, EN = GND		0.4	**1.0**	mA
LINEAR REGULATORS					
Output Voltage	AVDD, DVDD = 13.2V	**4.5**	5.0	**5.5**	V
Current Limit	AVDD, DVDD = 13.2V	**50**		**190**	mA

Electrical Specifications Unless otherwise noted, PVINx = AVDD = DVDD = 3V - 13.2V; GND = AGND = DGND = PGNDx = SGND = 0V; POR_V_{IN} = 0.65V; SYNC = LXx = Open Circuit; PGOOD is pulled up to VREFD with a 3k resistor; REF is bypassed to GND with a 220nF capacitor; SS is bypassed to GND with a 100nF capacitor; I_{OUT} = 0A; T_A = T_J = +25°C. (Note 7). **Boldface limits apply across the operating temperature range, -55°C to +125°C; over a total ionizing dose of 100krad(Si) with exposure at a high dose rate of 50 to 300rad(Si)/s; or over a total ionizing dose of 50krad(Si) with exposure at a low dose rate of <10mrad(Si)/s. (Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 16)	TYP	MAX (Note 16)	UNIT
POWER-ON RESET					
POR Pin Input Voltage		**0.56**	0.60	**0.64**	V
POR Sink Current		**9.6**	12	**14.4**	µA
ENABLE					
Enable V_{IH} Voltage		**2**			V
Enable V_{IL} Voltage				**0.8**	V
Enable (EN) Leakage	EN = 4.5V		1.0	**10**	µA
SELECT PHASE					
SEL 1, 2 V_{IH} Voltage		**2**			V
SEL 1, 2 V_{IL} Voltage				**0.8**	V
SEL 1, 2 Leakage Current	SEL1, 2 = VREFD		1.0	**10**	µA
PWM CONTROL LOGIC					
Switching Frequency	FSEL = 1	**255**	300	**345**	kHz
	FSEL = 0	**425**	500	**575**	kHz
Minimum On-Time	SS = GND (Note 15)		250	**320**	ns
Minimum On-Time	(Note 15)		160	**220**	ns
Minimum Off-Time	(Note 15)		200	**270**	ns
Modulator Gain (V_{IN} /ΔV_{OSC})	R_T = 22kΩ, C_T = 370pF, FSEL = 0		5		V/V
	R_T = 36kΩ, C_T = 370pF, FSEL = 1		4.8		V/V
External Synchronization Frequency Range	FSEL = 1, PV_{INx} = 3.0V	**255**	300	**345**	kHz
	FSEL = 0, PV_{INx} = 3.0V	**425**	500	**575**	kHz
SYNC V_{IH} Voltage		**2**			V
SYNC V_{IL} Voltage				**0.8**	V
Synchronization Input Leakage Current	SYNC = VREFD		1.0	**4**	µA
SOFT-START					
Soft-Start Source Current	SS = GND	**20**	23	**27**	µA
Soft-Start Discharge ON-Resistance			3.0	**6.0**	Ω
Soft-Start Discharge Time	(Note 15)		256		Clock Cycles
REFERENCE VOLTAGE					
Reference Voltage Tolerance	V_{REF} including Error Amplifier V_{IO}	**0.594**	0.600	**0.606**	V

Electrical Specifications Unless otherwise noted, PVINx = AVDD = DVDD = 3V - 13.2V; GND = AGND = DGND = PGNDx = SGND = 0V; POR_V_{IN} = 0.65V; SYNC = LXx = Open Circuit; PGOOD is pulled up to VREFD with a 3k resistor; REF is bypassed to GND with a 220nF capacitor; SS is bypassed to GND with a 100nF capacitor; I_{OUT} = 0A; T_A = T_J = +25°C. (Note 7). **Boldface limits apply across the operating temperature range, -55°C to +125°C; over a total ionizing dose of 100krad(Si) with exposure at a high dose rate of 50 to 300rad(Si)/s; or over a total ionizing dose of 50krad(Si) with exposure at a low dose rate of <10mrad(Si)/s. (Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 16)	TYP	MAX (Note 16)	UNIT
LOAD REGULATION					
Output Voltage Tolerance Over Output Current Range	PVIN = 3V - 13.2V, to 9A (Notes 14, 15)	**-0.45**	-0.05	**0.25**	%
ERROR AMPLIFIER					
DC Gain	(Note 15)		80		dB
Gain-Bandwidth Product	(Note 15)		7		MHz
Maximum Output Voltage	V_{IN} = 5.5V	**3.5**	4.2		V
Slew Rate	(Note 15)		8.5		V/µs
Feedback (FB) Input Leakage Current	V_{FB} = 0.6V, PV_{INx} = 13.2V			**250**	nA
Offset Voltage (V_{IO})		**-3**	0	**3**	mV
POWER BLOCKS					
CQFP Individual Upper FET $r_{DS(ON)}$	PV_{INx} = 3.0V, PVIN to LX	**170**	420	**700**	mΩ
	PV_{INx} = 5.5V, PVIN to LX	**120**	310	**600**	mΩ
CQFP Individual Lower FET $r_{DS(ON)}$	PV_{INx} = 3.0V, LX to GND	**90**	240	**455**	mΩ
	PV_{INx} = 5.5V, LX to GND	**60**	210	**425**	mΩ
LXx Output Leakage	EN = LXx = GND, single LXx output		1	**3**	µA
	EN = GND, LXx = PV_{INx}, Single LXx output		1	**3**	µA
Dead Time	Within a single power block or between power blocks (Note 15)	**4**			ns
POWER-GOOD SIGNAL					
Rising Threshold	V_{FB} as a % of V_{REF}	**107**	111	**115**	%
Rising Hysteresis	V_{FB} as a % of V_{REF}	**2**	3.5	**5**	%
Falling Threshold	V_{FB} as a % of V_{REF}	**85**	89	**93**	%
Falling Hysteresis	V_{FB} as a % of V_{REF}	**2**	3.5	**5**	%
Power-Good Drive	PV_{IN} = 3V, PGOOD = 0.4V, EN = GND	**7.2**			mA
Power-Good Leakage	PV_{IN} = PGOOD = 13.2V			**1**	µA
PROTECTION FEATURES					
Undervoltage Protection					
Undervoltage Trip Threshold	V_{FB} as a % of V_{REF}, test mode	**71**	75	**79**	%
Undervoltage Recovery Threshold	V_{FB} as a % of V_{REF}, test mode	**86**	90	**94**	%
Overcurrent Protection					
Overcurrent Accuracy	ROCSETA, B = 6kΩ (IOC = 0.6A/LX) V_{IN} = 12V	**0.43**	0.60	**0.77**	A/LX

Electrical Specifications Unless otherwise noted, PVINx = AVDD = DVDD = 3V - 13.2V; GND = AGND = DGND = PGNDx = SGND = 0V; POR_V_{IN} = 0.65V; SYNC = LXx = Open Circuit; PGOOD is pulled up to VREFD with a 3k resistor; REF is bypassed to GND with a 220nF capacitor; SS is bypassed to GND with a 100nF capacitor; I_{OUT} = 0A; T_A = T_J = +25°C. (Note 7). **Boldface limits apply across the operating temperature range, -55°C to +125°C; over a total ionizing dose of 100krad(Si) with exposure at a high dose rate of 50 to 300rad(Si)/s; or over a total ionizing dose of 50krad(Si) with exposure at a low dose rate of <10mrad(Si)/s. (Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 16)	TYP	MAX (Note 16)	UNIT
BUFFER AMPLIFIER					
Gain-Bandwidth Product	C_L = 1µF, I_{SOURCE} = 1mA, A_V = 1, V_{OUT} = 1.25V (Note 15)		200		kHz
Source Current Capability				**20**	mA
Sink Current Capability		**250**	400		µA
Offset Voltage		**-4**	0	**4**	mV
IMON CURRENT MONITOR					
IMON Sense Time		**145**	225	**300**	ns
IMON Output Current Gain	I_{LOAD} = 1A/power stage, LXx off time >300ns		100		µA/A
IMON Gain Accuracy	I_{LOAD} = 1A/power stage, LXx off time >300ns	**-14**		**14**	µA

NOTES:

13. Typical values shown are not guaranteed.
14. The 0A to 9A output current range may be reduced by minimum LXx on-time and minimum LXx off-time specifications.
15. Limits established by characterization or analysis and are not production tested.
16. Parameters with MIN and/or MAX limits are 100% tested at -55°C, +25°C and +125°C, unless otherwise specified.

Typical Performance Curves

Unless otherwise noted, the test platform is the ISL70003ASEHEV1Z where V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 3A, f_{SW} = 500kHz, C_{IN} = 4x 100µF + 5x1µF, L_{OUT} = 3.3µH, C_{OUT} = 1x 150µF + 1µF, T_{CASE} = +25°C, all outputs active.

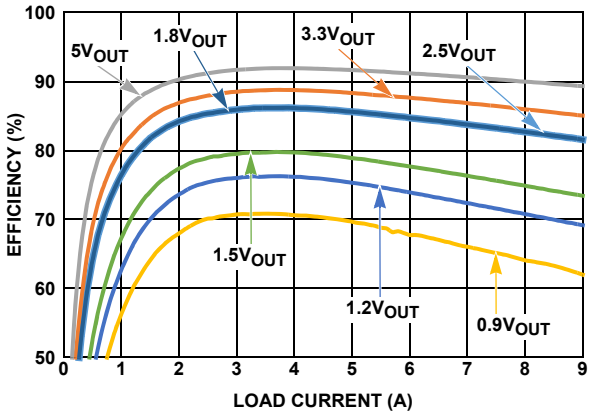


FIGURE 6. EFFICIENCY vs LOAD, V_{IN} = 12V, 300kHz

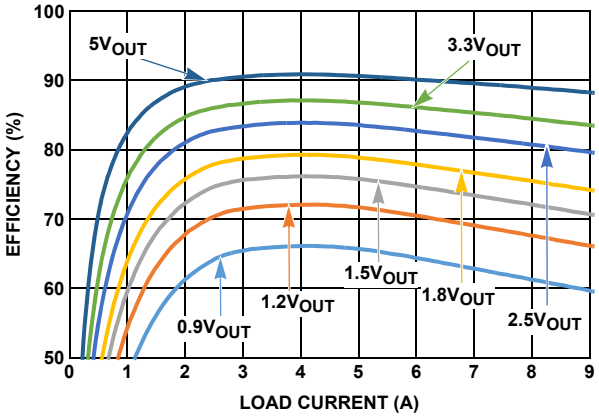


FIGURE 7. EFFICIENCY vs LOAD, V_{IN} = 12V, 500kHz

Typical Performance Curves

Unless otherwise noted, the test platform is the ISL70003ASEHEV1Z where V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 3A, f_{SW} = 500kHz, C_{IN} = 4x 100µF + 5x1µF, L_{OUT} = 3.3µH, C_{OUT} = 1x 150µF + 1µF, T_{CASE} = +25°C, all outputs active. **(Continued)**

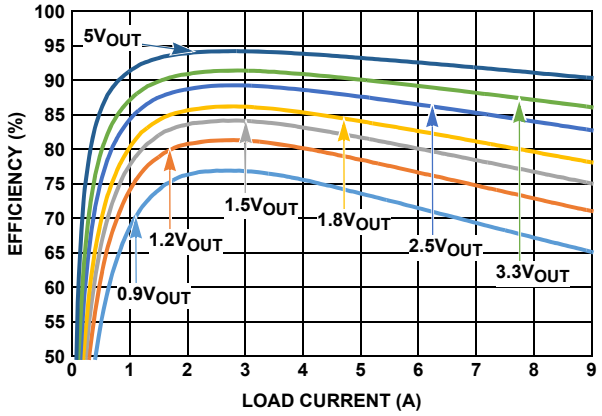


FIGURE 8. EFFICIENCY vs LOAD, V_{IN} = 8V, 300kHz

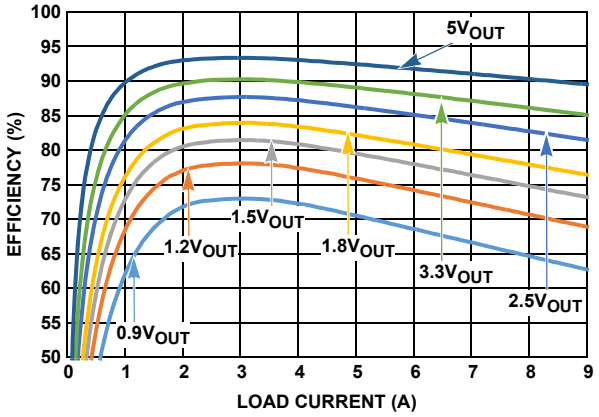


FIGURE 9. EFFICIENCY vs LOAD, V_{IN} = 8V, 500kHz

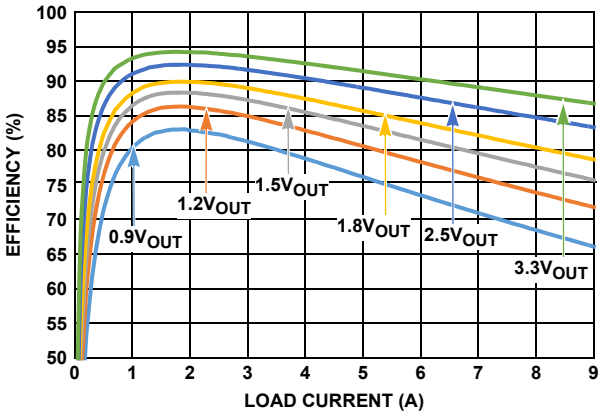


FIGURE 10. EFFICIENCY vs LOAD, V_{IN} = 5V, 300kHz

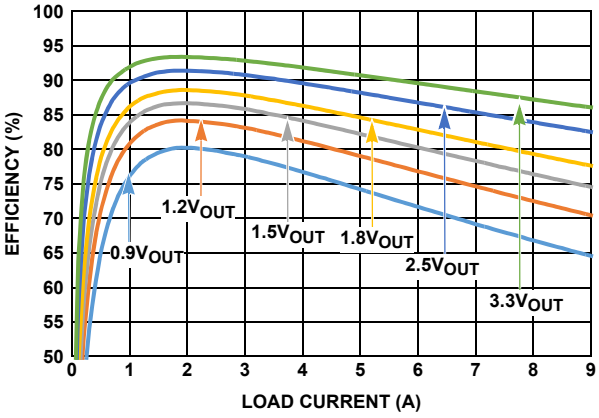


FIGURE 11. EFFICIENCY vs LOAD, V_{IN} = 5V, 500kHz

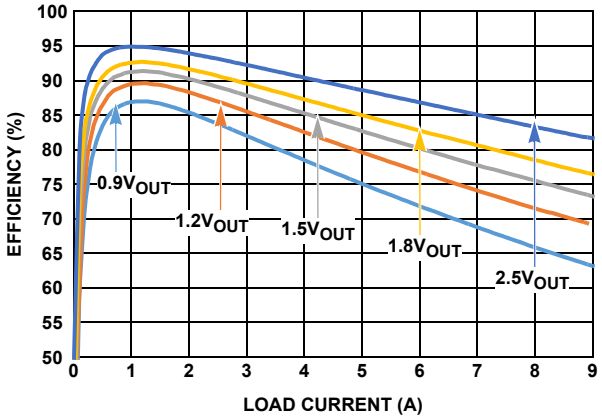


FIGURE 12. EFFICIENCY vs LOAD, V_{IN} = 3.3V, 300kHz

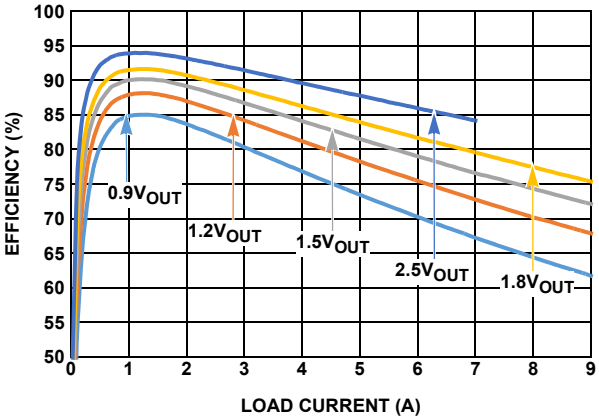


FIGURE 13. EFFICIENCY vs LOAD, V_{IN} = 3.3V, 500kHz

Typical Performance Curves

Unless otherwise noted, the test platform is the ISL70003ASEHEV1Z where V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 3A, f_{SW} = 500kHz, C_{IN} = 4x 100µF + 5x1µF, L_{OUT} = 3.3µH, C_{OUT} = 1x 150µF + 1µF, T_{CASE} = +25°C, all outputs active. **(Continued)**

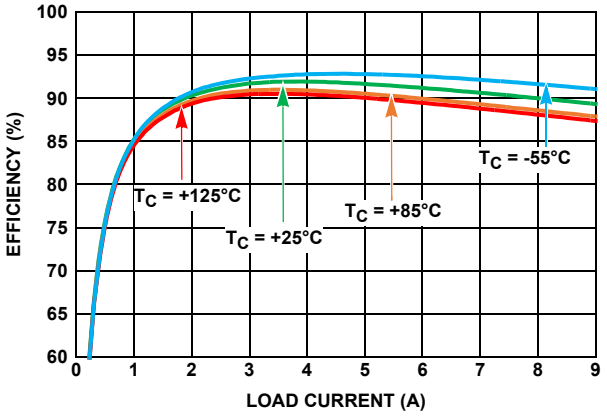


FIGURE 14. EFFICIENCY vs LOAD, V_{IN} = 12V, V_{OUT} = 5V, 300kHz

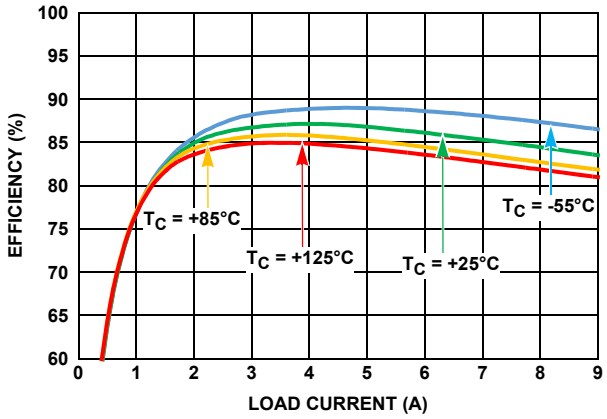


FIGURE 15. EFFICIENCY vs LOAD, V_{IN} = 12V, V_{OUT} = 3.3V, 500kHz

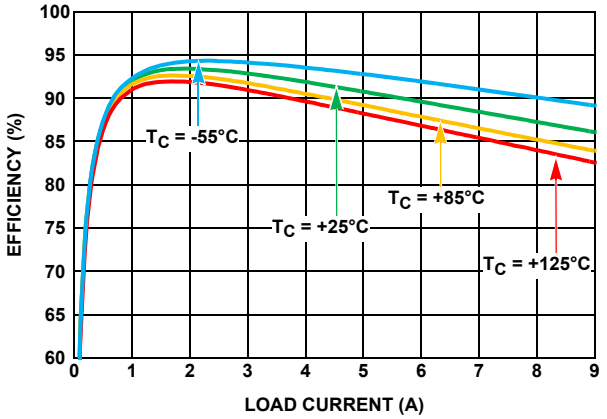


FIGURE 16. EFFICIENCY vs LOAD, V_{IN} = 5V, V_{OUT} = 3.3V, 500kHz

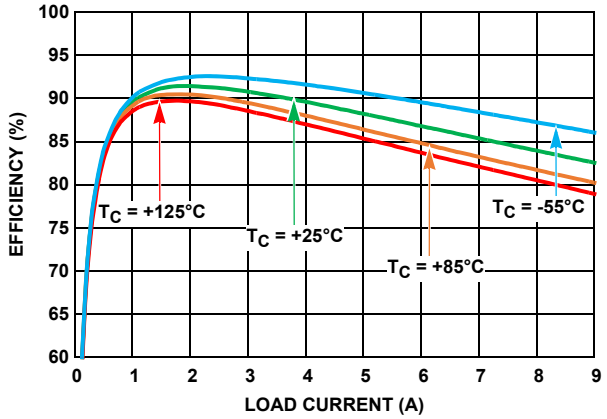


FIGURE 17. EFFICIENCY vs LOAD, V_{IN} = 5V, V_{OUT} = 2.5V, 500kHz

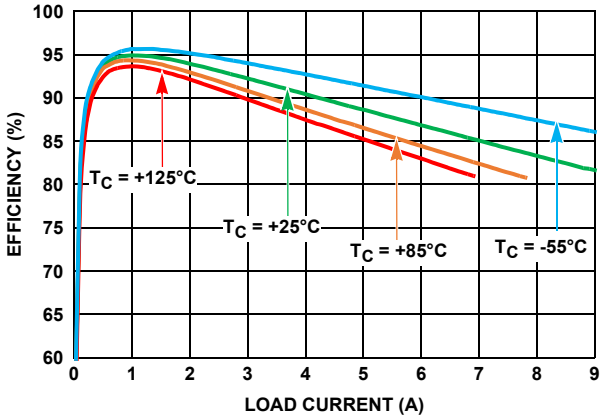


FIGURE 18. EFFICIENCY vs LOAD, V_{IN} = 3.3V, V_{OUT} = 2.5V, 300kHz

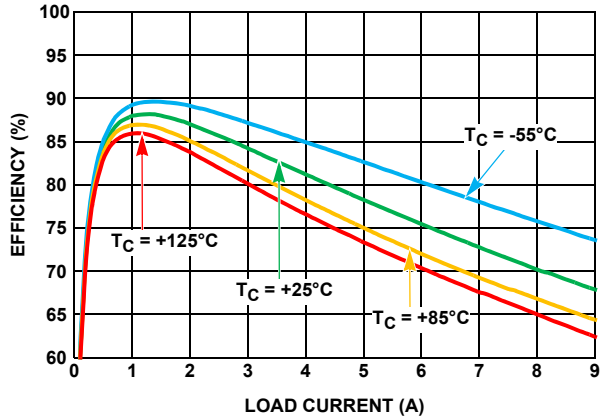


FIGURE 19. EFFICIENCY vs LOAD, V_{IN} = 3.3V, V_{OUT} = 1.2V, 500kHz

Typical Performance Curves

Unless otherwise noted, the test platform is the ISL70003ASEHEV1Z where V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 3A, f_{SW} = 500kHz, C_{IN} = 4x 100µF + 5x1µF, L_{OUT} = 3.3µH, C_{OUT} = 1x 150µF + 1µF, T_{CASE} = +25°C, all outputs active. **(Continued)**

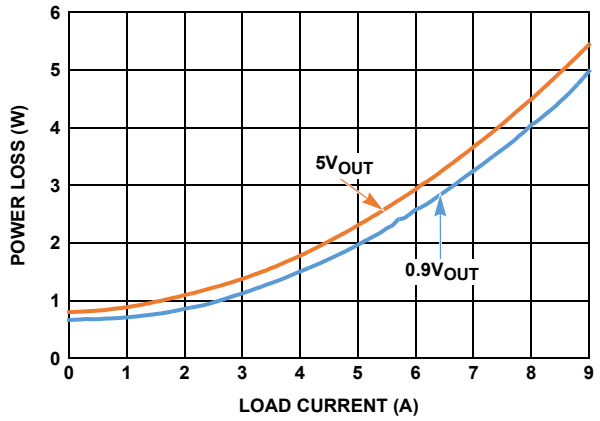


FIGURE 20. POWER LOSS, V_{IN} = 12V, 300kHz

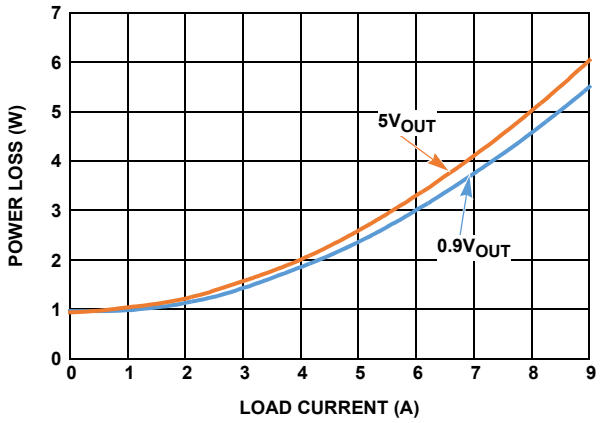


FIGURE 21. POWER LOSS, V_{IN} = 12V, 500kHz

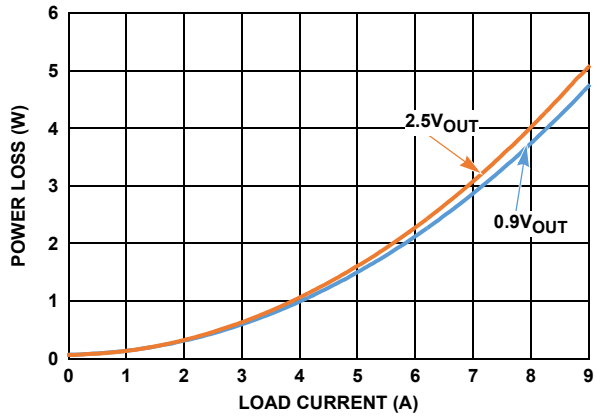


FIGURE 22. POWER LOSS, V_{IN} = 3.3V, 300kHz

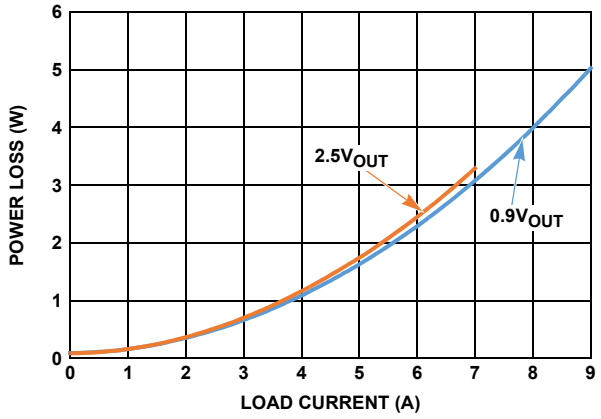


FIGURE 23. POWER LOSS, V_{IN} = 3.3V, 500kHz

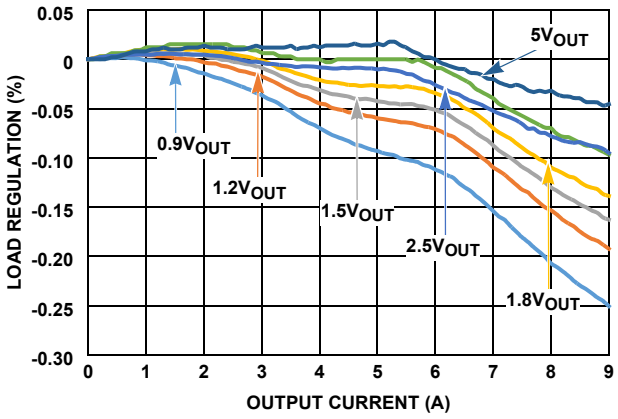


FIGURE 24. LOAD REGULATION vs V_{OUT}, PVIN = 12V

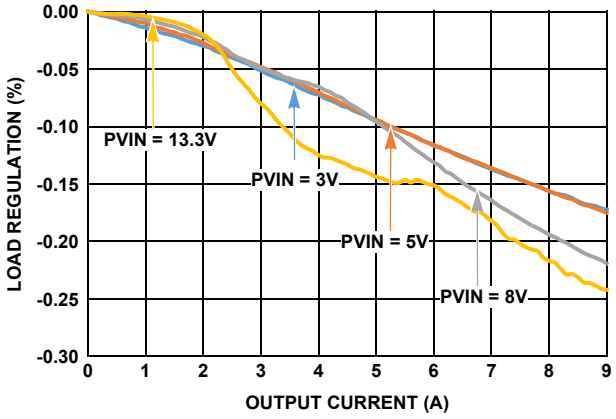


FIGURE 25. LOAD REGULATION vs PVIN, V_{OUT} = 1.0V

Typical Performance Curves

Unless otherwise noted, the test platform is the ISL70003ASEHEV1Z where V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 3A, f_{SW} = 500kHz, C_{IN} = 4x 100µF + 5x1µF, L_{OUT} = 3.3µH, C_{OUT} = 1x 150µF + 1µF, T_{CASE} = +25°C, all outputs active. **(Continued)**

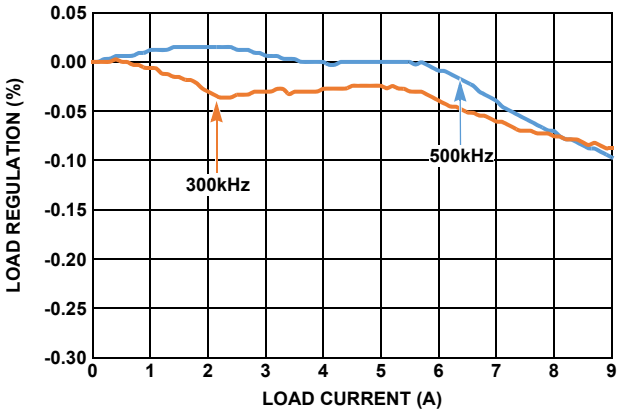


FIGURE 26. LOAD REGULATION vs SWITCHING FREQUENCY

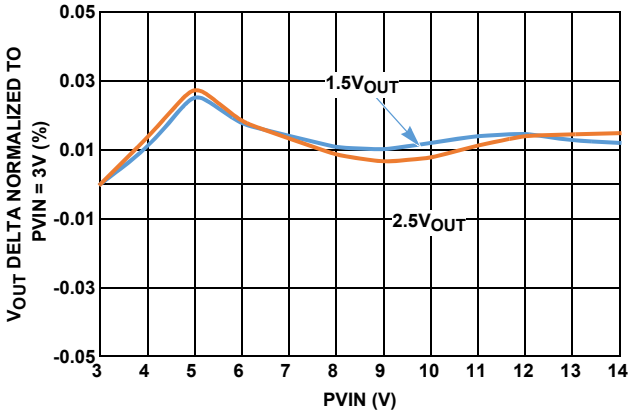


FIGURE 27. LINE REGULATION, V_{OUT} = 1.0V, LOAD = 3A

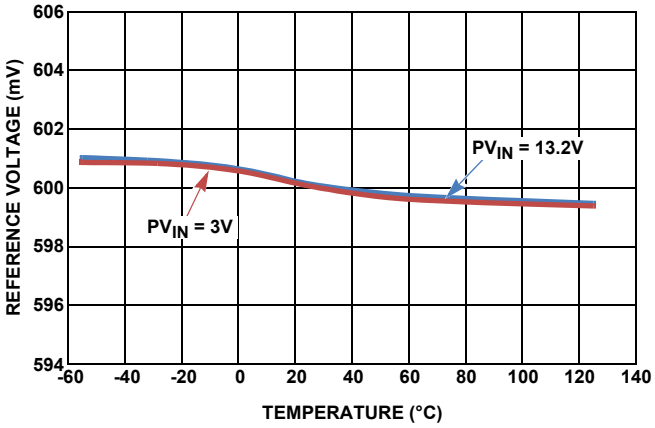


FIGURE 28. REFERENCE VOLTAGE vs TEMPERATURE

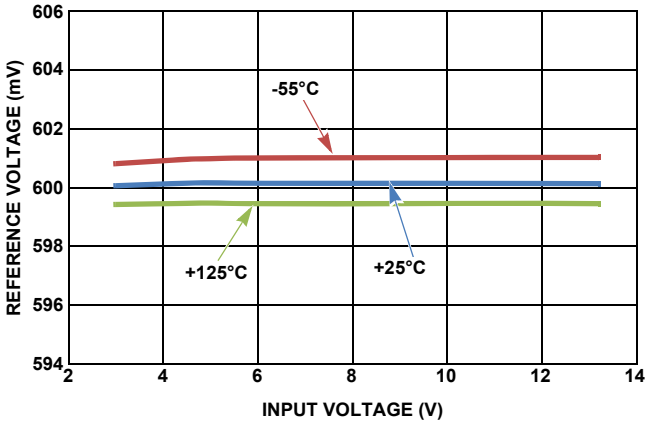


FIGURE 29. REFERENCE VOLTAGE vs V_{IN}

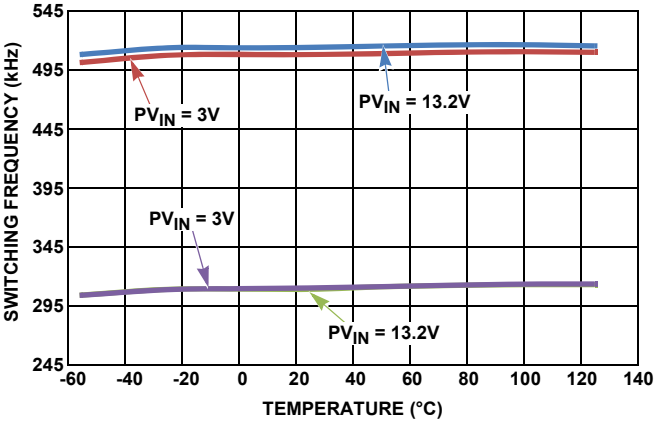


FIGURE 30. SWITCHING FREQUENCY vs TEMPERATURE

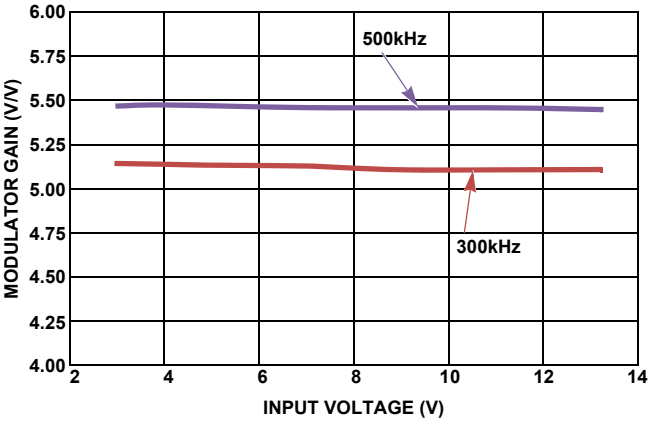


FIGURE 31. MODULATOR GAIN vs V_{IN}

Typical Performance Curves

Unless otherwise noted, the test platform is the ISL70003ASEHEV1Z where V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 3A, f_{SW} = 500kHz, C_{IN} = 4x 100µF + 5x1µF, L_{OUT} = 3.3µH, C_{OUT} = 1x 150µF + 1µF, T_{CASE} = +25°C, all outputs active. **(Continued)**

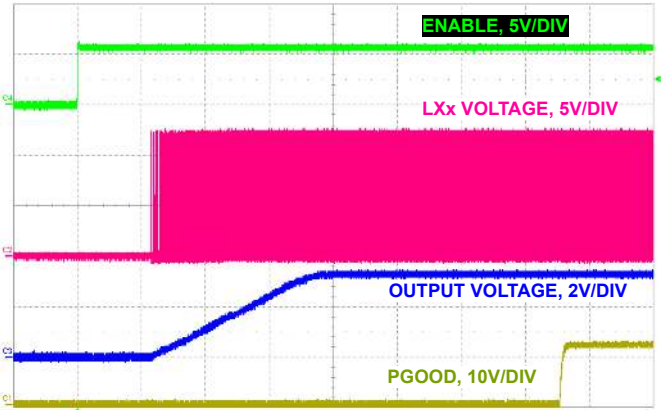


FIGURE 32. MONOTONIC SOFT-START WITH NO LOAD, CCM

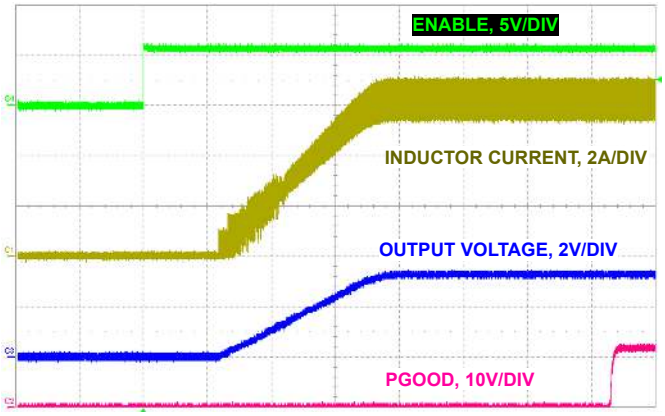


FIGURE 33. MONOTONIC SOFT-START WITH 6A LOAD, CCM

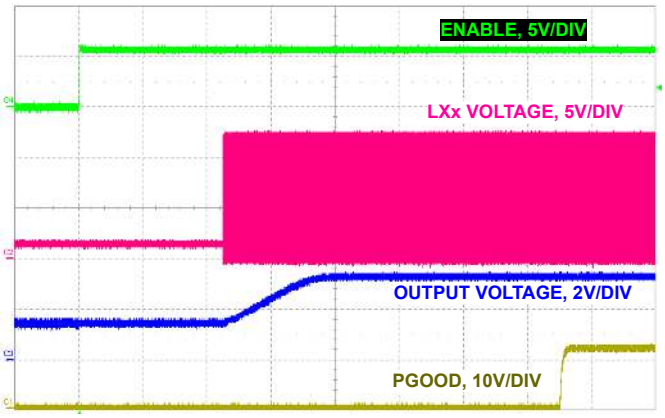


FIGURE 34. MONOTONIC SOFT-START WITH 1.5V PREBIASED LOAD

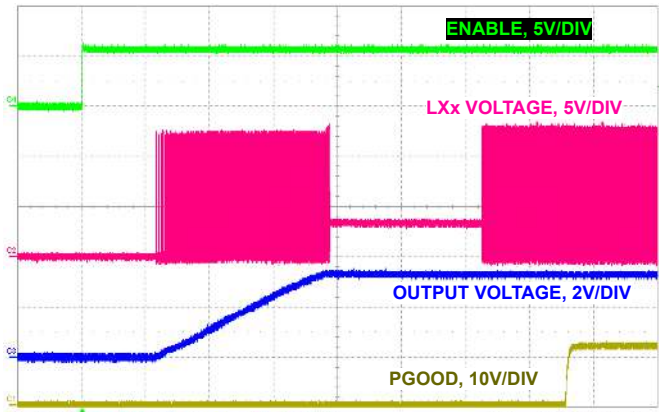


FIGURE 35. MONOTONIC SOFT-START WITH NO LOAD, DEM

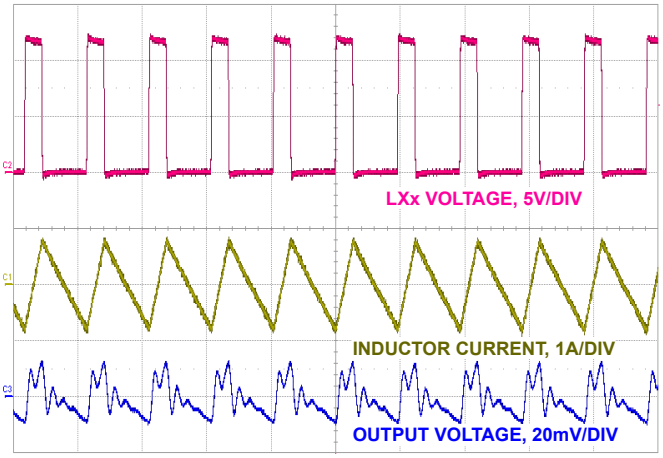


FIGURE 36. STEADY STATE OPERATION NO LOAD, CCM

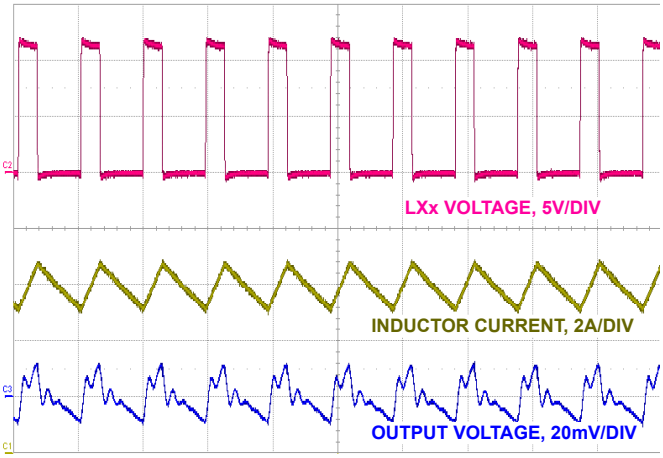


FIGURE 37. STEADY STATE OPERATION 6A LOAD, CCM

Typical Performance Curves

Unless otherwise noted, the test platform is the ISL70003ASEHEV1Z where V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 3A, f_{SW} = 500kHz, C_{IN} = 4x 100µF + 5x1µF, L_{OUT} = 3.3µH, C_{OUT} = 1x 150µF + 1µF, T_{CASE} = +25°C, all outputs active. **(Continued)**

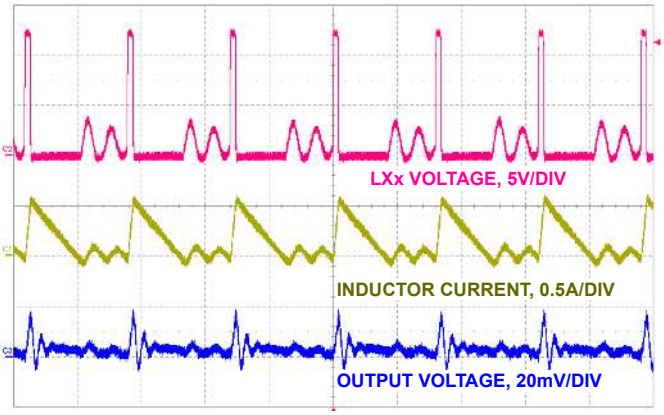


FIGURE 38. DIODE EMULATION OPERATION, V_{OUT} = 1.2V, 125mA LOAD

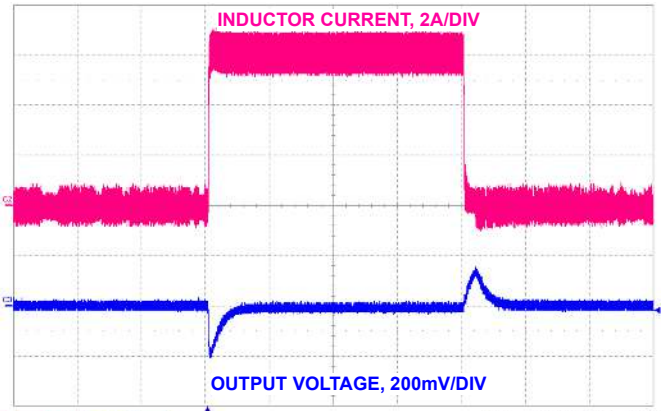


FIGURE 39. 6A LOAD TRANSIENT RESPONSE, DIODE EMULATION

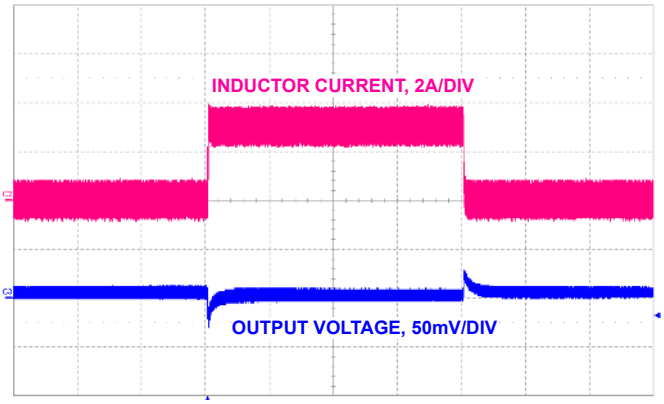


FIGURE 40. 3A LOAD TRANSIENT RESPONSE

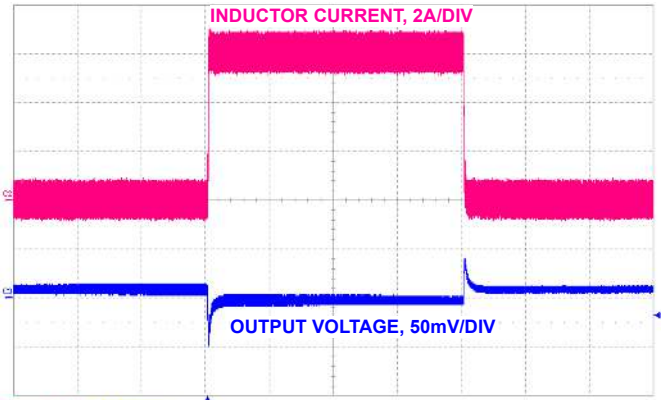


FIGURE 41. 6A LOAD TRANSIENT RESPONSE

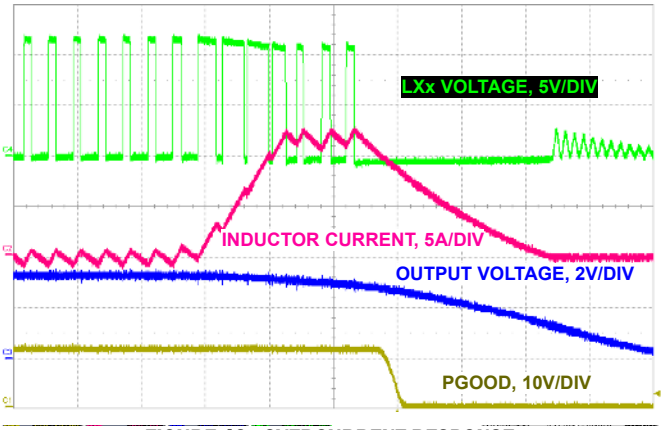


FIGURE 42. OVERCURRENT RESPONSE

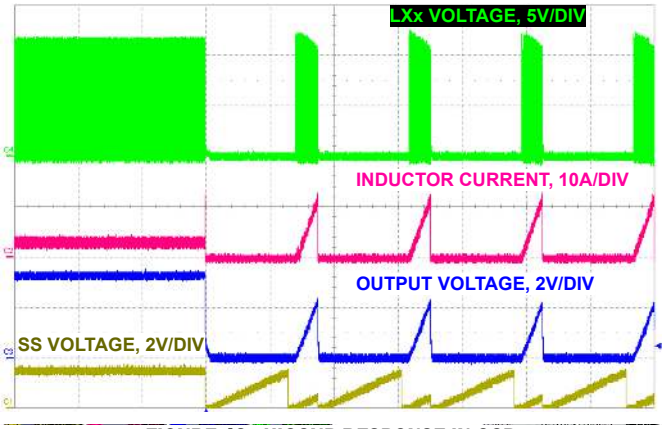


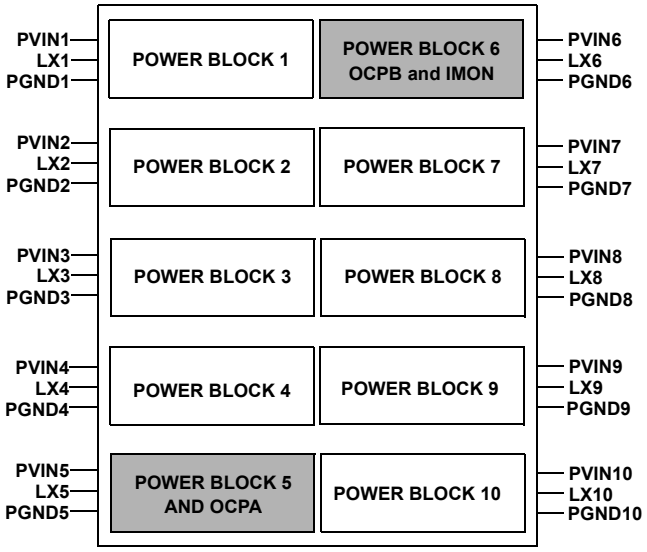
FIGURE 43. HICCUP RESPONSE IN OCP

Functional Description

The ISL70003ASEH is a monolithic synchronous buck regulator IC with integrated power MOSFETs. The device uses voltage-mode control with feed-forward and switches at a nominal frequency of 500kHz or 300kHz. It is fabricated on a 0.6µm BiCMOS junction isolated process optimized for power management applications. With this device and a handful of external components, a complete synchronous buck DC/DC converter can be readily implemented. The converter accepts an input voltage ranging from 3V to 13.2V and provides both a tightly regulated output voltage ranging from 0.6V to ~90% of the input voltage and output currents ranging from 0A to 9A. Typical applications include Point-Of-Load (POL) regulation for FPGAs, CPLDs, DSPs, DDR memory, and microprocessors.

Power Blocks

The power output stage of the regulator consists of ten power blocks that are paralleled to provide full 9A output current capability at T_J = +125°C. The block diagram in Figure 44 shows a top level view of the individual power blocks.



Note: Shaded blocks indicate pilot current and current sensors.

FIGURE 44. POWER BLOCK DIAGRAM

The SEL1 and SEL2 pins allow users to disable power blocks to reduce switching losses in light-load applications. Depending on the state of these pins the ISL70003ASEH can operate with 2, 4, or 10 active power blocks and also be placed in sleep mode.

Each power block has a power supply input pin, PVINx, a phase output pin, LXx, and a power supply ground pin, PGNDx. All PVINx pins must be connected to a common power supply rail and all PGNDx pins must be connected to a common ground. The LXx pins should be connected to the output inductor based on the required load current and the state of the SEL1, SEL2 pins, but the LX5 and LX6 pins must be included. The unused LXx pins should be left unconnected.

Scaled pilot devices associated with Power Blocks 5 and 6 provide current feedback for overcurrent detection and the IMON current monitor feature. Power Blocks 5 and 6 must be connected to the output inductor at all times for proper operation.

Initialization

The ISL70003ASEH initializes based on the state of the EN input and POR input. Successful initialization prompts a soft-start interval and the regulator begins slowly ramping the output voltage. When the commanded output voltage is within the proper window of operation, the power-good signal changes state from low to high indicating proper regulator operation.

Enable

The EN pin accepts TTL/CMOS logic input as described in the "Electrical Specifications" table on page 10. When the voltage on the EN pin exceeds its logic rising threshold, the controller monitors the POR voltage before initiating the soft-start function for the PWM regulator. When EN is pulled low, the device enters shutdown mode, and the supply current drops to a typical value of 1.5mA. All internal power devices are held in a high impedance state while in Shutdown mode. Due to the internal 5V clamp, the EN pin should be driven no higher than 5V or excessive leakage current may be seen on the pin. In standalone applications, the EN pin can be tied to an input voltage >5V through a 50kΩ resistor to minimize the current into the EN pin. The current should not be allowed to exceed 160µA at any operating voltage.

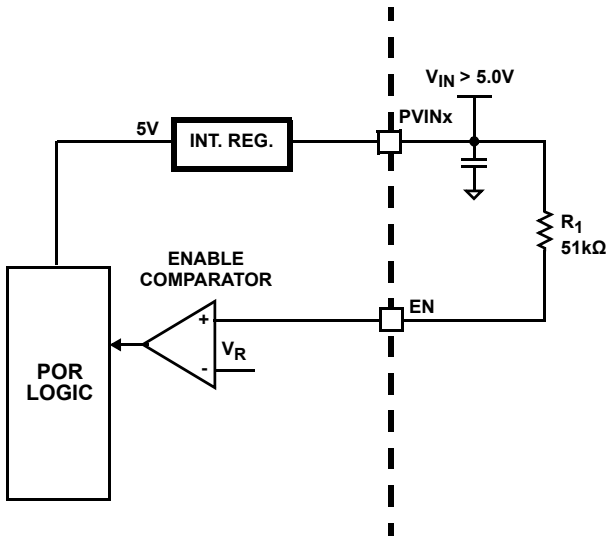


FIGURE 45. ENABLE TO V_{IN} FOR >5.0V INPUT VOLTAGE

Power-On Reset

After the EN input requirements are met, the ISL70003ASEH remains in shutdown until the voltage at the POR pin rises above its threshold. The POR circuitry prevents the controller from attempting to soft-start before sufficient bias is present at the PVINx pins.

As shown in Figure 46 on page 21, the POR circuit features a comparator type input. The POR circuit allows the level of the input voltage to precisely gate the turn-on/turn-off of the regulator. An internal I_{POR} current sink with a typical value of 12µA is only active when the voltage on the POR pin is below the enable threshold so that it can pull the POR pin low. As V_{IN} rises, the POR enable level is set by the resistor divider (R_1 and R_2) from V_{IN} and the internal sink current source, I_{POR}.

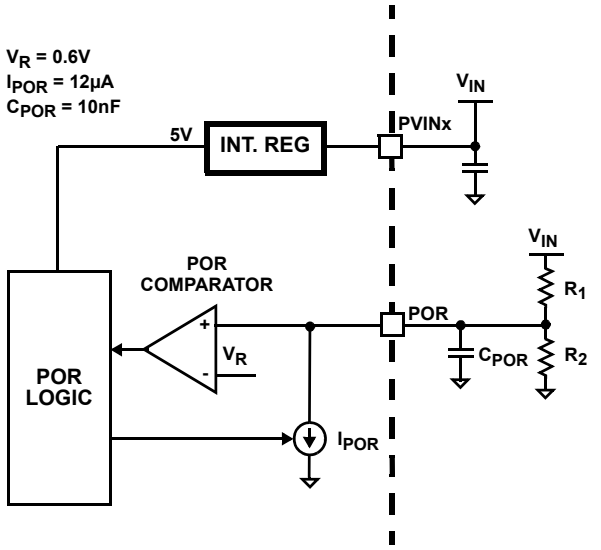


FIGURE 46. POR CIRCUIT

Equation 2 defines the relationship between the resistor divider, sink current, and POR rising level (V_{PORR}).

$$V_{PORR} = V_R \cdot \left[1 + \frac{R_1}{R_2}\right] + I_{POR} \cdot R_1 \quad \text{(EQ. 2)}$$

When the voltage at the POR pin reaches the enable threshold, the I_{POR} current sink turns off.

With the part enabled and the I_{POR} current sink off, the falling level (V_{PORF}) is set by the resistor divider network and is defined by Equation 3.

$$V_{PORF} = V_R \cdot \left[1 + \frac{R_1}{R_2}\right] \quad \text{(EQ. 3)}$$

The difference between the POR rising and falling levels provides adjustable hysteresis so that noise on V_{IN} does not interfere with the enabling or disabling of the regulator.

Soft-Start

The ISL70003ASEH soft-start function uses an internal current source and an external capacitor to reduce stresses and surge current during start-up.

When the POR and enable circuits are satisfied, the regulator waits 32 clock cycles and then initiates a soft-start. Figure 47 shows that the soft-start circuit clamps the error amplifier reference voltage to the voltage on an external soft-start capacitor connected to the SS pin. The soft-start capacitor is charged by an internal I_{SS} current source. As the soft-start capacitor is charged, the output voltage slowly ramps to the set point determined by the reference voltage and the feedback network. When the voltage on the SS pin is equal to the internal reference voltage, the soft-start interval is complete. Following the soft-start interval is a delay to power good being signaled. The soft-start output ramp interval is defined in Equation 4 and is adjustable from approximately 2ms to 200ms. The value of the soft-start capacitor, C_{SS}, should range from 82nF to 8.2µF, inclusive. The peak inrush current can be computed from Equation 5. Select a soft-start interval that is long enough to ensure that the peak inrush current plus the peak output load current does not exceed the overcurrent trip level of the regulator.

$$t_{SS} = C_{SS} \cdot \frac{V_{REF}}{I_{SS}} \quad \text{(EQ. 4)}$$

$$I_{INRUSH} = C_{OUT} \cdot \frac{V_{OUT}}{t_{SS}} \quad \text{(EQ. 5)}$$

The soft-start capacitor is immediately discharged by a 3.0Ω resistor whenever POR conditions are not met or EN is pulled low. The soft-start discharge time is equal to 256 clock cycles.

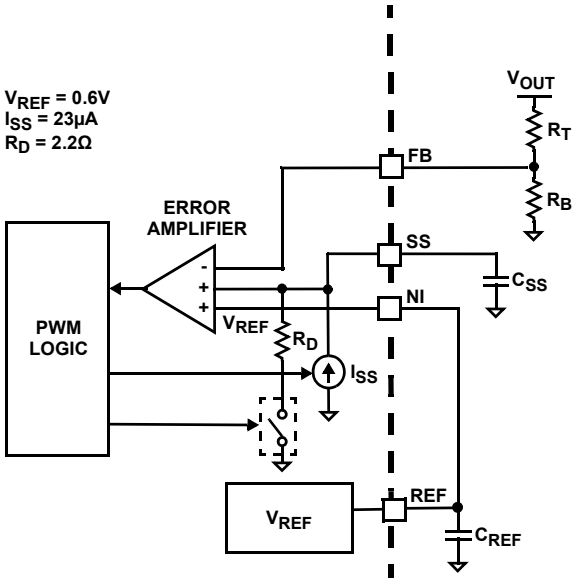


FIGURE 47. SOFT-START CIRCUIT

Power-Good

A power-good indicator is the final step of initialization. After a successful soft-start, the PGOOD pin releases and the voltage rises with an external pull-up resistor. The power-good signal transitions low immediately when the EN pin is pulled low.

The PGOOD pin is an open-drain, logic output and can be pulled up to any voltage from 0V to 13.2V. The pull-up resistor should have a nominal value from 1kΩ to 10kΩ. To mitigate SEE, bypass the PGOOD pin to DGND with a 10nF ceramic capacitor.

Fault Monitoring and Protection

The ISL70003ASEH actively monitors the output voltage and current to detect fault conditions. Fault conditions trigger protective measures to prevent damage to the regulator and the external load device. One common power-good indication signal is provided for linking to external system monitors. The schematic in Figure 48 on page 22 outlines the interaction between the fault monitors and the power-good signal.

Undervoltage and Overvoltage Monitor

The power-good pin (PGOOD) is an open-drain, logic output which indicates that the converter is operating properly and the output voltage is within a set window. The Undervoltage (UV) and

Overvoltage (OV) comparators create the output voltage window. The power-good circuitry monitors the FB pin and compares it to the rising and falling thresholds shown in the “Electrical Specifications” table on page 12. If the feedback voltage exceeds the typical rising limit of 111% of the reference voltage, the PGOOD pin pulls low. The PGOOD pin continues to pull low until the feedback voltage falls to a typical of 107.5% of the reference voltage. If the feedback voltage drops below a typical of 89% of the reference voltage, the PGOOD pin pulls low. The PGOOD pin continues to pull low until the feedback voltage rises to a typical 92.5% of the reference voltage. The PGOOD pin then releases and signals the return of the output voltage within the power-good window.

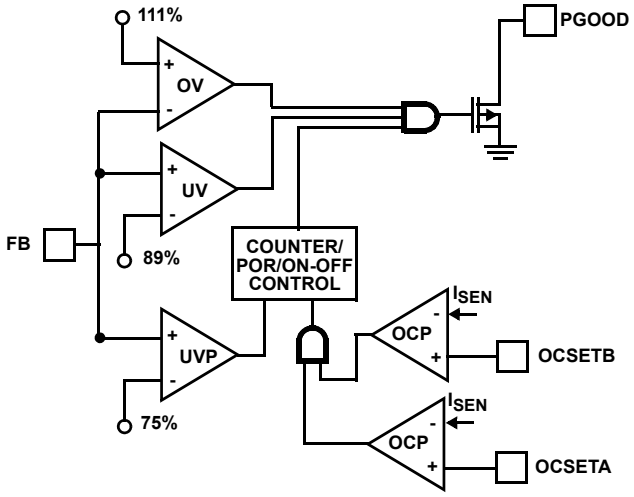


FIGURE 48. POWER-GOOD AND OC PROTECTION CIRCUITRY

Undervoltage Protection

A hysteretic comparator monitors the FB pin of the regulator. The feedback voltage is compared to an undervoltage threshold that is a fixed percentage of the reference voltage, typically 75%. When the comparator trips, indicating a valid undervoltage condition, an undervoltage counter increments. The counter is reset if the feedback voltage rises back both above the undervoltage threshold plus a specified amount of hysteresis outlined in the “Electrical Specifications” table on page 12. If there are four consecutive undervoltage detections, the counter will overflow and the undervoltage protection logic shuts down the regulator pulling PGOOD low.

After the regulator shuts down, it enters a delay interval, approximately equivalent to 512 clock cycles plus one soft-start interval, allowing the device to cool. The undervoltage counter is reset entering the delay interval. The protection logic initiates a normal soft-start when the delay interval ends. If the output successfully soft starts, the power-good signal goes high and normal operation continues. If undervoltage conditions continue to exist during the soft-start interval, the undervoltage counter must overflow before the regulator shuts down again. This Hiccup mode continues indefinitely until the output soft starts successfully.

Overcurrent Protection

A pilot device integrated into the PMOS transistor of Power Blocks 5 and 6 sample the current each cycle. This current feedback is scaled and compared to an overcurrent threshold based on the resistor value tied from pins OCSETA and OCSETB to AGND.

Upon detection of an overcurrent condition, the upper MOSFET is immediately turned off and is not turned on again until the next switching cycle. Upon detection of the initial overcurrent condition, the overcurrent fault counter is set to “1”. If, on the subsequent cycle, another overcurrent condition is detected, the OC fault counter increments. However, if the sampled current falls below the threshold, the counter is reset. If there are four sequential OC fault detections, the counter overflows and the regulator is shut down under an overcurrent fault condition, pulling PGOOD low.

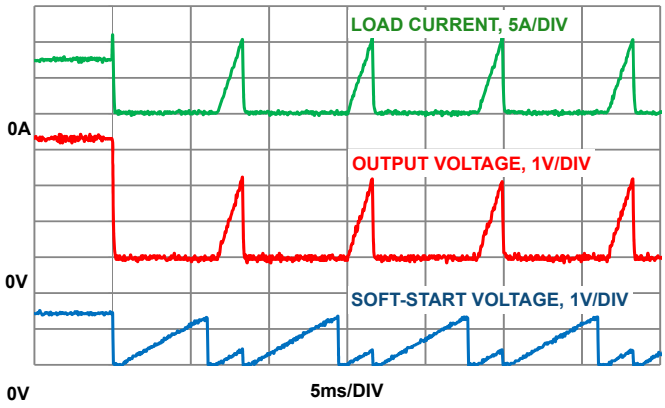


FIGURE 49. OVERCURRENT BEHAVIOR IN HICCUP MODE

After the regulator shuts down, it enters a delay interval, allowing the device to cool. The delay interval is approximately equal to 512 clock cycles plus one soft-start interval. The overcurrent counter is reset entering the delay interval. The protection logic initiates a normal soft-start when the delay interval ends. If the output successfully soft starts, the power-good signal goes high and normal operation continues. If overcurrent conditions continue to exist during the soft-start interval, the overcurrent counter must overflow before the regulator shutdowns the output again. This Hiccup mode continues indefinitely until the output soft starts successfully (see Figure 49).

Load Regulation

The ISL70003ASEH is a metal-only revision of the ISL70003SEH specifically designed to improve load regulation across the wider 9A output current rating. Although the load regulation is now improved by an order of magnitude, there are performance generalities to be aware of: higher temperature, lower PVIN, and higher VOUT/PVIN ratio all yield tighter load regulation performance. The switching frequency has no deterministic effect, producing differences one order of magnitude less than the other condition considerations. Figure 2 on page 1 and Figures 24, 25, 26, and 27 on page 17 illustrate performance trends for a sampling of these conditions.

Application Information

Voltage Feed-Forward

Feed-forward is used to maintain a constant modulator gain and achieve optimum loop response over a wide input voltage range. A resistor from PVINx to RT/CT and a capacitor from RT/CT to PGNDx are used to adjust the amplitude of the sawtooth ramp proportional to the input voltage. The capacitor value must be chosen so that it is large enough for mitigation of single-event transients, but low enough for the internal MOSFET device to pull the pin to ground. The following table gives the recommended values for R_T and C_T for a given switching frequency. These values achieve a constant modulator gain across the complete input voltage range.

FSEL STATE	f_{SW} (kHz)	R_T (kΩ)	C_T (pF)	MODULATOR GAIN (TYP)
0	500	22	370	5
1	300	36	370	4.8

Switching Frequency Selection

Several variables to consider when choosing the switching frequency are:

- A high switching frequency increases the switching losses, but may lead to a decrease in output filter size.
- A lower switching frequency may increase efficiency, but may lead to more output voltage ripple and increased output filter size.

On the ISL70003ASEH, the internal switching frequency is determined by the state of the FSEL pin. This pin is to be tied either high to VREFD for 300kHz or low to GND for 500kHz switching frequency.

Synchronization

The ISL70003ASEH can be synchronized to an external clock with a frequency range of 500kHz ±15% or 300kHz ±15%, depending on the state of the FSEL pin.

The SYNC pin accepts the external clock signal and the regulator is synchronized in phase with the external clock. During start-up, the regulator uses its internal oscillator to regulate the output voltage. When soft-start is complete and PGOOD is released, the regulator synchronizes to the external clock signal. This feature allows the ISL70003ASEH regulator to be the power source to the external components that are providing the external clock without the requirement that a signal must be present at the SYNC pin before start-up.

Output Voltage Selection

The output voltage of the regulator can be programmed through an external resistor divider that is used to scale the output voltage relative to the reference voltage. The reference voltage and the noninverting input to the error amplifier are not internally connected; therefore, for standalone applications the REF pin must be tied to the NI pin (see Figure 50). To mitigate SEE, bypass the REF pin to AGND with a 220nF ceramic capacitor.

Note that no current (sourcing or sinking) is available from the REF pin.

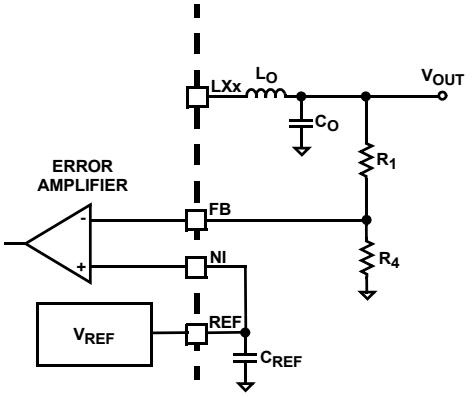


FIGURE 50. OUTPUT VOLTAGE SELECTION

The output voltage programming resistor, R_4, depends on the value chosen for the feedback resistor, R_1, and the desired output voltage of the regulator. The value for the feedback resistor is typically between 5kΩ and 25kΩ.

If the output voltage desired is 0.6V, R_4 is left unpopulated.

$$R_4 = \frac{R_1 \times 0.6V}{V_{OUT} - 0.6V} \quad \text{(EQ. 6)}$$

Setting the Overcurrent Protection Level

The ISL70003ASEH features dual redundancy in the overcurrent detection circuitry, which helps avoid false overcurrent triggering due to single event effects. Two external resistors from pins OCSETA and OCSETB to AGND set the level of the Overcurrent Protection (OCP) trip point. The OCP circuit senses the peak current across a pilot device, not the average current so it is important to determine the overcurrent trip point (I_{OCP}) greater than the maximum output continuous current (I_{MAX}), plus half the maximum inductor ripple current (ΔI).

Use Equation 7 to determine the peak-to-peak inductor ripple current:

$$\Delta I = \frac{V_{IN} - V_{OUT}}{f_{SW} \times L} \times D \quad \text{(EQ. 7)}$$

where f_{SW} is the switching frequency, L is the output inductor value, and D is duty cycle. When an I_{OCP} value is chosen that satisfies Equation 8:

$$I_{OCP} \geq I_{MAX} + \frac{\Delta I}{2} \quad \text{(EQ. 8)}$$

Equation 9 can be used to determine the value of R_{OCSETA} and R_{OCSETB} with all 10 power blocks active.

$$R_{OCSET(A,B)} = \frac{36024}{I_{OCP}} \quad \text{(EQ. 9)}$$

The minimum value for $R_{OCSET(A,B)}$ is 2.87kΩ, which is equivalent to a 12.5A I_{OCP} level.

Disabling the Power Blocks

The ISL70003ASEH offers two TTL/CMOS compatible power block select pins, SEL1 and SEL2, which form a 2-bit logic input that are used to turn off the internal power blocks. Depending on the state of the SEL1 and SEL2 pins, the ISL70003ASEH can operate with 2, 4, or 10 power blocks on or have all the outputs in a tri-state mode. This allows the designer to reduce switching losses in low current applications, where all power blocks are not needed to supply the load current. Table 1 compares the logic state of SEL1 and SEL2 with the current capability of the regulator and the number of active LXx pins.

TABLE 1. LOGIC STATE COMPARISON

SEL2 STATE	SEL1 STATE	ACTIVE LXx PINS	LOAD CAPABILITY (T_J = +125°C)
0	0	All	9A
0	1	5, 6, 7, 8	3.6A
1	0	5, 6	1.8A
1	1	None	N/A

With both SEL pins in a logic high state, the ISL70003ASEH is in a low power Sleep mode in which all outputs are tri-stated. When the logic activates the power blocks, the regulator ramps the output voltage to its set value within a soft-start interval, however, the device no longer goes through the preinitialization phase.

Transitions between the number of active LXx pins through the use of SEL1 and SEL2 should not be done while the part is operating. On-the-fly transitions cause glitches on the output voltage which may exceed transient requirements. Renesas recommends placing the ISL70003ASEH in Standby mode, by pulling SEL1 and SEL2 HIGH, then change the number of active LXx pins.

The overcurrent trip point scales depending on the number of active power blocks. Equation 10 can be used to determine the value of R_{OCSETA} and R_{OCSETB} when less than 10 power blocks are active:

$$R_{OCSET(A,B)} = \frac{3602.4 \times N}{I_{OCP}} \quad \text{(EQ. 10)}$$

where N is the number of active power block phases.

IMON Current-Sense Output

The ISL70003ASEH provides a current monitor function through IMON. Current monitoring informs designers if downstream loads are operating as expected. It is also useful in the prototype and debug phase of the design and during normal operation to measure the overall performance of a system. The IMON pin outputs a high speed analog current source that is proportional to the sensed peak current through the ISL70003ASEH. In typical applications, a resistor R_{IMON} is connected to the IMON pin to convert the sensed current to voltage, V_{IMON}, which is proportional to the peak current as shown in Equation 11:

$$V_{IMON} = 100 \times 10^{-6} \cdot \frac{I_{SAMPLE} \times R_{IMON}}{N} \quad \text{(EQ. 11)}$$

V_{IMON} is the voltage at the IMON pin, R_{IMON} is the resistor between the IMON pin and AGND, I_{SAMPLE} is the current through the converter at the time IMON samples the current, and N is the number of active power blocks. I_{SAMPLE} can be calculated from Equation 12.

$$I_{SAMPLE} = I_{LOAD} + \frac{\Delta I}{2} - \left(\Delta I \cdot \frac{t_{SAMPLE} \times f_{SW}}{(1-D)}\right) \quad \text{(EQ. 12)}$$

t_{SAMPLE} is the time it takes the IMON circuitry to sample the current (300ns, max.), I_{LOAD} is the load current, and ΔI is the inductor peak-to-peak ripple current as calculated in Equation 7.

Place a small capacitor between the IMON pin and AGND to reduce the noise impact and mitigate single event transients. If this pin is not used, it is best connected to VREFA. It is also acceptable to tie to GND through a resistor.

Figures 51 and 52 show the response of the IMON current monitor due to a load step with a R_{IMON} = 10kΩ and 100pF ceramic capacitor in parallel.

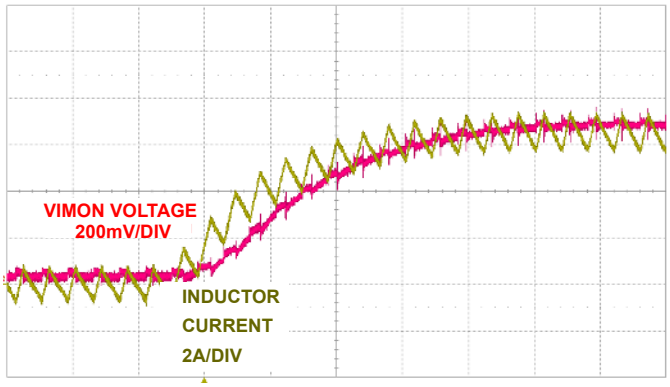


FIGURE 51. IMON RESPONSE TO 6A LOAD STEP

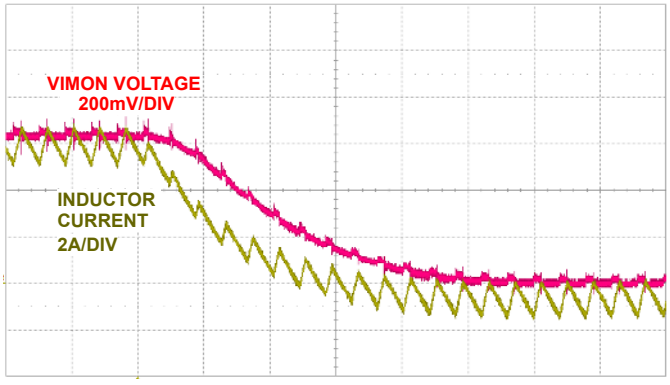


FIGURE 52. IMON RESPONSE TO 6A LOAD RELEASE

Although the IMON output reflects the peak current sensed, it can be also used to approximate the DC output current with a more accurate approximation at higher current levels and lower PVIN voltage. Figure 53 shows a graph normalized to 100µA of IMON current to 1A of output current across a 10kΩ resistor.

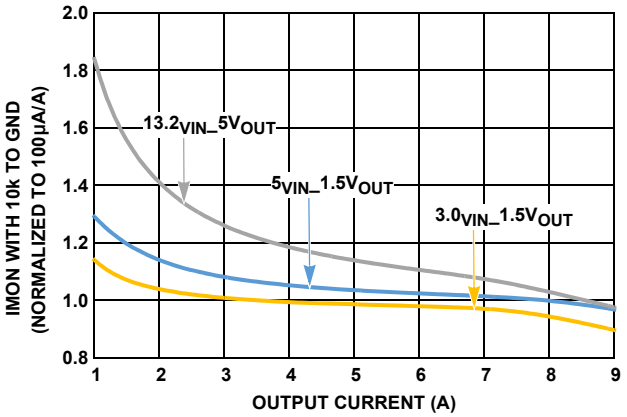


FIGURE 53. IMON TO DC I_{OUT}

It is important to note that if the on-time of the lower NMOS FET is shorter than the IMON current-sense time (300ns max), the IMON output is tri-stated after four consecutive failed sense occurrences.

Diode Emulation

Diode Emulation (DE) allows for higher converter efficiency under light-load situations. In DE mode, the low-side MOSFET conducts when the current is flowing from source-to-drain and does not allow reverse current, emulating a diode. As shown in Figure 54, when the LGATE signal is HIGH, the low-side MOSFET carries current, creating negative voltage on the phase node due to the voltage drop across the ON-resistance. When the DE pin is pulled HIGH, the ISL70003ASEH is in DE mode and detect the zero current crossing of the inductor current, and turn off the lower MOSFET to prevent the inductor current from reversing direction and creating unnecessary power loss. This ensures that Discontinuous Conduction Mode (DCM) is achieved. Because diode emulation prevents the low-side MOSFET from sinking current, no negative spike at the output is generated during prebiased startup when DE mode is active.

After a significantly fast load-release transient, diode emulation does not allow the converter to bring the output voltage back down following the hump created by the inductor energy dump into the output capacitor bank. The ISL70003ASEH overcomes this issue by monitoring the output of the error amplifier and allowing the low-side MOSFET to turn on and sink the necessary current needed to properly regulate the output voltage. The same mechanism allows the converter to properly regulate the output voltage when starting into a prebiased condition in which the prebias level is greater than the desired output voltage.

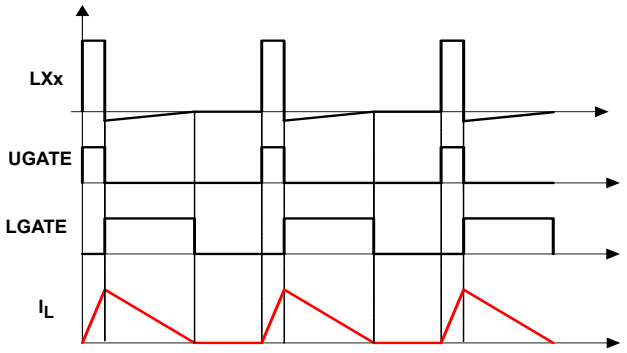


FIGURE 54. DIODE EMULATION

The DE pin is not intended to actively change states while the regulator is operating. If any part of the inductor current is below zero and the DE pin changes state, there is a glitch on the output voltage. However, if the state of the DE pin changes state when the inductor current is positive, no change in the operation of the regulator is seen.

DDR Application

High throughput Double Data Rate (DDR) memory ICs are replacing traditional memory ICs in space applications. A novel feature associated with this type of memory is the referencing and data bus termination techniques. These techniques employ a reference voltage, V_{REF}, that tracks the center point of V_{DDQ} and V_{SS} voltages, and an additional V_{TT} power source where all terminating resistors are connected. Despite the additional power source, the overall memory power consumption is reduced compared to traditional termination.

The added power source has a cluster of requirements that should be observed and considered. Due to the reduced differential thresholds of DDR memory, the termination power supply voltage, V_{TT}, closely tracks $V_{DDQ}/2$ voltage.

Another very important feature of the termination power supply is the capability to operate at equal efficiency in sourcing and sinking modes. The V_{TT} supply regulates the output voltage with the same degree of precision when current is flowing from the supply to the load, and when the current is diverted back from the load into the power supply.

The ISL70003ASEH regulator possesses several important enhancements that allow reconfiguration for DDR memory applications. Two ISL70003ASEH ICs provide all three voltages required in a DDR memory compliant system.

DDR Configuration

In the DDR application presented in Figure 55, an independent architecture is implemented to generate the voltages needed for DDR memory applications. Consequently, both $V_{DD}Q$ and V_{TT} are derived independently from the main power source.
The first regulator supplies the 2.5V for the $V_{DD}Q$ voltage. The output voltage is set by external dividers R_{T1} and R_{B1}.
The second regulator generates the V_{TT} rail typically = $V_{DDQ}/2$. Using an identical resistor divider from the output of the V_{DDQ} output to the noninverting input pin of the V_{TT} regulator's error amplifier (NI), R_{T1} and R_{B1} provides the tracking function for the V_{TT} voltage. R_{T2} and R_{B2} are used to set the V_{TT} output voltage to 1.25V.

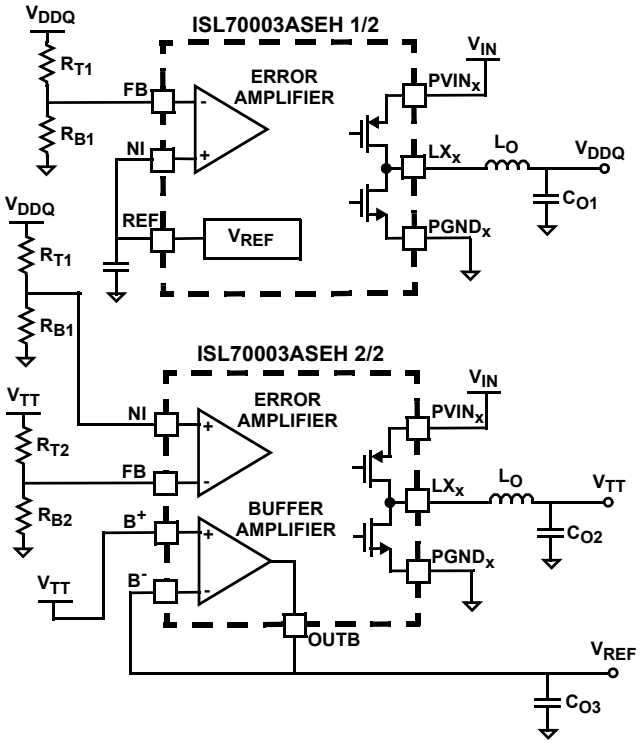


FIGURE 55. SIMPLIFIED DDR APPLICATION SCHEMATIC

The V_{REF} voltage is generated by connecting the noninverting input of the buffer amplifier to the V_{TT} output. The output of the buffer is tied back to the inverting input for a unity gain configuration. The buffer output voltage serves as a 1.25V reference (V_{REF}) for the DDR memory devices. Sourcing capability of the buffer amplifier is 10mA typical (20mA max) and needs a minimum of 1µF load capacitance for stability.

Diode Emulation mode of operation must be disabled on the V_{TT} regulator to allow sinking capability. In the event both channels are enabled simultaneously, the soft-start capacitor on the $V_{DD}Q$ regulator should be two to three times larger than the soft-start capacitor on the V_{TT} regulator. This allows the $V_{DD}Q$ regulator voltage to be the lowest input into the error amplifier of the V_{TT} regulator and dominate the soft-start ramp. However, if the V_{TT} regulator is enabled later than the $V_{DD}Q$, the soft-start capacitor can be any value based on design goals.

Each regulator has its own fault protections and must be individually configured. All the sink current on the V_{TT} regulator is provided by the $V_{DD}Q$ rail. The over current protection on the $V_{DD}Q$ rail limits the amount of current that the V_{TT} rail will sink.

When sinking current or at a no-load condition, the inductor valley current is negative, see Figure 36. During any time when the inductor valley current is negative and the ISL70003ASEH is exposed to a heavy ion environment, the absolute maximum PVIN voltage must be ≤13.7V, see Note 8 on page 10.

SEL1 and SEL2 can be tied together and used to place the V_{TT} regulator in Sleep mode, common to DDR applications. The outputs are tri-stated, however, the buffer amplifier is still active and the V_{REF} voltage is present even if the V_{TT} is in Sleep mode. When SEL1 and SEL2 are asserted low, the V_{TT} regulator ramps up the voltage. The ramp is controlled and timing is based on soft-start capacitor value.

Refer to Figure 5 on page 9 for complete DDR power solution typical application circuit schematic.

Voltages for DDR2 memory can be like wise derived with the V_{DD} (V_{DD}, $V_{DD}L$, $V_{DD}Q$) specified as 1.8V ±100mV, the V_{REF} is expected to equal $V_{DD}Q/2$ and to track variations in the DC level of $V_{DD}Q$. V_{TT} is equal to V_{REF} ±40mV and is to track V_{REF}.

Operational Envelope

The ISL70003ASEH is rated for operation across a PVIN of 3V to 13.2V, for a V_{OUT} of 0.6V to ~11.9V, and an output current up to 9A, with a 500kHz switching frequency, and to a +125°C die temperature. Although rated to these conditions, operation is not simultaneously all-inclusive because there are combinations of these conditions, particularly at the extremes of minimum on and off times, in which it does not operate, thus defining a conditional operational envelope.

Figures 13 and 18 show the reduced output current capability for the PVIN = 3.3V, V_{OUT} = 2.5V condition illustrating one corner of the envelope in which the ratio of V_{OUT} to PVIN is too high in combination with the temperature and current extremes. The converter runs into regulation issues with a 500kHz switching frequency due to inadequate off time being realized under these conditions. Another conditional operation corner, being the situation where the ratio of V_{OUT} to PVIN is too low, and the result is current limiting. In both of these extreme conditions, the maximum output current capability is reduced and output accuracy is compromised.

These graphs are to be considered illustrative of the operation envelope and not guidance. Users must characterize and evaluate their circuit performance to their satisfaction when approaching the extreme conditions of voltage, current, and temperature.

High Current Protection Clamp

When using the ISL70003ASEH to output >6A, it is necessary to implement a LX to PGND Schottky diode clamp to prevent damage to the lower power FET devices. The MBRS320T3G diode is used on the ISL70003ASEHEV1Z evaluation platform.

Derating Current Capability

Most space programs issue specific derating guidelines for parts, but these guidelines take the pedigree of the part into account. For instance, a device built to MIL-PRF-38535, such as the ISL70003ASEH, is already heavily derated from a current density standpoint. However, a mil-temp or commercial IC that is up-screened for use in space applications may need additional current derating to ensure reliable operation because it was not built to the same standards as the ISL70003ASEH.

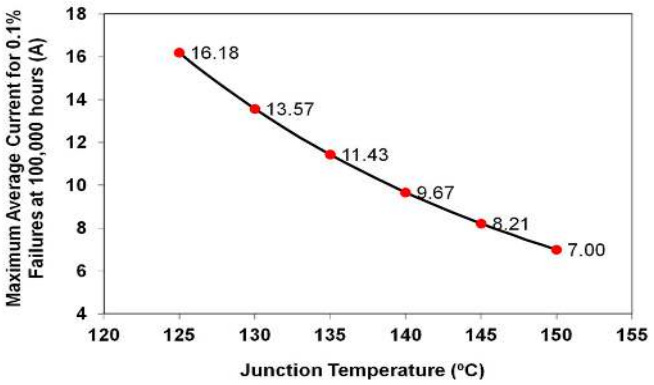


FIGURE 56. CURRENT vs TEMPERATURE

Figure 56 shows the wear out maximum average output current of the ISL70003ASEH with respect to junction temperature for 0.1% failure at 100k hours of operation. This plot takes into account the worst-case current share mismatch in the power blocks and the current density requirement of MIL-PRF-38535 (<$2x10^5$A/cm^2). The plot clearly shows that the ISL70003ASEH can handle 7A at +150°C from a worst-case current density standpoint, but the part is rated to 6A. Therefore, no further current derating of the ISL70003ASEH is needed.

General Design Guide

This design guide provides a high-level explanation of the steps necessary to design the power stage and feedback compensation network of a single-phase power converter. It is assumed that the reader is familiar with many of the basic skills and techniques in switch mode power supply design. In addition to this guide, an evaluation board that includes schematics, bills of materials, and board layout is provided.

Output Inductor Selection

The output inductor is selected to minimize the converter's response time to a load transient and meet steady-state output voltage ripple requirements. The inductor value determines the converter's inductor ripple current and the output voltage ripple is a function of the inductor ripple current. The output voltage ripple and the inductor ripple current are approximated by using Equation 13:

$$\Delta I = \frac{V_{IN} - V_{OUT}}{f_{SW} \times L} \times \frac{V_{OUT}}{V_{IN}} \qquad \Delta V_{OUT} = \Delta I \times ESR \qquad \text{(EQ. 13)}$$

Increasing the value of inductance reduces the ripple current and output voltage ripple. However, the large inductance values reduce the converter's response time to a load transient.

One of the parameters limiting the converter's response to a load transient is the time required to change the inductor current. The response time is the time required to slew the inductor current from an initial current value to the transient current level. During this interval the difference between the inductor current and the transient current level must be supplied by the output capacitor. Minimizing the response time can minimize the output capacitance required.

The response time to a transient is different for the application of load and the removal of load. Equation 14 gives the approximate response time interval for application and removal of a transient load.

$$t_{RISE} = \frac{L \times I_{TRAN}}{V_{IN} - V_{OUT}} \qquad t_{FALL} = \frac{L \times I_{TRAN}}{V_{OUT}} \qquad \text{(EQ. 14)}$$

I_{TRAN} is the transient load current step, t_{RISE} is the response time to the application of load, and t_{FALL} is the response time to the removal of load. The worst case response time can be either at the application or removal of load. Be sure to check both Equations 13 and 14 at the minimum and maximum output levels for the worst case response time.

Output Capacitor Selection

An output capacitor is required to filter the inductor current and supply the load transient current. The filtering requirements are a function of the switching frequency and the ripple current. The load transient requirements are a function of the slew rate (di/dt) and the magnitude of the transient load current. These requirements are generally met with a mix of capacitors and careful layout.

High-frequency capacitors initially supply the transient and slow the current load rate seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the Effective Series Resistance (ESR) and voltage rating requirements rather than actual capacitance requirements.

High-frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. The shape of the output voltage waveform during a load transient that represents the worst case loading conditions ultimately determine the number of output capacitors and their type. When this load transient is applied to the converter, most of the energy required by the load is initially delivered from the output capacitors. This is due to the finite amount of time required for the inductor current to slew up to the level of the output current required by the load. This phenomenon results in a temporary dip in the output voltage. At the very edge of the transient, the Equivalent Series Inductance (ESL) of each capacitor induces a spike that adds on top of the existing voltage drop due to the Equivalent Series Resistance (ESR).

After the initial spike, attributable to the ESR and ESL of the capacitors, the output voltage experiences sag. This sag is a direct consequence of the amount of capacitance on the output.

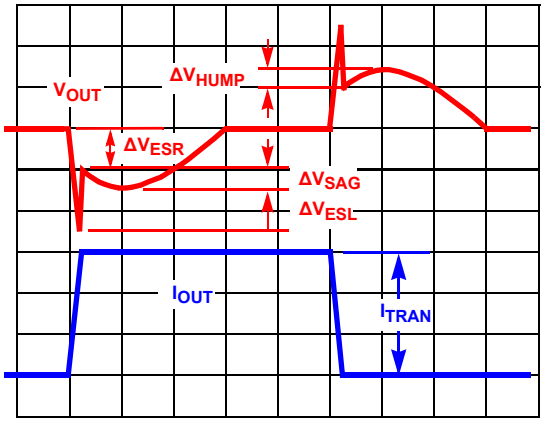


FIGURE 57. TYPICAL TRANSIENT RESPONSE

During the removal of the same output load, the energy stored in the inductor is dumped into the output capacitors. This energy dumping creates a temporary hump in the output voltage. This hump, as with the sag, can be attributed to the total amount of capacitance on the output. Figure 57 shows a typical response to a load transient.

The amplitudes of the different types of voltage excursions can be approximated using Equation 15.

$$\Delta V_{ESR} = ESR \times I_{tran} \qquad \Delta V_{ESL} = ESL \times \frac{dI_{tran}}{dt}$$

$$\Delta V_{SAG} = \frac{L_{OUT} \times I_{tran}^{2}}{C_{OUT} \times (V_{IN} - V_{OUT})}$$

$$\Delta V_{HUMP} = \frac{L_{OUT} \times I_{tran}^{2}}{C_{OUT} \times V_{OUT}} \qquad \text{(EQ. 15)}$$

where I_{tran} = Output load current transient and C_{OUT} = Total output capacitance

In a typical converter design, the ESR of the output capacitor bank dominates the transient response. The ESR and the ESL are typically the major contributing factors in determining the output capacitance. The number of output capacitors can be determined by using Equation 16, which relates the ESR and ESL of the capacitors to the transient load step and the voltage limit (ΔV_O).

$$\text{Number of Capacitors} = \frac{ESL \times \frac{dI_{tran}}{dt} + ESR \times I_{tran}}{\Delta V_o} \qquad \text{(EQ. 16)}$$

If ΔV_{SAG} and/or ΔV_{HUMP} are found to be too large for the output voltage limits, the amount of capacitance may need to be increased. In this situation, a trade-off between output inductance and output capacitance may be necessary.

The ESL of the capacitors, which is an important parameter in the previous equations, is not usually listed in datasheets. Practically, it can be approximated using Equation 17 if an Impedance vs Frequency curve is given for a specific capacitor:

$$ESL = \frac{1}{C(2\pi f_{res})^{2}} \qquad \text{(EQ. 17)}$$

where f_{res} is the frequency where the lowest impedance is achieved (resonant frequency).

The ESL of the capacitors becomes a concern when designing circuits that supply power to loads with high rates of change in the current.

Input Capacitor Selection

Use a mix of input bypass capacitors to control the voltage overshoot across the MOSFETs. Use small ceramic capacitors for high-frequency decoupling and bulk capacitors to supply the current needed each time the upper MOSFET turns on. Place the small ceramic capacitors physically close to the MOSFETs and between the drain of the upper MOSFET and the source of the lower MOSFET.

The important parameters for the bulk input capacitance are the voltage rating and the RMS current rating. For reliable operation, select bulk capacitors with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. Their voltage rating should be at least 1.25 times greater than the maximum input voltage, while a voltage rating of 1.5 times is a conservative guideline. For most cases, the RMS current rating requirement for the input capacitor of a buck regulator is approximately 1/2 the DC load current.

The maximum RMS current through the input capacitors may be closely approximated using Equation 18:

$$\sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(I_{OUT_{MAX}}^{2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) + \frac{1}{12} \times \left(\frac{V_{IN} - V_{OUT}}{Lxf_{OSC}} \times \frac{V_{OUT}}{V_{IN}} \right)^{2} \right)} \qquad \text{(EQ. 18)}$$

For surface mount designs, solid tantalum capacitors can be used, but caution must be exercised with regard to the capacitor surge current rating. These capacitors must be capable of handling the surge current at power-up. Some capacitor series available from reputable manufacturers are surge current tested.

Feedback Compensation

Figure 58 highlights the voltage-mode control loop for a synchronous rectified buck converter. The output voltage (V_{OUT}) is regulated to the reference voltage level. The Error Amplifier output (V_{EA}) is compared with the Oscillator (OSC) triangular wave to provide a Pulse-Width Modulated (PWM) wave with an amplitude of V_{IN} at the PHASE node. The PWM wave is smoothed by the output filter (L_O and C_O).

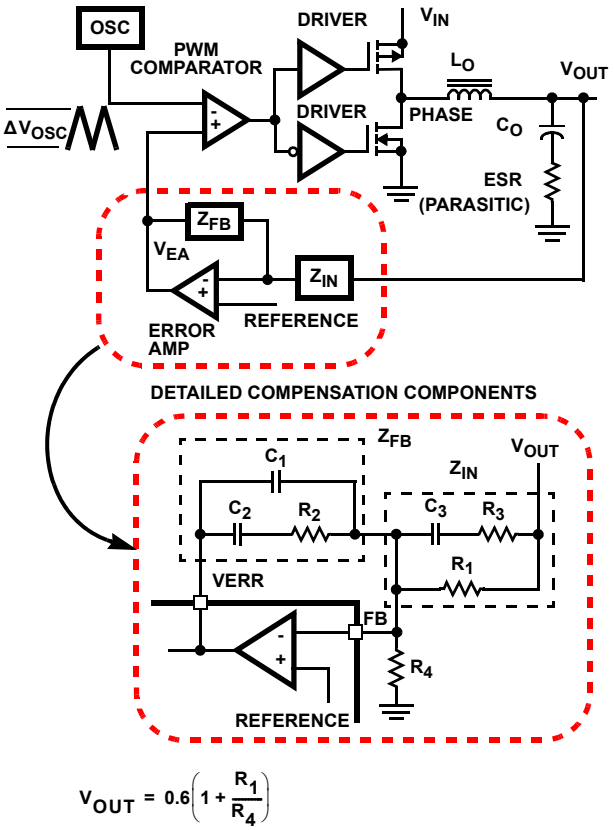


FIGURE 58. VOLTAGE-MODE BUCK CONVERTER COMPENSATION

The modulator transfer function is the small-signal transfer function of V_{OUT}/V_{EA}. This function is dominated by a DC Gain and the output filter (L_O and C_O), with a double pole break frequency at f_{LC} and a zero at f_{ESR}. The DC gain of the modulator is simply the input voltage (V_{IN}) divided by the peak-to-peak oscillator voltage ΔV_{OSC}. The ISL70003ASEH incorporates a feed-forward loop that accounts for changes in the input voltage. This maintains a constant modulator gain of 5, typical.

Modulator Break Frequency Equations

$$f_{LC} = \frac{1}{2\pi \times \sqrt{L_O \times C_O}} \qquad f_{ESR} = \frac{1}{2\pi \times ESR \times C_O} \qquad \text{(EQ. 19)}$$

The compensation network consists of the error amplifier and the impedance networks Z_{IN} and Z_{FB}. The goal of the compensation network is to provide a closed loop transfer function with the highest 0dB crossing frequency (f_{0dB}) and adequate phase margin. Phase margin is the difference between the closed loop phase at f_{0dB} and 180°.

Equation 20 relates the compensation network's poles, zeros, and gain to the components (R_1, R_2, R_3, C_1, C_2, and C_3) in Figure 58. Use these guidelines for locating the poles and zeros of the compensation network:

1. Pick gain (R_2/R_1) for desired converter bandwidth.
2. Place 1st zero below filter's double pole (~75% F_{LC}).
3. Place 2nd zero at filter's double pole.
4. Place 1st pole at the ESR zero.
5. Place 2nd pole at half the switching frequency.
6. Check gain against error amplifier's open-loop gain.
7. Estimate phase margin - repeat if necessary.

Compensation Break Frequency Equations

$$f_{Z1} = \frac{1}{2\pi \times R_2 \times C_2} \qquad f_{P1} = \frac{1}{2\pi \times R_2 \times \left(\frac{C_1 \times C_2}{C_1 + C_2}\right)}$$

$$f_{Z2} = \frac{1}{2\pi \times (R_1 + R_3) \times C_3} \qquad f_{P2} = \frac{1}{2\pi \times R_3 \times C_3}$$

(EQ. 20)

Figure 59 shows an asymptotic plot of the DC/DC converter's gain vs frequency. The actual modulator gain has a high gain peak due to the high Q factor of the output filter and is not shown in Figure 59. Using the guidelines provided should give a compensation gain similar to the curve plotted. The open-loop error amplifier gain bounds the compensation gain. Check the compensation gain at f_{P2} with the capabilities of the error amplifier. The closed-loop gain is constructed on the graph of Figure 59 by adding the modulator gain (in dB) to the compensation gain (in dB). This is equivalent to multiplying the modulator transfer function to the compensation transfer function and plotting the gain. The compensation gain uses external impedance networks Z_{FB} and Z_{IN} to provide a stable, high bandwidth (BW) overall loop. A stable control loop has a gain crossing with -20dB/decade slope and a phase margin greater than +45°. Include worst case component variations when determining phase margin. A more detailed explanation of voltage mode control of a buck regulator can be found in TB417, entitled "Designing Stable Compensation Networks for Single Phase Voltage Mode Buck Regulators".

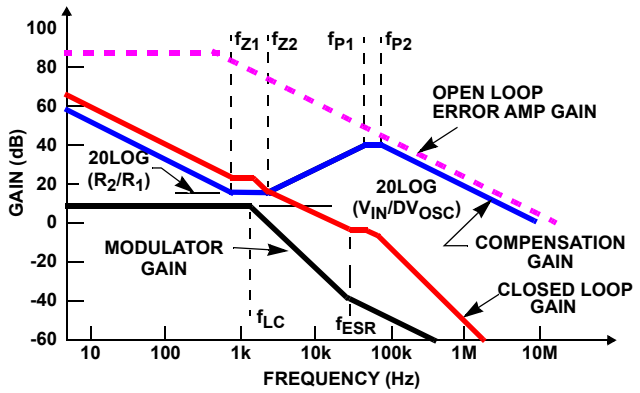


FIGURE 59. ASYMPTOTIC BODE PLOT OF CONVERTER GAIN

PCB Design

PCB design is critical to high frequency switching regulator performance. Careful component placement and trace routing are necessary to reduce voltage spikes and minimize undesirable voltage drops. Selection of a suitable thermal interface material is also required for optimum heat dissipation and to provide lead strain relief.

Optimize load regulation by reducing noise from the power and digital grounds into the analog ground by splitting ground into three planes: analog, digital, and power. Bypass or ground pins accordingly to their design preferred ground. See the "Pin Descriptions" on page 5 and Figure 4 on page 8 for guidance. Independently tie each of the analog and digital grounds to power ground through a single trace in a low noise area.

PCB Plane Allocation

A minimum of four layers of two ounce copper are recommended. Layer 2 should be a dedicated ground plane with all critical component ground connections made with vias to this layer. Layer 3 should be a dedicated power plane split between the input and output power rails. Layers 1 and 4 should be used primarily for signals but can also provide additional power and ground islands as required.

PCB Component Placement

Place components as close as possible to the IC to minimize stray inductance and resistance. Prioritize the placement of bypass capacitors on the pins of the IC in the order shown: REF, SS_CAP, AVDD, DVDD, PVINx (high-frequency capacitors), EN, PGOOD, PVINx (bulk capacitors).

Locate the output voltage resistive divider as close as possible to the FB pin of the IC. Connect the top leg of the divider directly to the output of the inductor through a Kelvin trace and the bottom leg of the divider directly to AGND pin. This AGND connection is also a Kelvin trace connected to the closest ground to the inductor output. Connect the junction of the resistive divider directly to the FB pin.

Place a Schottky clamp diode as close as possible to the LXx and PGNDx pins of the IC. A small series R-C snubber connected from the LXx pins to the PGNDx pins may be used to damp high-frequency ringing on the LXx pins, see Figure 60.

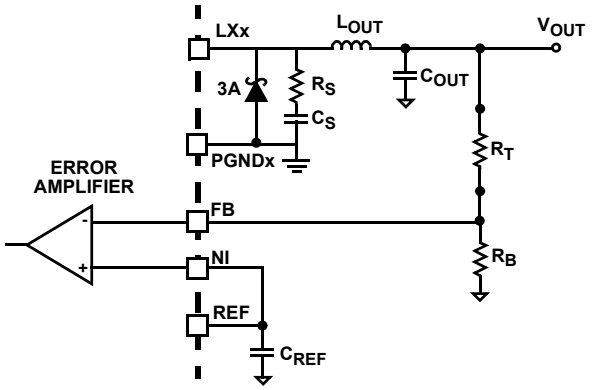


FIGURE 60. SCHOTTKY DIODE AND R-C SNUBBER

LX Connection

Use a small island of copper to connect the LXx pins of the IC to the output inductor on Layers 1 and 4. Void the copper on Layers 2 and 3 adjacent to the island to minimize capacitive coupling to the power and ground planes. Place most of the island on Layer 4 to minimize the amount of copper that must be voided from the ground plane (Layer 2).

Keep all other signal traces as short as possible.

Lead Strain Relief

The package leads protrude from the bottom of the package and the leads need forming to provide strain relief. On the heatsink option of the package R64.C, the lead forming should be made so that the bottom of the heatsink and the formed leads are flush.

Heatsink Mounting Guidelines

The R64.C package option has a heatsink mounted on the underside of the package. The following JESD-51x series guidelines may be used to mount the package:

1. Place a thermal land on the PCB under the heatsink.
2. The land should be approximately the same size as to 1mm larger than the 10.16x10.16mm heatsink.
3. Place an array of thermal vias below the thermal land.
   - Via array size: ~9x9 = 81 thermal vias.
   - Via diameter: ~0.3mm drill diameter with plated copper on the inside of each via.
   - Via pitch: ~1.2mm.
   - Vias should drop to and contact as much metal area as feasible to provide the best thermal path.

Heatsink Electrical Potential

The heatsink is connected to Pin 50 within the package, so the PCB design and potential applied to Pin 50 defines the heatsink potential.

Heatsink Mounting Materials

In the case of electrically conductive mounting methods (conductive epoxy, solder, etc.) the thermal land, vias, and connected plane(s) below must be the same potential as Pin 50.

In the case of electrically nonconductive mounting methods (nonconductive epoxy), the heatsink and Pin 50 could have different electrical potential than the thermal land, vias, and connected plane(s) below.

Package Characteristics

Weight of Packaged Device

2.65 Grams (typical) - R64.C Package

Lid Characteristics

Finish: Gold
Lid Potential: PGND

Die Characteristics

Die Dimensions

8300µm x 8300µm (327 mils x 327 mils)
Thickness: 300µm ±25.4µm (12 mils ±1 mil)

Interface Materials

GLASSIVATION

Type: Silicon Oxide and Silicon Nitride
Thickness: 0.3µm ±0.03µm to 1.2µm ±0.12µm

TOP METALLIZATION

Type: AlCu (99.5%/0.5%)
Thickness: 2.7µm ±0.4µm

BACKSIDE FINISH

Silicon

PROCESS

0.6µM BiCMOS Junction Isolated

ASSEMBLY RELATED INFORMATION

Substrate and Lid Potential

PGND

ADDITIONAL INFORMATION

Worst Case Current Density

$<2 \times 10^5$ A/cm^2

Transistor Count

26,144

Metallization Mask Layout

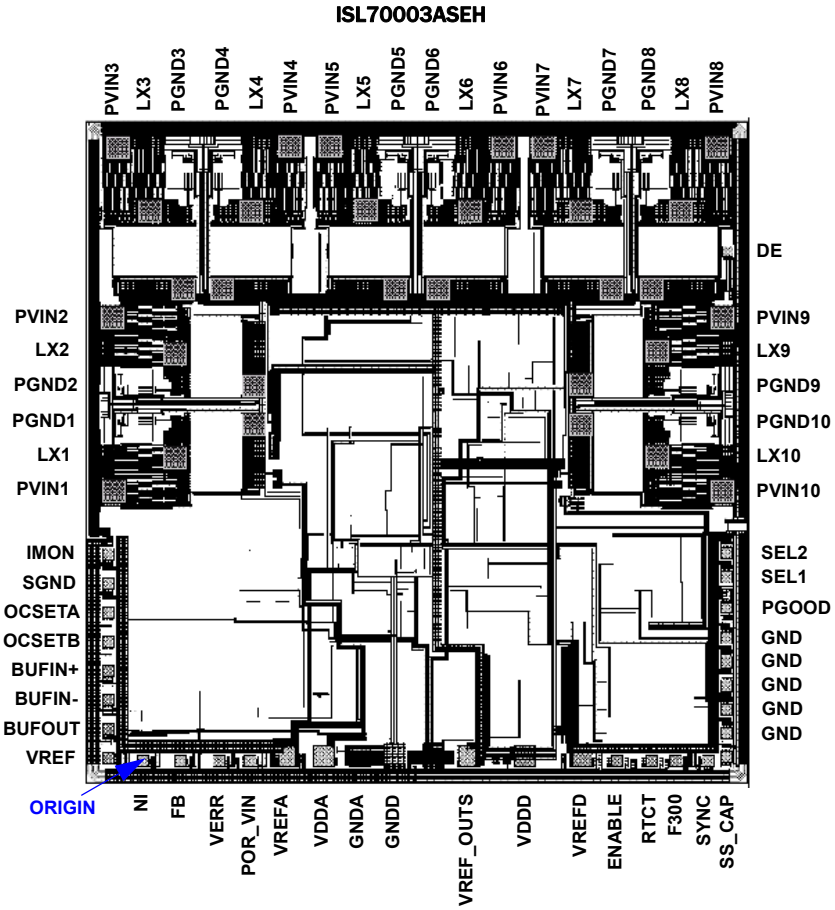


TABLE 2. LAYOUT X-Y COORDINATES

PAD NAME	PAD NUMBER	X (µm)	Y (µm)	dX (µm)	dY (µm)	BOND WIRES DIA (mil)
NI	1	0	0	135	135	1.5
FB	2	452	0	135	135	1.5
VERR	3	929	0	135	135	1.5
POR_VIN	4	1371	0	135	135	1.5
VREFA	5	1854	58	254	254	3
AVDD	6	2577	60	254	254	3
AGND	7	3104	60	254	254	3
DGND	8	3589	60	254	254	3
VREF_OUTS	9	4035	60	254	254	3
DVDD	10	4713	60	254	254	3
VREFD	11	5420	60	254	254	3
ENABLE	12	5846	0	135	135	1.5
RT/CT	13	6274	0	135	135	1.5
FSEL	14	6579	0	135	135	1.5
SYNC	15	6976	0	135	135	1.5
SS_CAP	16	7201	51	135	135	1.5
GND	17	7201	345	135	135	1.5
GND	18	7201	639	135	135	1.5
GND	19	7201	934	135	135	1.5
GND	20	7201	1228	135	135	1.5
GND	21	7201	1522	135	135	1.5
PGOOD	22	7201	1902	135	135	1.5
SEL1	23	7201	2275	135	135	1.5
SEL2	24	7201	2569	135	135	1.5
PVIN10	25	7140	3285	254	254	3
LX10	26	6350	3771	254	254	3
PGND10	27	5387	4179	254	254	3
PGND9	28	5387	4625	254	254	3
LX9	29	6350	5033	254	254	3
PVIN9	30	7140	5518	254	254	3
DE	31	7220	6303	135	135	1.5
PVIN8	32	7140	7578	254	254	3
LX8	33	6655	6788	254	254	3
PGND8	34	6247	5825	254	254	3
PGND7	35	5801	5825	254	254	3
LX7	36	5393	6788	254	254	3
PVIN7	37	4908	7578	254	254	3
PVIN6	38	4497	7578	254	254	3
LX6	39	4011	6788	254	254	3

TABLE 2. LAYOUT X-Y COORDINATES (Continued)

PAD NAME	PAD NUMBER	X (µm)	Y (µm)	dX (µm)	dY (µm)	BOND WIRES DIA (mil)
PGND6	40	3603	5825	254	254	3
PGND5	41	3157	5825	254	254	3
LX5	42	2749	6788	254	254	3
PVIN5	43	2264	7578	254	254	3
PVIN4	44	1853	7578	254	254	3
LX4	45	1367	6788	254	254	3
PGND4	46	960	5825	254	254	3
PGND3	47	514	5825	254	254	3
LX3	48	106	6788	254	254	3
PVIN3	49	-379	7578	254	254	3
PVIN2	50	-379	5518	254	254	3
LX2	51	411	5033	254	254	3
PGND2	52	1374	4625	254	254	3
PGND1	53	1374	4179	254	254	3
LX1	54	411	3771	254	254	3
PVIN1	55	-379	3285	254	254	3
IMON	56	-438	2561	135	135	1.5
SGND	57	-438	2201	135	135	1.5
OCSETA	58	-438	1841	135	135	1.5
OCSETB	59	-438	1481	135	135	1.5
BUFIN+	60	-438	1121	135	135	1.5
BUFIN-	61	-438	761	135	135	1.5
BUFOUT	62	-438	401	135	135	1.5
VREF	63	-438	41	135	135	1.5

Revision History

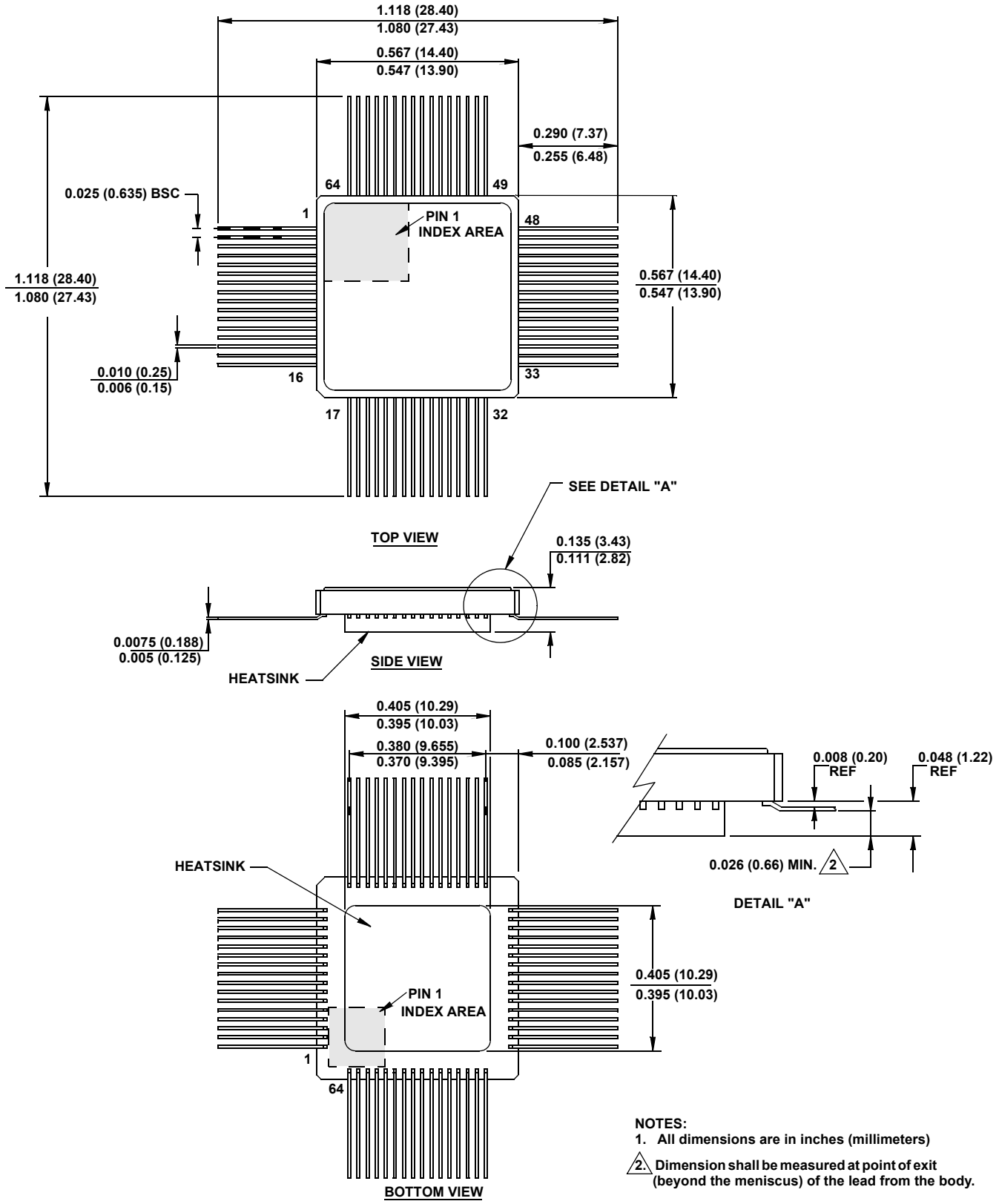
The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

DATE	REVISION	CHANGE
Dec 12, 2019	FN8746.4.01	Changed Tolerant to Hardened in the title to clarify internal semantic requirements. Updated LDR value from 100 to 50 in the features bullet on page1. Added Note 3 and the Radiation Hardness column to Ordering Information Table on page 4. Corrected typographical errors in the equations on page 28. Updated disclaimer.
Sep 13, 2018	FN8746.4	Updated Figures 4 and 5. Updated Note 3. Updated Figure 48 to more closely align with accompanying text context. Removed About Intersil section.
Dec 21, 2017	FN8746.3	Page 4: Added Notes 3 and 4 to Ordering Information table. Removed Table of Differences. Minor text edits throughout the document for clarification, expansion or related subject matter to parametric specifications.
Jan 5, 2017	FN8746.2	Added Table of Differences on page 4 Corrected ESD voltage clamp information on page 7. Clarified connections in Figure 4 on page 8 and Figure 5 on page 9. Clarified and expanded DDR Application section on page 25 and page 26. Corrected Figure 55 configuration on page 26.
May 12, 2016	FN8746.1	Updated Ordering information table on page 4. Updated Note 1. Removed Pb-Free Reflow reference under “Thermal Information” on page 10 as it is not applicable to hermetic packages. Corrected Equation 20 on page 29.
Aug 5, 2015	FN8746.0	Initial release

Package Outline Drawing

For the most recent package outline drawing, see R64.C.

R64.C
64 CERAMIC QUAD FLATPACK PACKAGE (CQFP) WITH BOTTOM HEATSINK
Rev 1, 10/13



NOTES:
1. All dimensions are in inches (millimeters)
2. Dimension shall be measured at point of exit (beyond the meniscus) of the lead from the body.

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(Rev.4.0-1 November 2017)

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