

HEXFET® Power MOSFET

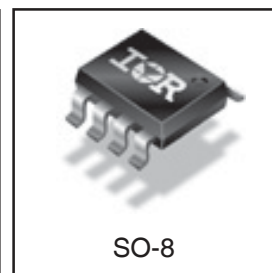
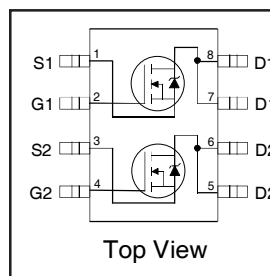
Applications

- High frequency DC-DC converters
- Lead-Free

V_{DS}	$R_{DS(on)}$ max	I_D
80V	73mΩ @ $V_{GS} = 10V$	3.6A

Benefits

- Low Gate to Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective C_{OSS} to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current



Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	80	V
V_{GS}	Gate-to-Source Voltage	± 20	
$I_D @ T_A = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V$	3.6	A
$I_D @ T_A = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V$	2.9	
I_{DM}	Pulsed Drain Current ①	29	
$P_D @ T_A = 25^\circ\text{C}$	Maximum Power Dissipation	2.0	W
	Linear Derating Factor	0.02	W/°C
dv/dt	Peak Diode Recovery dv/dt ②	2.3	V/ns
T_J	Operating Junction and	-55 to + 150	°C
T_{STG}	Storage Temperature Range		

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JL}$	Junction-to-Drain Lead	—	42	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) ④	—	62.5	

Notes ① through ⑥ are on page 8

Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	80	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.09	—	V/°C	Reference to 25°C, I _D = 1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	61	73	mΩ	V _{GS} = 10V, I _D = 2.2A ③
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA
I _{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	V _{DS} = 80V, V _{GS} = 0V
		—	—	250		V _{DS} = 64V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-200		V _{GS} = -20V

Dynamic @ T_J = 25°C (unless otherwise specified)

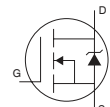
	Parameter	Min.	Typ.	Max.	Units	Conditions
g _{fs}	Forward Transconductance	4.3	—	—	S	V _{DS} = 25V, I _D = 2.2A
Q _g	Total Gate Charge	—	15	23		I _D = 2.2A
Q _{gs}	Gate-to-Source Charge	—	2.9	—	nC	V _{DS} = 40V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	4.5	—		V _{GS} = 10V ③
t _{d(on)}	Turn-On Delay Time	—	9.0	—		V _{DD} = 40V
t _r	Rise Time	—	10	—		I _D = 2.2A
t _{d(off)}	Turn-Off Delay Time	—	41	—	ns	R _G = 24Ω
t _f	Fall Time	—	17	—		V _{GS} = 10V ③
C _{iss}	Input Capacitance	—	660	—		V _{GS} = 0V
C _{oss}	Output Capacitance	—	110	—		V _{DS} = 25V
C _{rss}	Reverse Transfer Capacitance	—	15	—	pF	f = 1.0MHz
C _{oss}	Output Capacitance	—	710	—		V _{GS} = 0V, V _{DS} = 1.0V, f = 1.0MHz
C _{oss}	Output Capacitance	—	72	—		V _{GS} = 0V, V _{DS} = 64V, f = 1.0MHz
C _{oss} eff.	Effective Output Capacitance	—	140	—		V _{GS} = 0V, V _{DS} = 0V to 64V ③

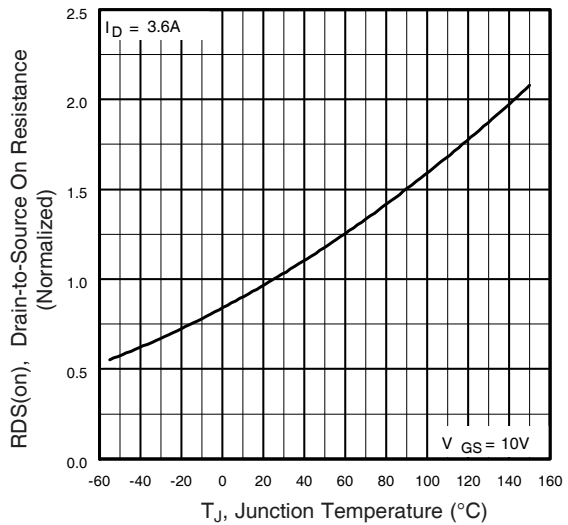
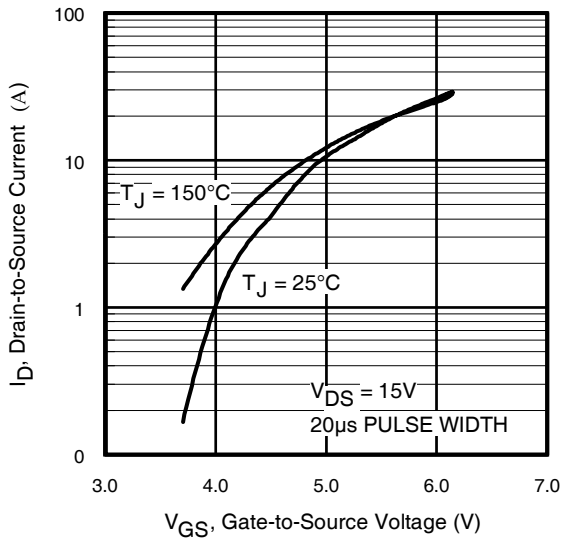
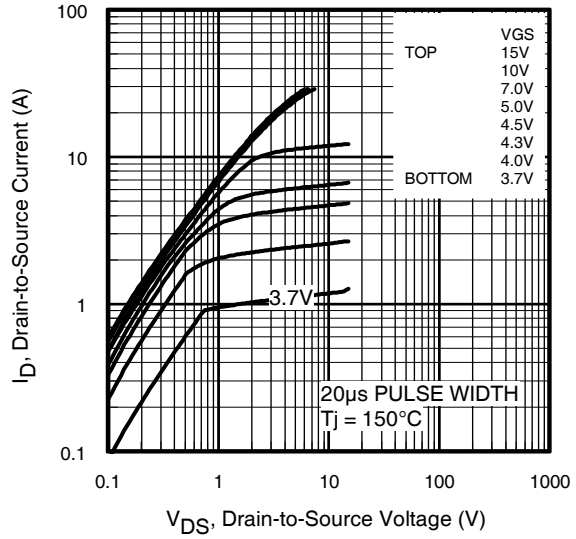
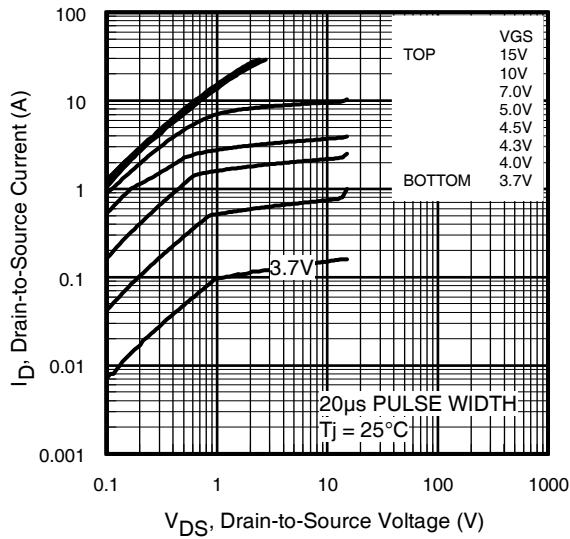
Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E _{AS}	Single Pulse Avalanche Energy ①②	—	75	mJ
I _{AR}	Avalanche Current ①	—	2.2	A

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	3.6	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	29	A	
V _{SD}	Diode Forward Voltage	—	—	1.3	V	T _J = 25°C, I _S = 2.2A, V _{GS} = 0V ③
t _{rr}	Reverse Recovery Time	—	50	—	ns	T _J = 25°C, I _F = 2.2A, V _{DD} = 40V
Q _{rr}	Reverse Recovery Charge	—	110	—	nC	di/dt = 100A/μs ③





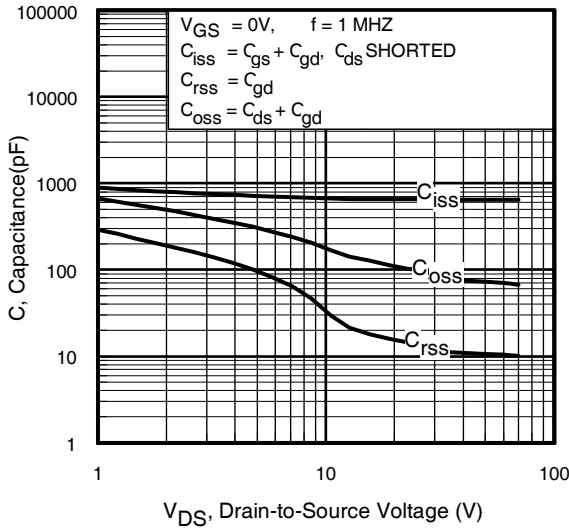


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

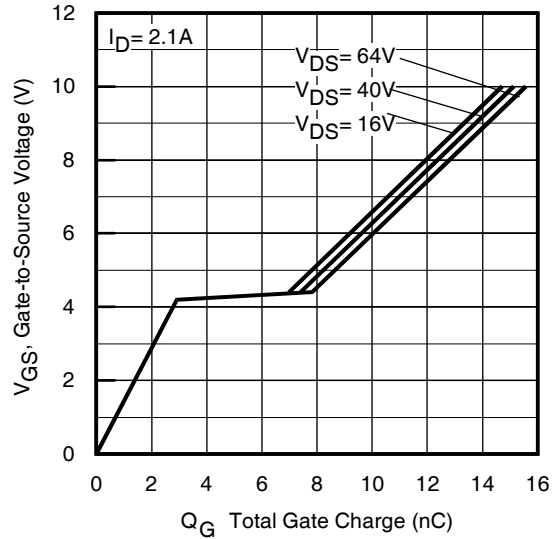


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

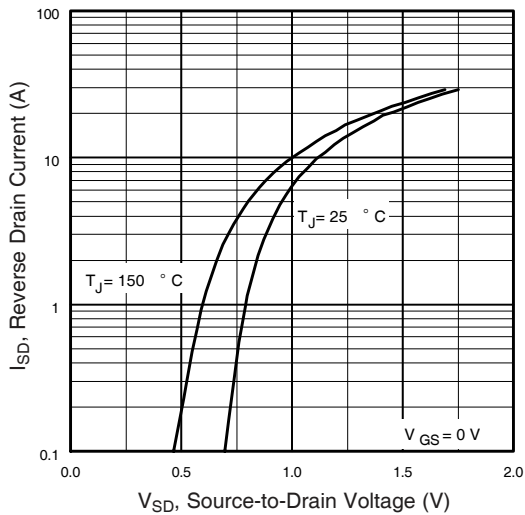


Fig 7. Typical Source-Drain Diode Forward Voltage

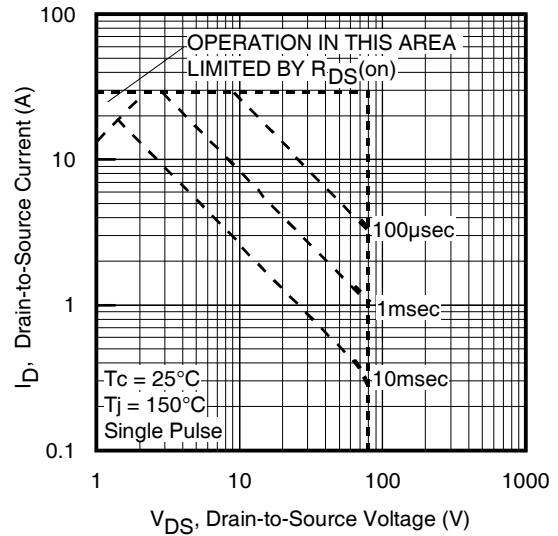


Fig 8. Maximum Safe Operating Area

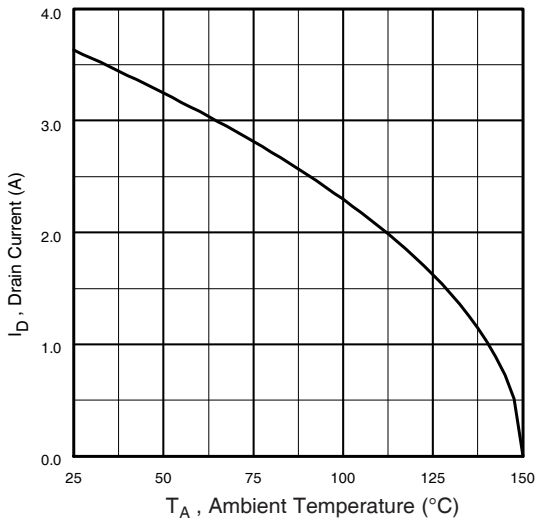


Fig 9. Maximum Drain Current Vs. Ambient Temperature

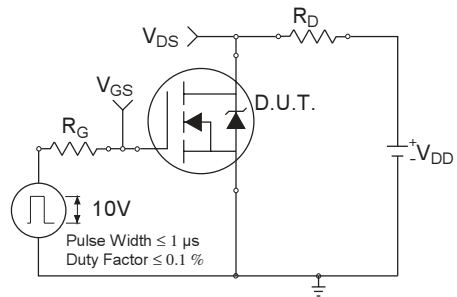


Fig 10a. Switching Time Test Circuit

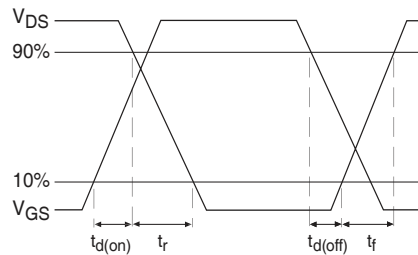


Fig 10b. Switching Time Waveforms

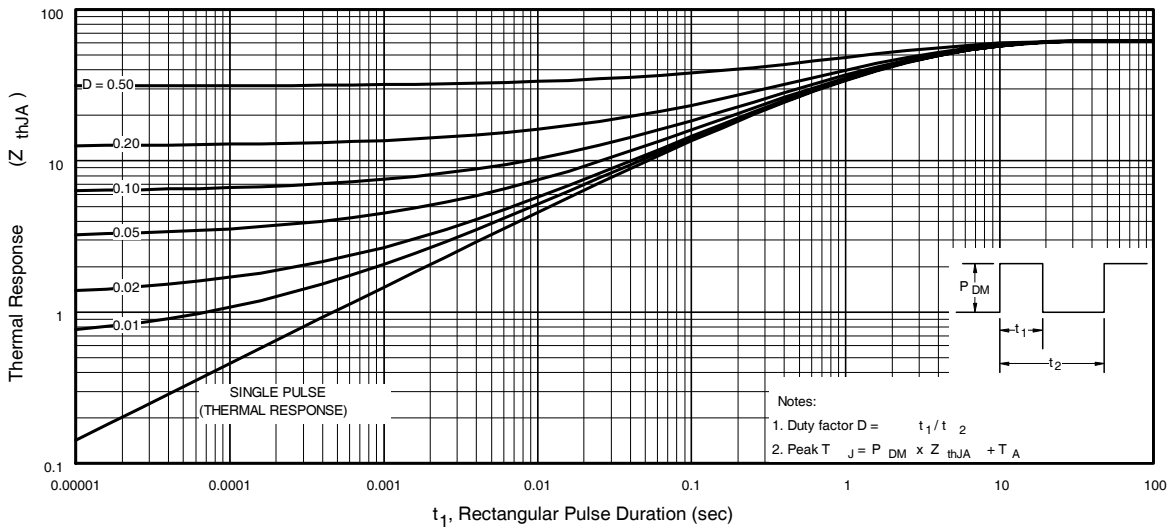


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

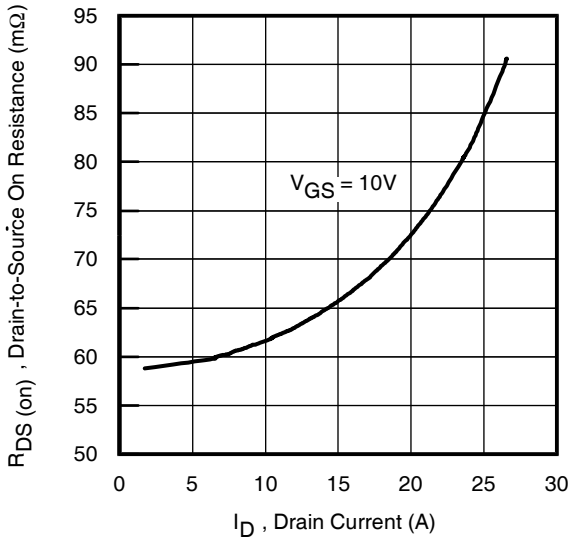


Fig 12. On-Resistance Vs. Drain Current

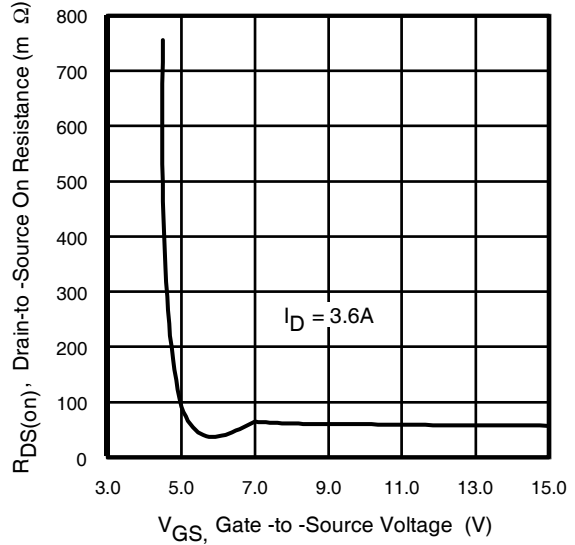


Fig 13. On-Resistance Vs. Gate Voltage

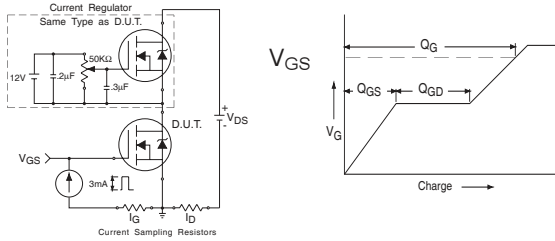


Fig 14a&b. Basic Gate Charge Test Circuit and Waveform

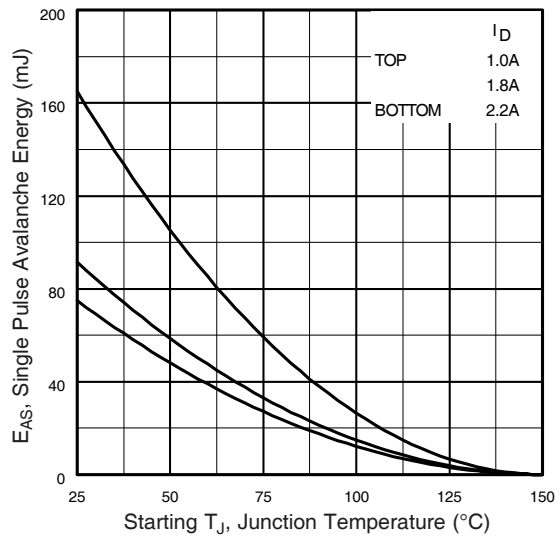


Fig 15c. Maximum Avalanche Energy Vs. Drain Current

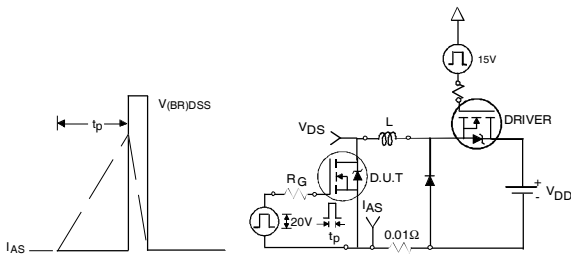


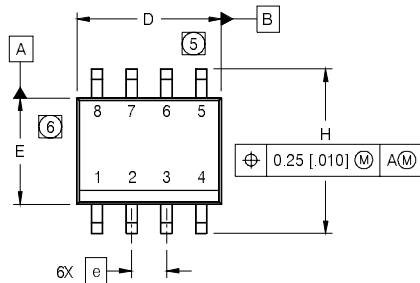
Fig 15a&b. Unclamped Inductive Test circuit and Waveforms



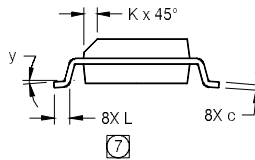
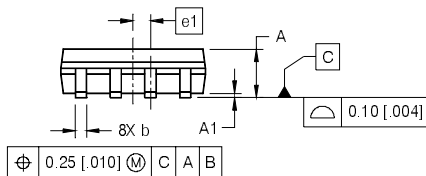
IRF7380PbF

SO-8 Package Outline (MOSFET & Fetky)

Dimensions are shown in millimeters (inches)



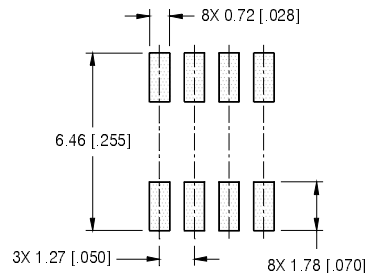
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°



NOTES:

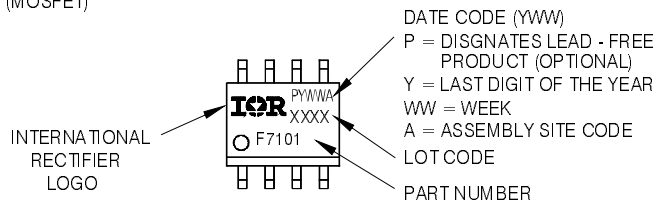
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
- ⑤ DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [0.006].
- ⑥ DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [0.010].
- ⑦ DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

FOOTPRINT



SO-8 Part Marking Information

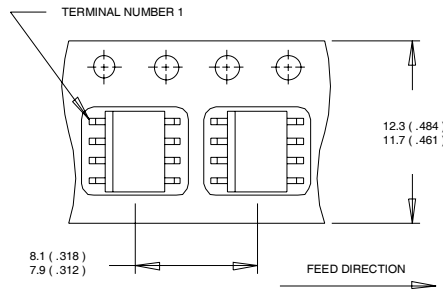
EXAMPLE: THIS IS AN IRF7101 (MOSFET)



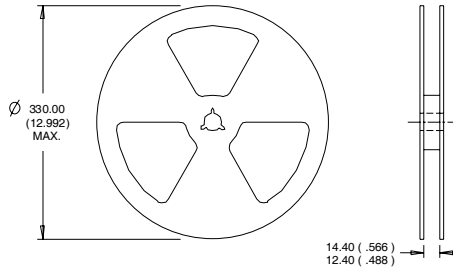
Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

SO-8 Tape and Reel

Dimensions are shown in millimeters (inches)



- NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
 2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
 3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



- NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
 2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 31\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 2.2\text{A}$.
- ③ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ④ When mounted on 1 inch square copper board.
- ⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑥ $I_{SD} \leq 2.2\text{A}$, $di/dt \leq 220\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 150^\circ\text{C}$.

Revision History

Date	Comments
09/16/2013	<ul style="list-style-type: none"> • Updated the R_{thja} from $50^\circ\text{C}/\text{W}$ to $62.5^\circ\text{C}/\text{W}$, on page 1. • Converted the data sheet to IR Corporate Template.

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