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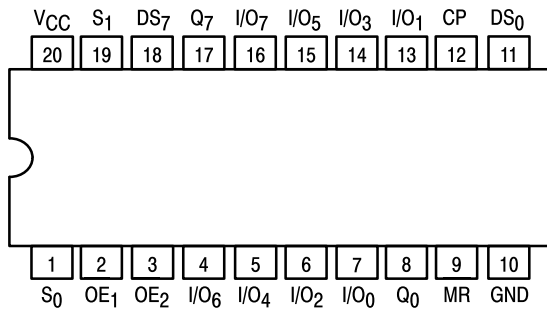
8-INPUT UNIVERSAL SHIFT/STORAGE REGISTER WITH COMMON PARALLEL I/O PINS

The MC74F299 is an 8-Bit Universal Shift/Storage Register with 3-state outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data.

The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Separate outputs are provided for flip-flops Q₀ and Q₇ to allow easy cascading. A separate active LOW Master Reset is used to reset the register.

- Common I/O for Reduced Pin Count
- Four Operation Modes: Shift left, Shift Right, Load and Store
- Separate Shift Right Serial Input and Shift Left Serial Input for Easy Cascading
- 3-State Outputs for Bus Oriented Applications
- Input Clamp Diodes Limit High-Speed Termination Effects

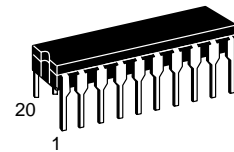
CONNECTION DIAGRAM



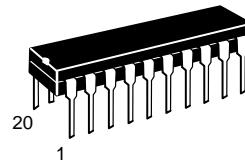
MC74F299

8-INPUT UNIVERSAL SHIFT/STORAGE REGISTER WITH COMMON PARALLEL I/O PINS

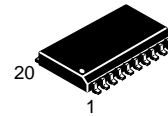
FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 732-03



N SUFFIX
PLASTIC
CASE 738-03



DW SUFFIX
SOIC
CASE 751D-03

ORDERING INFORMATION

MC74FXXXJ Ceramic
MC74FXXXN Plastic
MC74FXXXDW SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	74	0	25	70	°C
I _{OH}	Output Current — High	74			-1.0/-3.0	mA
I _{OL}	Output Current — Low	74			20/24	mA

MC74F299

FUNCTION TABLE

Inputs				Response
MR	S ₁	S ₀	CP	
L	X	X	X	Asynchronous Reset: Q ₀ –Q ₇ = LOW
H	H	H	↑	Parallel Load: I/O _n Q _n
H	L	H	↑	Shift Right: DS ₀ Q ₀ , Q ₀ Q ₁ , etc.
H	H	L	↑	Shift Left: DS ₇ Q ₇ , Q ₇ Q ₆ , etc.
H	L	L	X	Hold

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care
 ↑ = LOW-to-HIGH clock transition.

FUNCTIONAL DESCRIPTION

The MC74F299 is an 8-bit universal shift/storage register with 3-state outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Additional outputs are provided for flip-flops Q₀ and Q₇ to allow easy serial cascading. A separate active-LOW Master Reset is used to reset the register.

The MC74F299 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous shift left, shift right, parallel load and hold operations. The type of operation is determined by S₀ and S₁, as shown in the Function Table. All flip-flop outputs are brought out through 3-state buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q₀ and Q₇

are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on MR overrides the Select and CP inputs and resets the flip-flops. All other state changes are initiated by the rising edge of the clock. Inputs can change when the clock is in either state provided only that the recommended set-up and hold times, relative to the rising edge of CP, are observed.

A HIGH signal on either OE₁ or OE₂ disables the 3-state buffers and puts the I/O pins in the high impedance state. In this condition the shift, hold, load and reset operations can still occur. The 3-state buffers are also disabled by HIGH signals on both S₀ and S₁ in preparation for a parallel load operation.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions		
		Min	Typ	Max				
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage		
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage		
V _{IK}	Input Clamp Diode Voltage			-1.2	V	V _{CC} = MIN, I _{IN} = -18 mA		
V _{OH}	Output HIGH Voltage	Q ₀ /Q ₇	74	2.5		V	I _{OH} = -1.0 mA	V _{CC} = 4.5 V
			74	2.7				V _{CC} = 4.75 V
		I/O	74	2.7	3.4	V	I _{OH} = -3.0 mA	V _{CC} = 4.75 V
			74	2.4				V _{CC} = 4.5 V
V _{OL}	Output LOW Voltage	Q ₀ /Q ₇			V	I _{OL} = 20 mA	V _{CC} = MIN	
		I/O				I _{OL} = 24 mA		
I _{IH}	Input HIGH Current	Q ₀ /Q ₇			μA	V _{CC} = MAX, V _{IN} = 2.7 V		
		I/O					20	
		Q ₀ /Q ₇			mA	V _{CC} = MAX	V _{IN} = 7.0 V	
		I/O					1.0	V _{IN} = 5.5 V
I _{IL}	Input LOW Current	S ₀ , S ₁			mA	V _{CC} = MAX, V _{IN} = 0.5 V		
		Other Inputs					-1.2	
I _{OZH}	Off-State Output Current, High-Level Voltage Applied				70	μA	V _{CC} = MAX	V _{OUT} = 2.7 V
					1.0			mA
I _{OZL}	Off-State Output Current, Low-Level Voltage Applied				-0.6	mA	V _{CC} = MAX, V _{OUT} = 0.5 V	
I _{OS}	Output Short Circuit Current (Note 2)				-60	mA	V _{CC} = MAX	V _{OUT} = 0 V
I _{CC}	Total Supply Current				-150			OE = HIGH, CP = HIGH

NOTES:

- For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions for the applicable device type.
- Not more than one output should be shorted at one time, nor for more than 1 second.

MC74F299

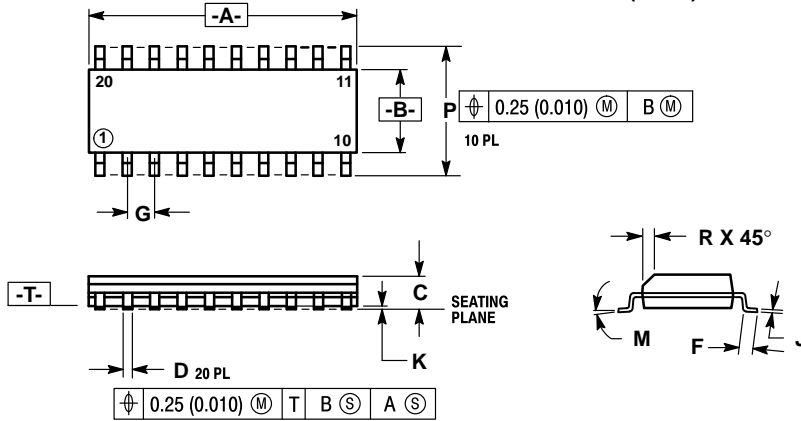
AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	74F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF		T _A = 0°C to +70°C V _{CC} = +5.0 V ±10% C _L = 50 pF		
		Min	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency	70		70		MHz
t _{PLH} t _{PHL}	Propagation Delay CP to Q ₀ or Q ₇	3.5 4.5	7.5 8.0	3.5 4.5	8.5 8.5	ns
t _{PLH} t _{PHL}	Propagation Delay CP to I/O _n	3.5 4.0	9.0 9.0	3.5 4.0	10 10	ns
t _{PHL}	Propagation Delay MR to Q ₀ or Q ₇	5.5	9.5	5.5	10.5	ns
t _{PHL}	Propagation Delay MR to I/O _n	5.5	10	5.5	10.5	ns
t _{PZH} t _{PZL}	Output Enable Time to HIGH or LOW Level	3.5 4.0	8.0 10	3.5 4.0	9.0 11	ns
t _{PHZ} t _{PLZ}	Output Disable Time to HIGH or LOW Level	2.0 1.0	7.0 5.5	2.0 1.0	8.0 6.5	ns

AC SETUP REQUIREMENTS

Symbol	Parameter	74F			74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF			T _A = 0°C to +70°C V _{CC} = +5.0 V ±10% C _L = 50 pF		
		Min	Typ	Max	Min	Max	
t _{s(H)} t _{s(L)}	Set-Up Time, HIGH or LOW S ₀ or S ₁ to CP	6.5 6.5			7.5 7.5		ns
t _{h(H)} t _{h(L)}	Hold Time, HIGH or LOW S ₀ or S ₁ to CP	0 0			0 0		ns
t _{s(H)} t _{s(L)}	Set-Up Time, HIGH or LOW I/O _n , DS ₀ , DS ₇ to CP	3.5 3.5			4.0 4.0		ns
t _{h(H)} t _{h(L)}	Hold Time, HIGH or LOW I/O _n , DS ₀ , DS ₇ to CP	0 1.0			0 1.0		ns
t _{w(H)} t _{w(L)}	CP Pulse Width, HIGH or LOW	5.0 4.5			5.0 4.5		ns
t _{w(L)}	MR Pulse Width LOW	4.5			4.5		ns
t _{rec}	Recovery Time MR to CP	4.0			4.0		ns

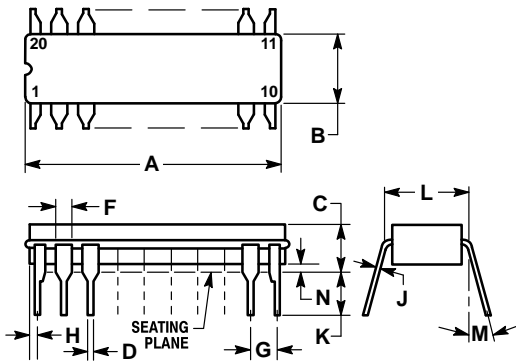
**Case 751D-03 DW Suffix
20-Pin Plastic
SO-20 (WIDE)**



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. 751D-01, AND -02 OBSOLETE, NEW STANDARD 751D-03.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC	0.050 BSC		
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

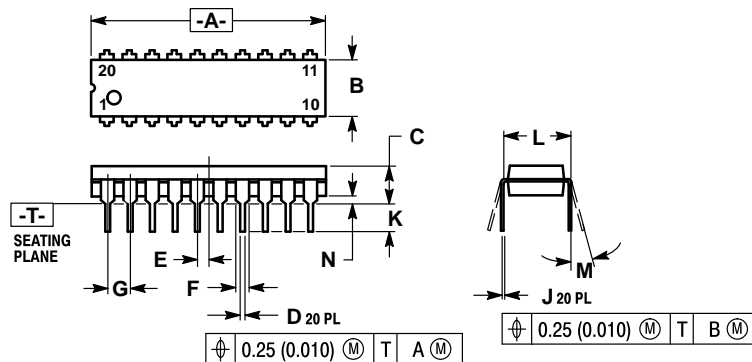
**Case 732-03 J Suffix
20-Pin Ceramic Dual In-Line**



- NOTES:
1. LEADS WITHIN 0.25 mm (0.010) DIA., TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
 2. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 3. DIM A AND B INCLUDES MENISCUS.


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	23.88	25.15	0.940	0.990
B	6.60	7.49	0.260	0.295
C	3.81	5.08	0.150	0.200
D	0.38	0.56	0.015	0.022
F	1.40	1.65	0.055	0.065
G	2.54 BSC	0.100 BSC		
H	0.51	1.27	0.020	0.050
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.62 BSC	0.300 BSC		
M	0°	15°	0°	15°
N	0.25	1.02	0.010	0.040

**Case 738-03 N Suffix
20-Pin Plastic**



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION "L" TO CENTER OF LEAD WHEN FORMED PARALLEL.
 4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
 5. 738-02 OBSOLETE, NEW STANDARD 738-03.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	25.66	27.17	1.010	1.070
B	6.10	6.60	0.240	0.260
C	3.81	4.57	0.150	0.180
D	0.39	0.55	0.015	0.022
E	1.27 BSC	0.050 BSC		
F	1.27	1.77	0.050	0.070
G	2.54 BSC	0.100 BSC		
J	0.21	0.38	0.008	0.015
K	2.80	3.55	0.110	0.140
L	7.62 BSC	0.300 BSC		
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

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