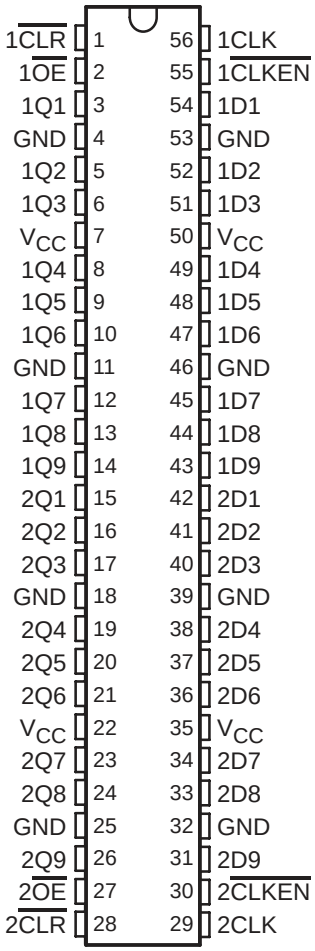
- **Members of the Texas Instruments Widebus™ Family**
- **Output Ports Have Equivalent 25-Ω Series Resistors So No External Resistors Are Required**
- **Typical V_{OLP} (Output Ground Bounce) <1 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Impedance State During Power Up and Power Down**
- **I_{off} and Power-Up 3-State Support Hot Insertion**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**

SN54ABT162823A . . . WD PACKAGE
SN74ABT162823A . . . DGG OR DL PACKAGE
(TOP VIEW)



description/ordering information

These 18-bit bus-interface flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

The ’ABT162823A devices can be used as two 9-bit flip-flops or one 18-bit flip-flop. With the clock-enable ($\overline{CLKEN}$) input low, the D-type flip-flops enter data on the low-to-high transitions of the clock. Taking $\overline{CLKEN}$ high disables the clock buffer, thus latching the outputs. Taking the clear ($\overline{CLR}$) input low causes the Q outputs to go low independently of the clock.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP − DL	Tube	SN74ABT162823ADL	ABT162823A
		Tape and reel	SN74ABT162823ADLR	
	TSSOP − DGG	Tape and reel	SN74ABT162823ADGGR	ABT162823A
−55°C to 125°C	CFP − WD	Tube	SNJ54ABT162823AWD	SNJ54ABT162823AWD

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

description/ordering information (continued)

A buffered output-enable ($\overline{OE}$) input places the nine outputs in either a normal logic state (high or low level) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components. $\overline{OE}$ does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The outputs, which are designed to source or sink up to 12 mA, include equivalent 25-Ω series resistors to reduce overshoot and undershoot.

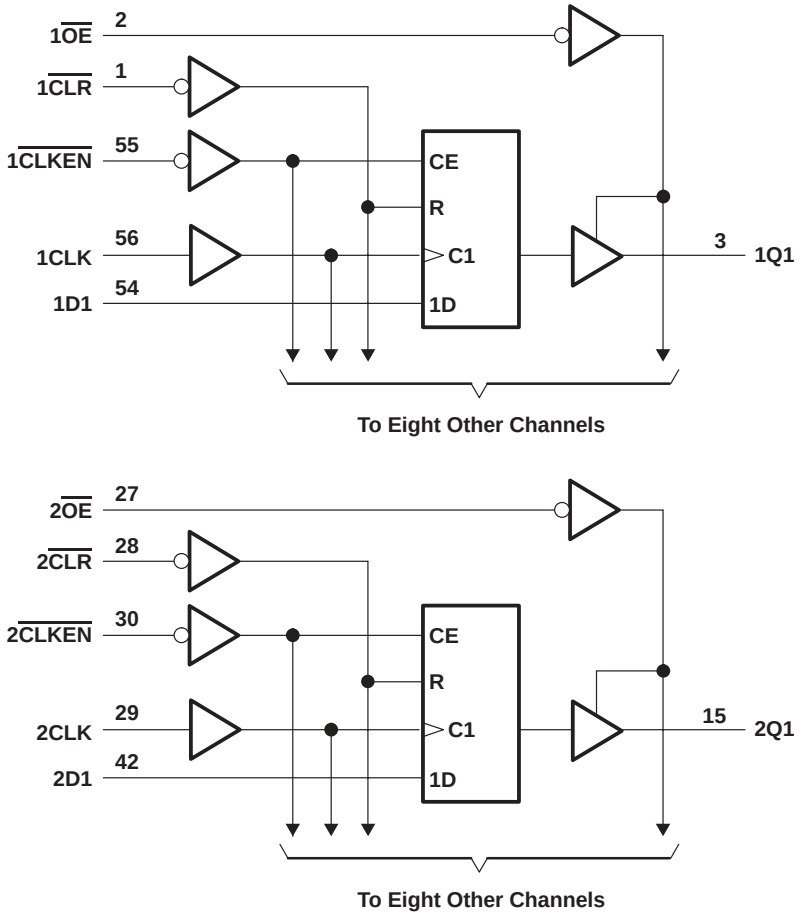
These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ shall be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE
(each 9-bit flip-flop)

INPUTS					OUTPUT
$\overline{OE}$	$\overline{CLR}$	$\overline{CLKEN}$	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	L	L	X	Q_0
L	H	H	X	X	Q_0
H	X	X	X	X	Z

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . −0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O . . . . . −0.5 V to 5.5 V
Current into any output in the low state, I_O . . . . . 30 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . −18 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . −50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package . . . . . 64°C/W
DL package . . . . . 56°C/W
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			SN54ABT162823A		SN74ABT162823A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−3		−12	mA
I_{OL}	Low-level output current			8		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Input transition rise or fall rate		200		200		µs/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A = 25°C			SN54ABT162823A		SN74ABT162823A		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = −1 mA	3			3		3		
	V_{CC} = 4.5 V	I_{OH} = −3 mA	2.4			2.4		2.4		
		I_{OH} = −12 mA	2*					2		
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 8 mA		0.4			0.8		0.65	V
		I_{OL} = 12 mA			0.8*				0.8	
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or GND			±1		±1		±1	µA
I_{OZPU}	V_{CC} = 0 to 2.1 V, V_O = 0.5 V to 2.7 V, $\overline{OE}$ = X				±50		±50		±50	µA
I_{OZPD}	V_{CC} = 2.1 V to 0, V_O = 0.5 V to 2.7 V, $\overline{OE}$ = X				±50		±50		±50	µA
I_{OZH}‡	V_{CC} = 5.5 V,	V_O = 2.7 V			10		10		10	µA
I_{OZL}‡	V_{CC} = 5.5 V,	V_O = 0.5 V			−10		−10		−10	µA
I_{off}	V_{CC} = 0,	V_I or V_O ≤ 4.5 V			±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50		50		50	µA
I_O§	V_{CC} = 5.5 V,	V_O = 2.5 V	−25	−55	−100	−25	−100	−25	−100	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			0.5		0.5		0.5	mA
		Outputs low			80		80		80	
		Outputs disabled			0.5		0.5		0.5	
ΔI_{CC}¶	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V			3.5						pF
C_o	V_O = 2.5 V or 0.5 V			9						pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† All typical values are at V_{CC} = 5 V.
‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL-voltage level, rather than V_{CC} or GND.

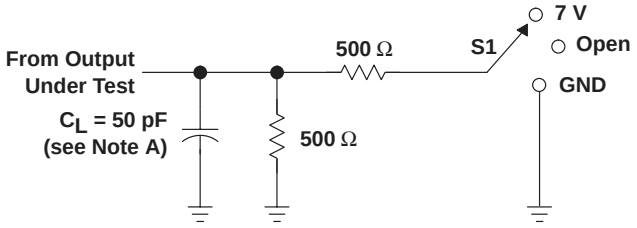
timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			V_{CC} = 5 V, T_A = 25°C		SN54ABT162823A		SN74ABT162823A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			150		150		150	MHz
t_w	Pulse duration	$\overline{CLR}$ low	3.3		3.3		3.3		ns
		CLK high or low	3.3		3.3		3.3		
t_{su}	Setup time before CLK↑	$\overline{CLR}$ inactive	1.6		2		1.6		ns
		Data	2		2		2		
		$\overline{CLKEN}$ low	2.8		2.8		2.8		
t_h	Hold time after CLK↑	Data	1.2		1.2		1.2		ns
		$\overline{CLKEN}$ low	0.6		0.6		0.6		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

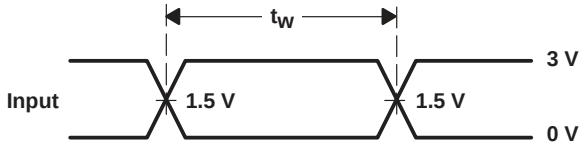
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT162823A		SN74ABT162823A		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			150			150		150		MHz
t_{PLH}	CLK	Q	2.3	4.6	6.2	2.3	8.4	2.3	7.5	ns
t_{PHL}			2.8	4.6	6.1	2.8	7.1	2.8	6.7	
t_{PHL}	$\overline{CLR}$	Q	2.8	5	6.3	2.8	7.2	2.8	7	ns
t_{PZH}	$\overline{OE}$	Q	1.7	3.8	5	1.7	5.8	1.7	5.9	ns
t_{PZL}			3	5	6.1	3	7.2	3	7	
t_{PHZ}	$\overline{OE}$	Q	2.6	4.8	6.1	2.6	7.3	2.6	6.6	ns
t_{PLZ}			1.9	4.6	6.7	1.9	10.2	1.9	9	

PARAMETER MEASUREMENT INFORMATION

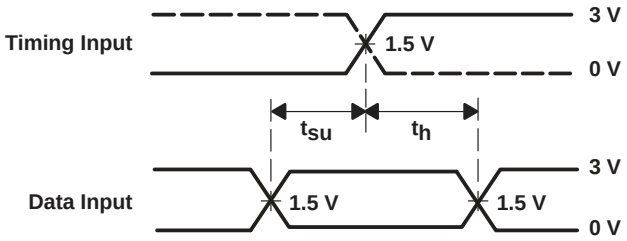


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

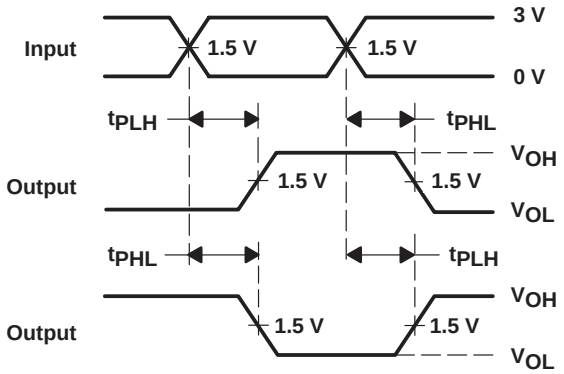
LOAD CIRCUIT



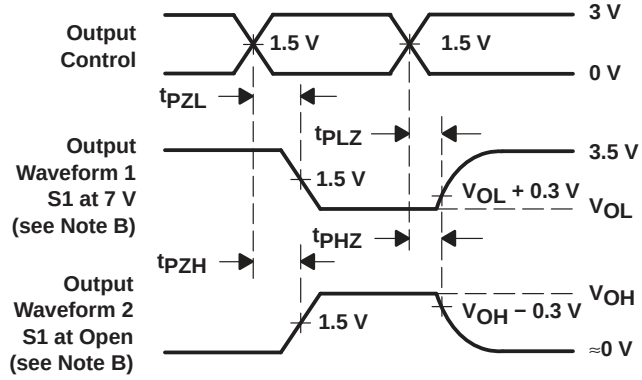
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74ABT162823ADGGRE4	ACTIVE	TSSOP	DGG	56		TBD	Call TI	Call TI	-40 to 85		Samples
74ABT162823ADGGRG4	ACTIVE	TSSOP	DGG	56		TBD	Call TI	Call TI	-40 to 85		Samples
SN74ABT162823ADGGR	OBSOLETE	TSSOP	DGG	56		TBD	Call TI	Call TI	-40 to 85		
SN74ABT162823ADL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT162823A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

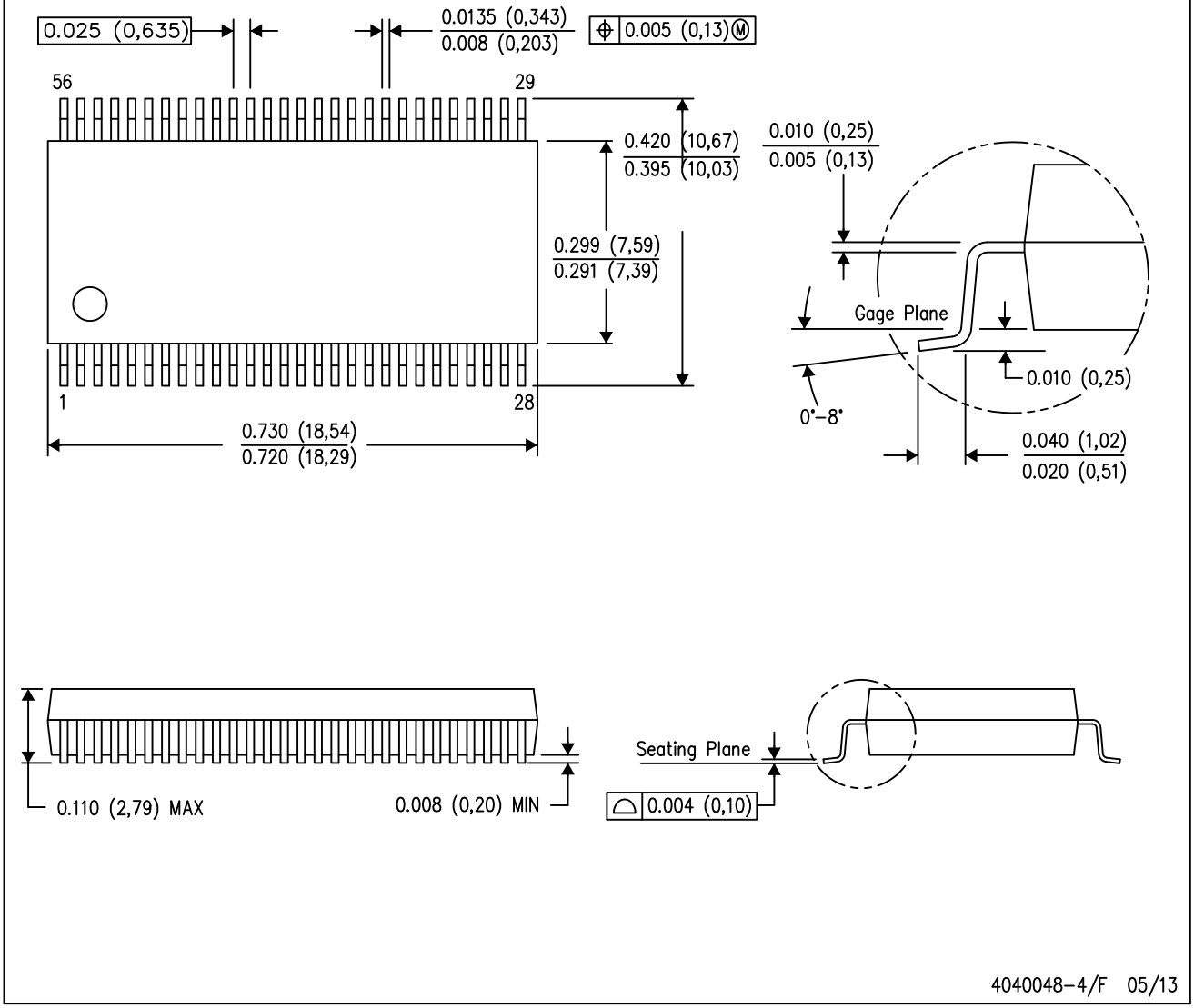
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

DL (R–PDSO–G56) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO–118

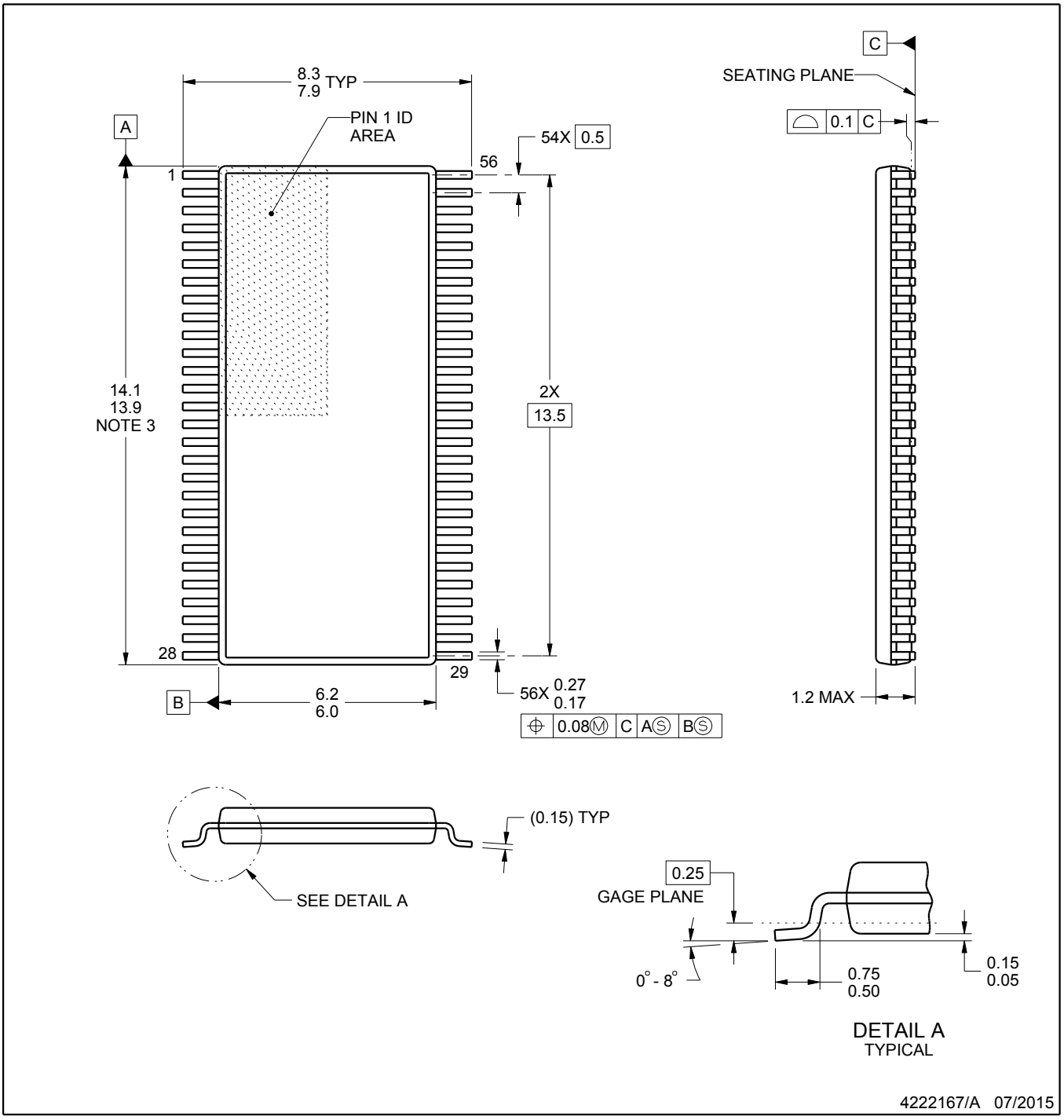
PowerPAD is a trademark of Texas Instruments.

PACKAGE OUTLINE

DGG0056A

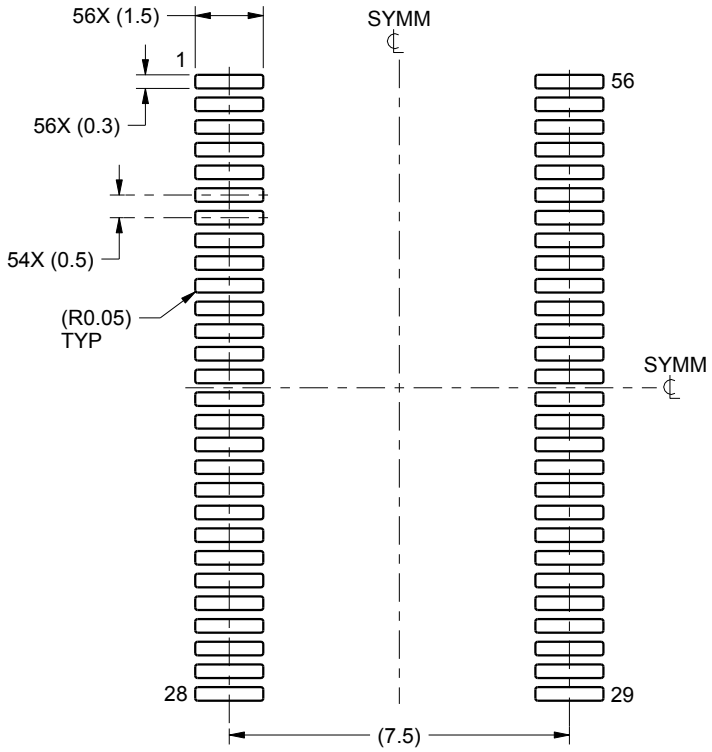
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

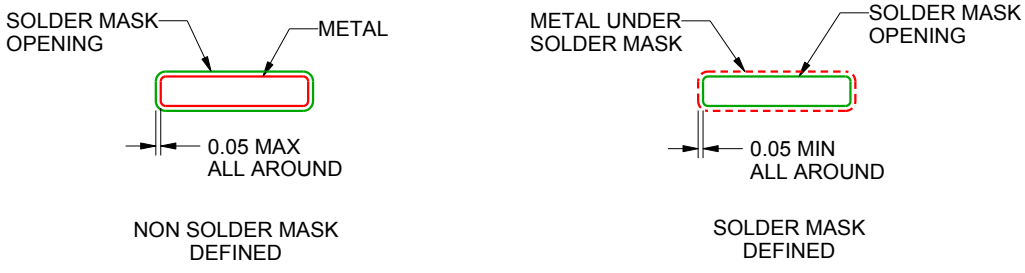


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
SCALE:6X

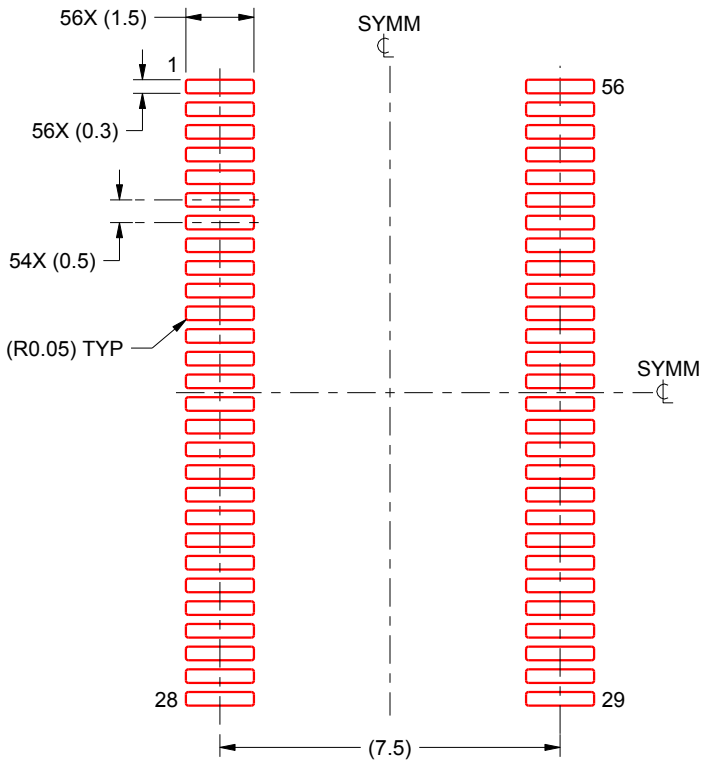


SOLDER MASK DETAILS

4222167/A 07/2015

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4222167/A 07/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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