TinyLogic HS Inverter

NC7S04

Description

The NC7S04 is a single high performance CMOS Inverter. Advanced Silicon Gate CMOS fabrication assures high speed and low power circuit operation over a broad V_{CC} range. ESD protection diodes inherently guard both input and output with respect to the V_{CC} and GND rails. Three stages of gain between input and output assures high noise immunity and reduced sensitivity to input edge rate.

Features

- Space−Saving SOT23−5, SC−74A and SC−88A 5−Lead Package
- Ultra−Small MicroPak™ Leadless Package
- High Speed: t_{PD} = 3 ns Typ
- Low Quiescent Power: I_{CC} < 1 μA
- Balanced Output Drive: 2 mA I_{OL}, −2 mA I_{OH}
- Broad V_{CC} Operating Range: 2 V – 6 V
- Balanced Propagation Delays
- Specified for 3 V Operation
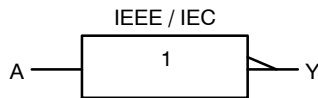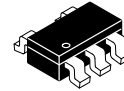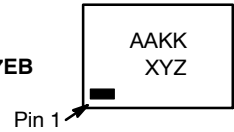- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant
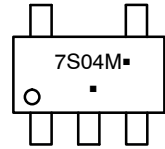

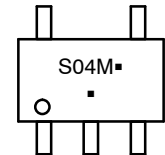
Figure 1. Logic Symbol

MARKING DIAGRAMS

SIP6 CASE 127EB	AAKK XYZ (Pin 1)
SC−74A CASE 318BQ	7S04M■
SOT23−5 CASE 527AH	7S04M
SC−88A CASE 419A−02	S04M■
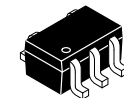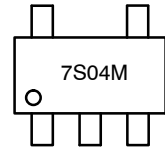
AA, 7S04, S04 = Specific Device Code
KK = 2−Digit Lot Run Traceability Code
XY = 2−Digit Date Code Format
Z = Assembly Plant Code
M = Date Code*

*Date Code orientation and/or position may vary depending upon manufacturing location.

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.
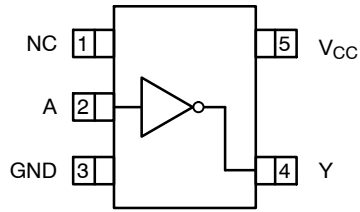
NC7S04

Pin Configurations

Figure 2. SOT23−5, SC−88A and SC−74A
(Top View)
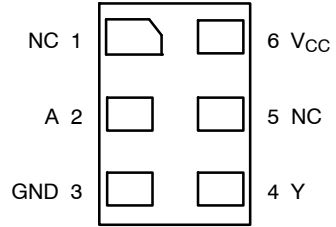
Figure 3. MicroPak (Top Through View)

PIN DESCRIPTIONS

Name	Description
A	Input
Y	Output
NC	No Connect

FUNCTION TABLE $(Y = \overline{A})$

Input	Output
A	**Y**
L	H
H	L

H = HIGH Logic Level
L = LOW Logic Level

NC7S04

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage		−0.5	6.5	V
I_{IK}	DC Input Diode Current	$V_{IN} < 0$ V	–	−20	mA
		$V_{IN} > V_{CC}$	–	+20	
V_{IN}	DC Input Voltage		−0.5	$V_{CC} + 0.5$	V
I_{OK}	DC Output Diode Current	$V_{OUT} < 0$ V	–	−20	mA
		$V_{OUT} > V_{CC}$	–	+20	
V_{OUT}	DC Output Voltage		−0.5	$V_{CC} + 0.5$	V
I_{OUT}	DC Output Source or Sink Current		–	±12.5	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current per Output Pin		–	±25	mA
T_{STG}	Storage Temperature		−65	+150	°C
T_J	Junction Temperature		–	+150	°C
T_L	Lead Temperature (Soldering, 10 Seconds)		–	+260	°C
P_D	Power Dissipation in Still Air	SC−74A / SOT23−5	–	390	mW
		SC−88A	–	332	
		MicroPak−6	–	812	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage		2.0	6.0	V
V_{IN}	Input Voltage		0	V_{CC}	V
V_{OUT}	Output Voltage		0	V_{CC}	V
T_A	Operating Temperature		−40	+85	°C
t_r, t_f	Input Rise and Fall Times	V_{CC} at 2.0 V	0	20	ns/V
		V_{CC} at 3.0 V	0	20	
		V_{CC} at 4.5 V	0	10	
		V_{CC} at 6.0 V	0	5	
θ_{JA}	Thermal Resistance	SC−74A / SOT23−5	–	320	°C/W
		SC−88A	–	377	
		MicroPak−6	–	154	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
1. Unused inputs must be held HIGH or LOW. They may not float.

DC ELECTICAL CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = +25°C			T_A = −40 to +85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	HIGH Level Input Voltage	2.0 3.0 – 6.0		1.50 0.7 V_{CC}	– –	– –	1.50 0.7 V_{CC}	– –	V
V_{IL}	LOW Level Input Voltage	2.0 3.0 – 6.0		– –	– –	0.50 0.3 V_{CC}	– –	0.50 0.3 V_{CC}	V
V_{OH}	HIGH Level Output Voltage	2.0 3.0 4.5 6.0	I_{OH} = −20 μA V_{IN} = V_{IH} or V_{IL}	1.90 2.90 4.40 5.90	2.0 3.0 4.5 6.0	– – – –	1.90 2.90 4.40 5.90	– – – –	V
		3.0 4.5 6.0	V_{IN} = V_{IH} or V_{IL} I_{OH} = −1.3 mA I_{OH} = −2.0 mA I_{OH} = −2.6 mA	2.68 4.18 5.68	2.85 4.35 5.85	– – –	2.63 4.13 5.63	– – –	V
V_{OL}	LOW Level Output Voltage	2.0 3.0 4.5 6.0	I_{OL} = 20 μA V_{IN} = V_{IH} or V_{IL}	– – – –	0.0 0.0 0.0 0.0	0.10 0.10 0.10 0.10	– – – –	0.10 0.10 0.10 0.10	V
		3.0 4.5 6.0	V_{IN} = V_{IH} or V_{IL} I_{OL} = 1.3 mA I_{OL} = 2.0 mA I_{OL} = 2.6 mA	– – –	0.1 0.1 0.1	0.26 0.26 0.26	– – –	0.33 0.33 0.33	V
I_{IN}	Input Leakage Current	6.0	V_{IN} = V_{CC}, GND	–	–	±0.1	–	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	V_{IN} = V_{CC}, GND	–	–	1.0	–	10.0	μA

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = +25°C			T_A = −40 to +85°C		Unit
				Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay (Figure 4, 6)	5.0	C_L = 15 pF	–	3.0	15.0	–	–	ns
		2.0 3.0 4.5 6.0	C_L = 50 pF	– – – –	18.0 10.0 7.0 6.0	100.0 27.0 20.0 17.0	– – – –	125.0 35.0 25.0 21.0	ns
t_{TLH}, t_{THL}	Output Transition Time (Figure 4, 6)	5.0	C_L = 15 pF	–	3.0	10.0	–	–	ns
		2.0 3.0 4.5 6.0	C_L = 50 pF	– – – –	25.0 16.0 11.0 9.0	125.0 35.0 25.0 21.0	– – – –	155.0 45.0 31.0 26.0	ns
C_{IN}	Input Capacitance (Figure 4, 6)	Open		–	2.0	10.0	–	10.0	pF
C_{PD}	Power Dissipation Capacitance (Figure 5)	5.0	(Note 2)	–	6.0	–	–	–	pF

2. C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. C_{PD} is related to I_{CCD} dynamic operating current by the expression:
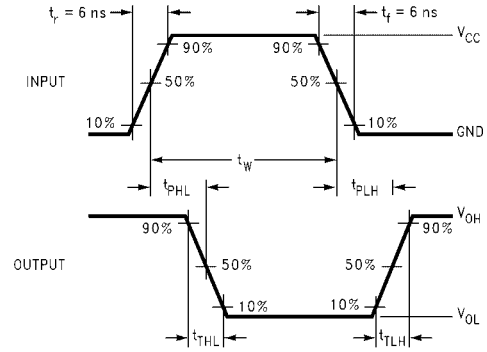I_{CCD} = (C_{PD}) (V_{CC}) (f_{IN}) + (I_{CC}static).

NC7S04

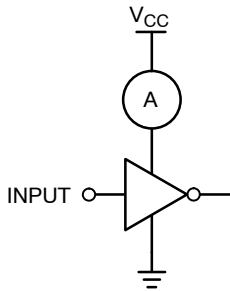**AC Loading and Waveforms**
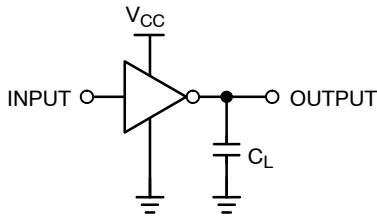
C_L includes load and stray capacitance
Input PRR = 1.0 MHz, t_w = 500 ns

Figure 4. AC Test Circuit

Figure 6. AC Waveforms

Input = AC Waveforms;
PRR = Variable; Duty Cycle = 50%.

Figure 5. I_{CCD} Test Circuit

DEVICE ORDERING INFORMATION

Device	Top Mark	Packages	Shipping[†]
NC7S04M5X	7S04	SC−74A	3000 / Tape & Reel
NC7S04M5X−L22090	7S04	SOT23−5	3000 / Tape & Reel
NC7S04P5X	S04	SC−88A	3000 / Tape & Reel
NC7S04P5X−L22057	S04	SC−88A	3000 / Tape & Reel
NC7S04L6X	AA	SIP6, MicroPak	5000 / Tape & Reel
NC7S04L6X−L22175	AA	SIP6, MicroPak	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

SIP6 1.45X1.0
CASE 127EB
ISSUE O

DATE 31 AUG 2016

TOP VIEW

PIN 1 IDENTIFIER
5

RECOMMENED
LAND PATTERN

PIN 1

BOTTOM VIEW

DETAIL A

DETAIL A
PIN 1 TERMINAL

0.075 X 45° CHAMFER

NOTES:
1. CONFORMS TO JEDEC STANDARD MO-252 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-2009
4. PIN ONE IDENTIFIER IS 2X LENGTH OF ANY OTHER LINE IN THE MARK CODE LAYOUT.

DOCUMENT NUMBER:	98AON13590G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	SIP6 1.45X1.0		PAGE 1 OF 1

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®
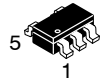
SC−74A
CASE 318BQ
ISSUE B

DATE 18 JAN 2018

SCALE 2:1

5X **b**

⊕ | 0.20 | C | A | B

E1

5 4

○1 2 3

B

A D

E

e

TOP VIEW

| 0.05 | A1

L

M

DETAIL A

A

C **SEATING PLANE**

SIDE VIEW

DETAIL A

c **END VIEW**
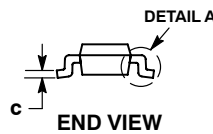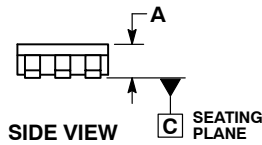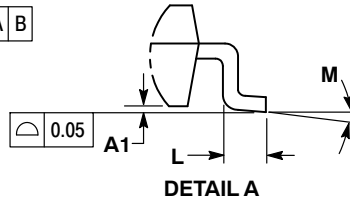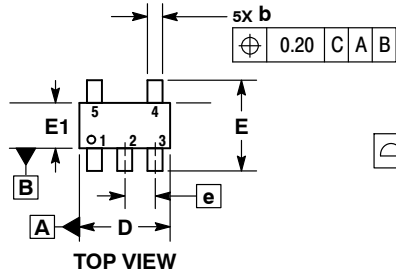
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.

	MILLIMETERS	
DIM	MIN	MAX
A	0.90	1.10
A1	0.01	0.10
b	0.25	0.50
c	0.10	0.26
D	2.85	3.15
E	2.50	3.00
E1	1.35	1.65
e	0.95 BSC	
L	0.20	0.60
M	0 °	10 °

RECOMMENDED SOLDERING FOOTPRINT*
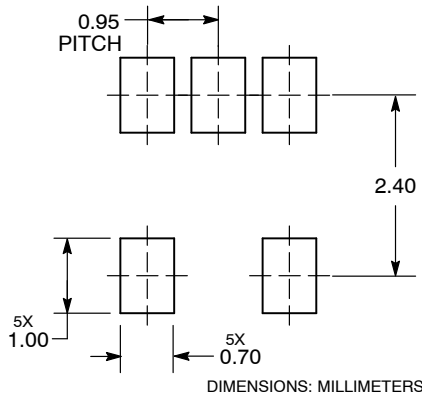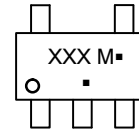
0.95 PITCH

2.40

5X 1.00

5X 0.70

DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*

XXX M▪

○ ▪

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	98AON66279G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	SC−74A		**PAGE 1 OF 1**

SC-88A (SC-70-5/SOT-353)
CASE 419A-02
ISSUE M
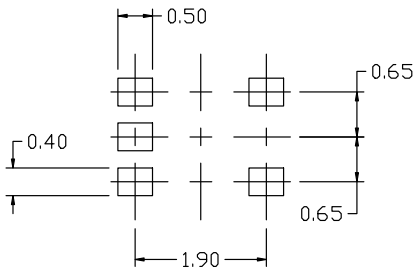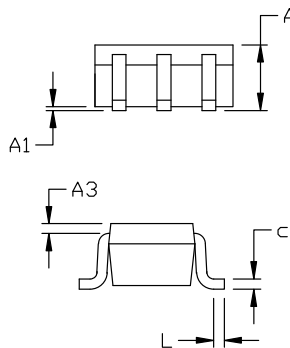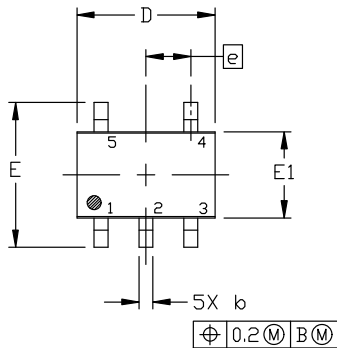
SCALE 2:1

DATE 11 APR 2023

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

2. CONTROLLING DIMENSION: MILLIMETERS

3. 419A-01 OBSOLETE, NEW STANDARD 419A-02

4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.1016MM PER SIDE.

$\boxed{\oplus\ 0.2\ \text{\textcircled{M}}\ B\ \text{\textcircled{M}}}$

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.95	1.10
A1	---	---	0.10
A3	0.20 REF		
b	0.10	0.20	0.30
c	0.10	---	0.25
D	1.80	2.00	2.20
E	2.00	2.10	2.20
E1	1.15	1.25	1.35
e	0.65 BSC		
L	0.10	0.15	0.30
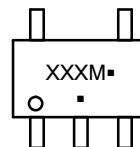
RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**GENERIC MARKING
DIAGRAM***

XXXM■

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

XXX = Specific Device Code
M = Date Code
■ = Pb-Free Package

(Note: Microdot may be in either location)

STYLE 1:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. EMITTER
3. BASE
4. COLLECTOR
5. CATHODE

STYLE 3:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. CATHODE 1

STYLE 4:
PIN 1. SOURCE 1
2. DRAIN 1/2
3. SOURCE 1
4. GATE 1
5. GATE 2

STYLE 5:
PIN 1. CATHODE
2. COMMON ANODE
3. CATHODE 2
4. CATHODE 3
5. CATHODE 4

STYLE 6:
PIN 1. EMITTER 2
2. BASE 2
3. EMITTER 1
4. COLLECTOR
5. COLLECTOR 2/BASE 1

STYLE 7:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 8:
PIN 1. CATHODE
2. COLLECTOR
3. N/C
4. BASE
5. EMITTER

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. ANODE
5. ANODE

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

| DOCUMENT NUMBER:	98ASB42984B	
DESCRIPTION:	SC-88A (SC-70-5/SOT-353)	PAGE 1 OF 1

SOT−23, 5 Lead
CASE 527AH
ISSUE A

DATE 09 JUN 2021

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 19894

2. CONTROLLING DIMENSION: MILLIMETERS

3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.

4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.25 PER SIDE. D AND E1 DIMENSIONS ARE DETERMINED AT DATUM D.

5. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL NOT BE LESS THAN 0.07mm.

TOP VIEW

SIDE VIEW

END VIEW
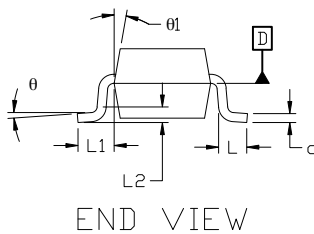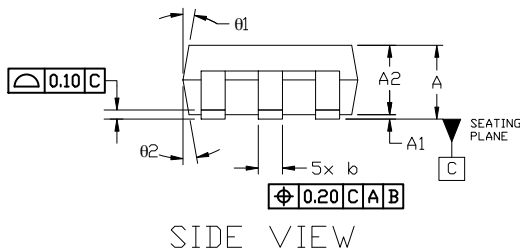
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	—	1.45
A1	0.00	—	0.15
A2	0.90	1.15	1.30
b	0.30	—	0.50
c	0.08	—	0.22
D	2.90 BSC		
E	2.80 BSC		
E1	1.60 BSC		
e	0.95 BSC		
L	0.30	0.45	0.60
L1	0.60 REF		
L2	0.25 REF		
θ	0°	4°	8°
θ1	0°	10°	15°
θ2	0°	10°	15°

GENERIC MARKING DIAGRAM*

XXXM
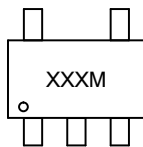
XXX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED MOUNTING FOOTPRINT
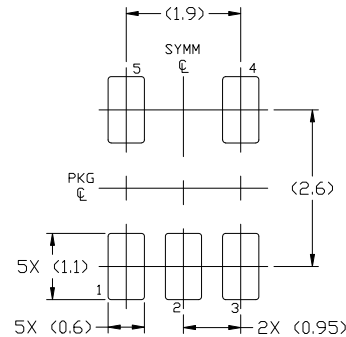
For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	98AON34320E	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	SOT−23, 5 LEAD		PAGE 1 OF 1

ADDITIONAL INFORMATION

◊