# 5+2 CH DC/DC Converters for DV

## General Description

This is a 5+2 CH integrated PMIC for DV application. There are 5 DC/DC converters : one synchronous step-up, one selectable synchronous step-up/step-down, two synchronous step-downs, and one WLED driver in either asynchronous step-up or current source mode, selectable by VOUT6 initial voltage. In addition, there are 2 LDO regulators : one RTC LDO and one generic LDO. The generic LDO can choose internal feedback loop for fixed output 2.5V or external feedback loop for customized output voltage. Both low voltage synchronous step-up converters are with load disconnect function. All power MOSFETs and compensation networks are integrated. There is a power good indicator to monitor FB2, FB3, and FB4 voltage status. CH1 to CH5 enabling can be controlled flexibly : enabled independently or in preset sequences.

## Ordering Information

RT9992□□

- Package Type
  QW : WQFN-32L 4x4 (W-Type)
- Lead Plating System
  Z : ECO (Ecological Element with Halogen Free and Pb free)

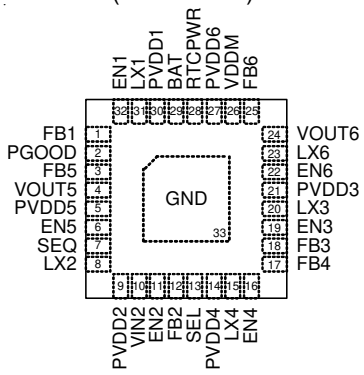
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

## Pin Configuration

(TOP VIEW)




WQFN-32L 4x4

## Features

- **All Power MOSFETs Integrated**
- **5 Channels with Internal Compensation**
- **Flexible Enabling Control**
  - **Enabled Independently or in Preset Power On/Off Sequences**
- **CH2 Synchronous Converter in Step-Up or Step-Down Mode Selectable by SEL Pin**
- **Synchronous Step-Down DC/DC Converter**
  - **Up to 95% Efficiency**
  - **100% (max) Duty Cycle**
- **Synchronous Step-Up DC/DC Converter**
  - **Adjustable Output Voltage**
  - **Up to 95% Efficiency**
- **Asynchronous Step-Up Converter to Drive WLED, Selectable Between Step-Up or Current Source**
  - **LED Open Protection (OVP6) in Step-Up Mode**
  - **PWM Dimming Control**
- **Load Disconnect Function for CH1 and CH2 Synchronous Step-Up Converter**
- **Fixed 2MHz Switching Frequency for CH1, CH2, CH3, and CH4**
- **Fixed 1MHz Switching Frequency for CH6**
- **Generic LDO (CH5)**
  - **Output Voltage : Fixed 2.5V or Set by External Feedback Network, Determined by FB5 Initial Voltage**
- **RTC LDO : Fixed Output Voltage 3.1V**
- **Power Good Indicator to Monitor Output Voltage Status of CH2, CH3, and CH4**
- **32-Lead Package**
- **RoHS Compliant and Halogen Free**

## Applications

- CMOS DV
- Gaming

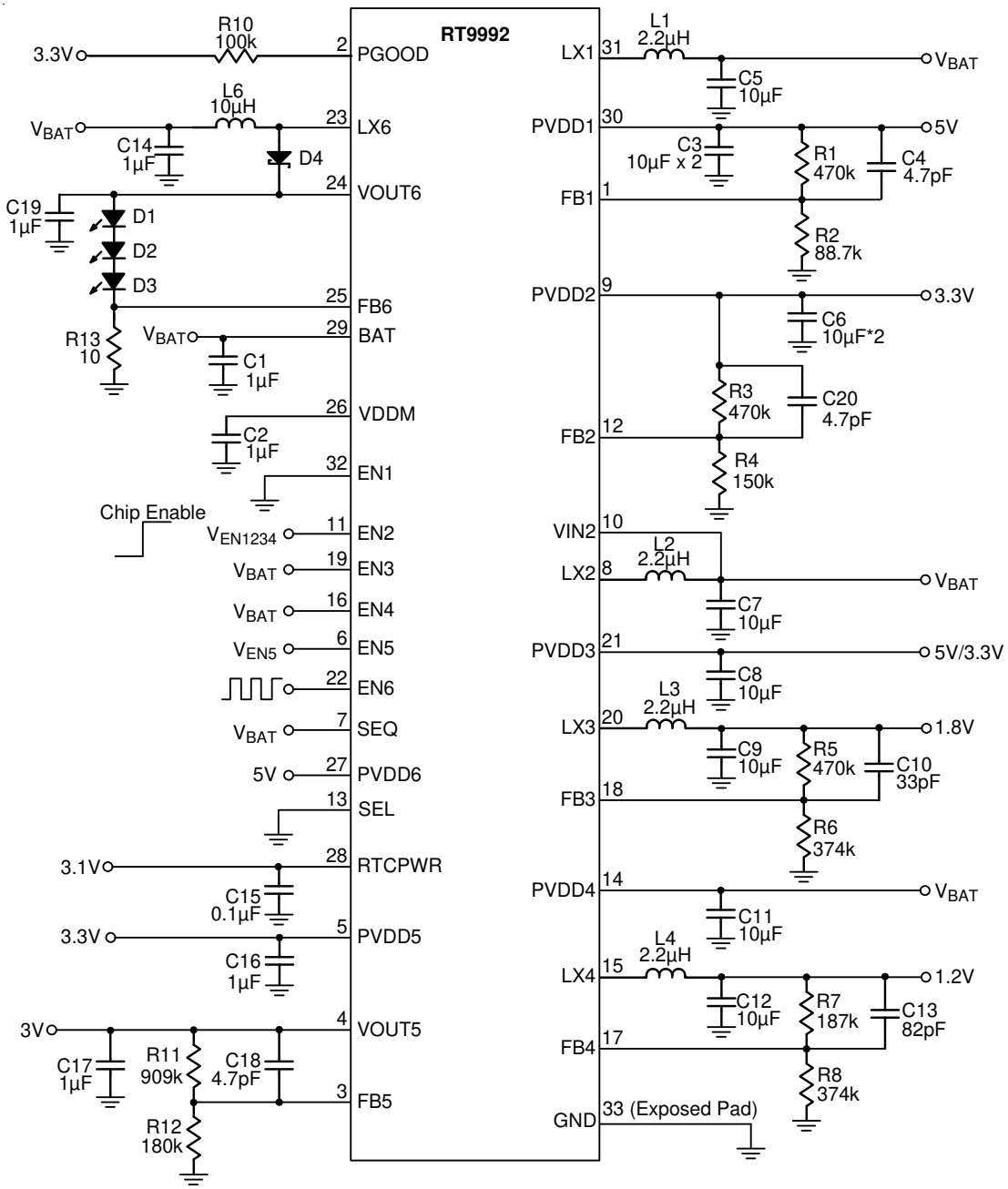
## Marking Information


ES : Product Code

YMDNN : Date Code

## Typical Application Circuit

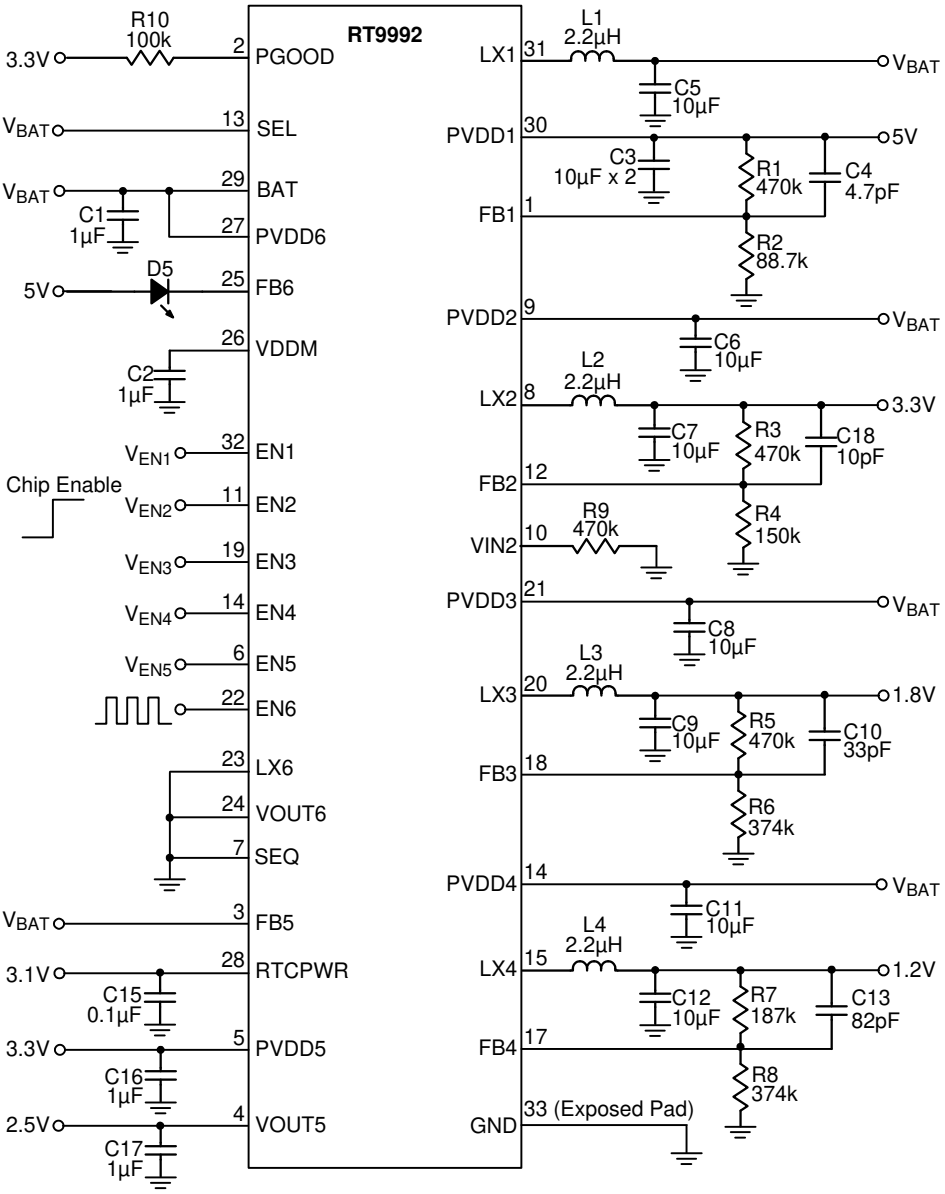
For 2AA :




For above circuit, the power sequence is CH1 → CH3 → CH4 → CH2, while CH5 remains independent.

For other power sequence combinations, refer to the power on/off sequence section in application information.

For Li+ :




For above circuit, all channels are independently enabled/disabled.

For other power sequence combinations, refer to the power on/off sequence section in application information.

**Table 1. Recommended Components for the Typical Application Circuit**

| Channel | CH3 | | | | | |
|---|---|---|---|---|---|---|
| Calculation | $V_{OUT\_CH3}$ = (1 + R5 / R6) x 0.8V | | | | | |
| $V_{OUT}$(V) | 2.5 | 1.8 | 1.5 | 1.3 | 1.2 | 1 |
| L3 (μH) | 2.2 | 2.2 | 2.2 | 2.2 | 2.2 | 2.2 |
| R5 (kΩ) | 768 | 470 | 330 | 237 | 187 | 23.2 |
| R6 (kΩ) | 360 | 374 | 374 | 374 | 374 | 93.1 |
| C9 (μF) | 10 | 10 | 10 | 10 | 10 | 10 |
| C10 (pF) | 22 | 33 | 47 | 68 | 82 | 47 |

| Channel | CH4 | | | | | |
|---|---|---|---|---|---|---|
| Calculation | $V_{OUT\_CH4}$ = (1 + R7 / R8) x 0.8V | | | | | |
| $V_{OUT}$ (V) | 2.5 | 1.8 | 1.5 | 1.3 | 1.2 | 1 |
| L4 (μH) | 2.2 | 2.2 | 2.2 | 2.2 | 2.2 | 2.2 |
| R7 (kΩ) | 768 | 470 | 330 | 237 | 187 | 23.2 |
| R8 (kΩ) | 360 | 374 | 374 | 374 | 374 | 93.1 |
| C12 (μF) | 10 | 10 | 10 | 10 | 10 | 10 |
| C13 (pF) | 22 | 33 | 47 | 68 | 82 | 47 |

Where C9, C12 are $C_{OUT}$,

C10, C13 are feedforward cap between output and FB

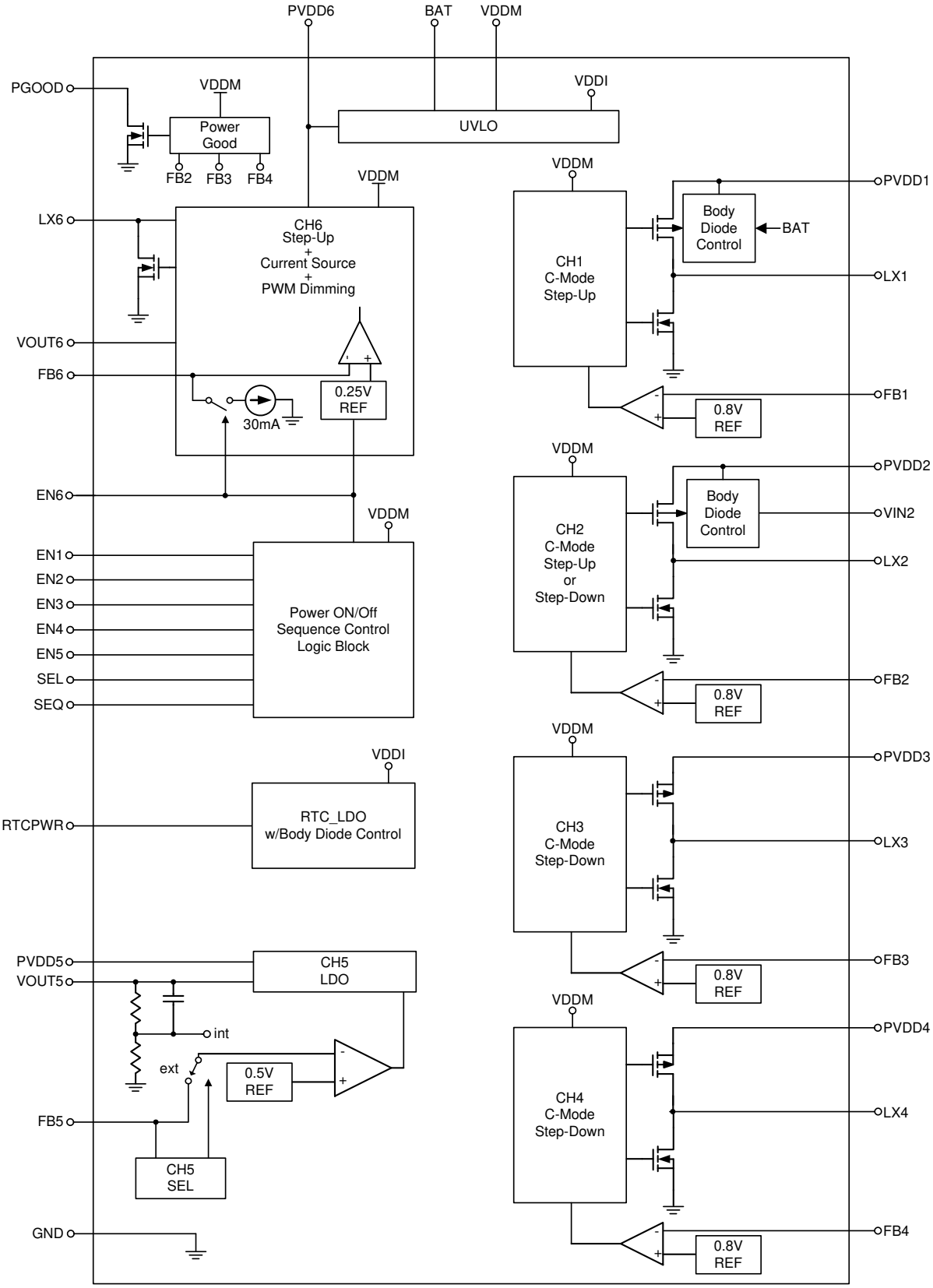
R5, R7 are the feedback resistor between output and FB

R6, R8 are the feedback resistor between GND and FB

## Functional Pin Description

| Pin No. | Pin Name | Pin Function |
|---|---|---|
| 1 | FB1 | Feedback input pin of CH1. High impedance in shutdown. |
| 2 | PGOOD | Power good indicator output pin (Open drain). |
| 3 | FB5 | Feedback input pin of CH5. High impedance in shutdown. |
| 4 | VOUT5 | Output pin for CH5. High impedance in shutdown. |
| 5 | PVDD5 | Power input pin of CH5. |
| 6 | EN5 | Enable pin of CH5. |
| 7 | SEQ | SEQ = H to use preset power on/off sequence. SEQ = L to independently enable CH1 to 5. Logic state can't be changed during operation. |
| 8 | LX2 | Switch node of CH2. High impedance in shutdown. |
| 9 | PVDD2 | Power input pin of CH2 in Step-Down or power output pin of CH2 in step-up. |
| 10 | VIN2 | Power input node of CH2 in step-up. |
| 11 | EN2 | Enable pin of CH2 or enable pin of preset On/Off sequence. |
| 12 | FB2 | Feedback input pin of CH2. High impedance in shutdown. |
| 13 | SEL | Select pin to define CH2 in step-down (SEL = H) or step-up (SEL = L) mode. Logic state can't be changed during operation. |
| 14 | PVDD4 | Power input pin of CH4. |
| 15 | LX4 | Switch node of CH4. High impedance in shutdown. |
| 16 | EN4 | Enable pin of CH4 or Select which preset On/Off sequence. |
| 17 | FB4 | Feedback input pin of CH4. High impedance in shutdown. |
| 18 | FB3 | Feedback input pin of CH3. High impedance in shutdown. |
| 19 | EN3 | Enable pin of CH3 or select which preset On/Off sequence. |
| 20 | LX3 | Switch node of CH3. High impedance in shutdown. |
| 21 | PVDD3 | Power input pin of CH3. |
| 22 | EN6 | Enable pin of CH6 and PWM dimming input signal pin. |
| 23 | LX6 | Switch node of CH6 in step-up mode. High impedance in shutdown. |
| 24 | VOUT6 | Sense pin for CH6 output voltage in step-up mode and CH6 mode selection pin. |
| 25 | FB6 | Feedback input pin of CH6 in step-up mode or current sink pin of CH6 in current source mode. |
| 26 | VDDM | Internal control circuit power pin. That must connect to a bypass capacitor for better noise rejection. |
| 27 | PVDD6 | Power input pin of CH6 N-MOSFET Driver. |
| 28 | RTCPWR | RTC power output pin. |
| 29 | BAT | Battery power input pin and CH1 step-up power input node. |
| 30 | PVDD1 | Power output pin of CH1. |
| 31 | LX1 | Switch node of CH1. High impedance in shutdown. |
| 32 | EN1 | Enable pin of CH1. |
| 33 (Exposed pad) | GND | Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation. |

## Functional Block Diagram



## Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VDDM ---------- –0.3V to 7V
- LX1, LX2, LX3, LX4 ---------- –0.3V to 7V
  < 20ns ---------- –0.3V to 10V
- LX6, VOUT6 ---------- –0.3V to 21V
  < 20ns ---------- –8V to 24V
- Other Pins ---------- –0.3V to 7V
- Power Dissipation, $P_D$ @ $T_A$ = 25°C
  WQFN–32L 4x4 ---------- 3.59W
- Package Thermal Resistance (Note 2)
  WQFN–32L 4x4, $\theta_{JA}$ ---------- 27.8°C/W
  WQFN–32L 4x4, $\theta_{JC}$ ---------- 7°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Mode) ---------- 2kV

## Recommended Operating Conditions (Note 4)

- Supply Input Voltage VDDM ---------- 2.7V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

## Electrical Characteristics

($V_{DDM}$ = 3.3V, $T_A$ = 25°C, unless otherwise specified)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Supply Voltage** | | | | | | |
| VDDM Startup Voltage | $V_{ST}$ | For Bootstrap, First Rising | 1.5 | -- | -- | V |
| **Supply Current** | | | | | | |
| Shutdown Supply Current into BAT (including RTC LDO quiescent current) | | $V_{BAT}$ = 4.2V, $V_{PVDD6}$ = 3V | -- | 7 | 12 | μA |
| Shutdown Supply Current into PVDD6 | | $V_{BAT}$ = 4.2V, $V_{PVDD6}$ < $V_{BAT}$ | -- | -- | 1 | μA |
| Shutdown Supply Current into VDDM | $I_{OFF}$ | ENx = 0, $V_{SEQ}$ = 0V, SEL = 0V | -- | 1 | 10 | μA |
| CH1 (Synchronous Step-Up) Supply Current into VDDM | $I_{Q1}$ | Non Switching, $V_{EN1}$ = 3.3V, $V_{FB1}$ = 0.9V, $V_{SEQ}$ = 0V | -- | -- | 800 | μA |
| CH2 (Synchronous Step-Up or Step-Down) Supply Current into VDDM | $I_{Q2}$ | Non Switching, $V_{EN2}$ = 3.3V, $V_{FB2}$ = 0.9V, $V_{SEQ}$ = 0V | -- | -- | 800 | μA |
| CH3 (Synchronous Step-Down) Supply Current into VDDM | $I_{Q3}$ | Non Switching, $V_{EN3}$ = 3.3V, $V_{FB3}$ = 0.9V, $V_{SEQ}$ = 0V | -- | -- | 800 | μA |

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| CH4 (Synchronous Step-Down) Supply Current into VDDM | $I_{Q4}$ | Non Switching, $V_{EN4}$ = 3.3V, $V_{FB4}$ = 0.9V, $V_{SEQ}$ = 0V | -- | -- | 800 | μA |
| CH6 (WLED) in Current Source Mode Supply Current into VDDM | $I_{Q6c}$ | $V_{EN6}$ = 3.3V, $V_{OUT6}$ = 0V | -- | -- | 600 | μA |
| CH6 (WLED) in Asynchronous Step-Up Mode Supply Current into VDDM | $I_{Q6b}$ | Non switching, $V_{EN6}$ = 3.3V, $V_{FB6}$ = 0.35V, VOUT6 = 1V | -- | -- | 800 | μA |
| **Oscillator** | | | | | | |
| CH1, 2, 3, 4 Operation Frequency | $f_{OSC}$ | | 1800 | 2000 | 2200 | kHz |
| CH6 Operation Frequency | $f_{OSC6}$ | | 900 | 1000 | 1100 | kHz |
| CH1 Maximum Duty Cycle (Step-Up) | | $V_{FB1}$ = 0.7V | 80 | 83.5 | 87 | % |
| CH2 Maximum Duty Cycle (Step-Up) | | $V_{FB2}$ = 0.7V | 80 | 83.5 | 87 | % |
| CH2 Maximum Duty Cycle (Step-Down) | | $V_{FB2}$ = 0.7V | -- | -- | 100 | % |
| CH3 Maximum Duty Cycle (Step-Down) | | $V_{FB3}$ = 0.7V | -- | -- | 100 | % |
| CH4 Maximum Duty Cycle (Step-Down) | | $V_{FB4}$ = 0.7V | -- | -- | 100 | % |
| CH6 Maximum Duty Cycle (Step-Up) | | $V_{FB6}$ = 0.15V, $V_{OUT6}$ = 1V | 91 | 93 | 97 | % |
| **Feedback and output Regulation Voltage** | | | | | | |
| Feedback Regulation Voltage @ FB1, FB2, FB3, and FB4 | | | 0.788 | 0.8 | 0.812 | V |
| Sink Current into FB6 (CS mode) | | $V_{OUT6}$ = 0V, Current Source | 28.5 | 30 | 31.5 | mA |
| Dropout Voltage @ FB6 (CS mode) | | $V_{OUT6}$ = 0V, $V_{DDM}$ = 3.3V, Current Source | -- | -- | 0.6 | V |
| Feedback Regulation Voltage @ FB6 | $V_{FB6}$ | $V_{OUT6}$ = 1V. Step-Up | 0.237 | 0.25 | 0.263 | V |
| **Power Switch** | | | | | | |
| CH1 On Resistance of MOSFET | $R_{DS(ON)}$ | P-MOSFET, $V_{PVDD1}$ = 3.3V | -- | 200 | 300 | mΩ |
| | | N-MOSFET, $V_{PVDD1}$ = 3.3V | -- | 130 | 250 | |
| CH1 Current Limitation (Step-Up) | $I_{LIM1}$ | | 2.2 | 3 | 4 | A |
| CH2 On Resistance of MOSFET | $R_{DS(ON)}$ | P-MOSFET, $V_{PVDD2}$ = 3.3V | -- | 400 | 550 | mΩ |
| | | N-MOSFET, $V_{PVDD2}$ = 3.3V | -- | 260 | 400 | |
| CH2 Current Limitation (Step-Down) | $I_{LIM2\_D}$ | | 1 | 1.5 | 2 | A |
| CH2 Current Limitation (Step-Up) | $I_{LIM2\_U}$ | | 1.5 | 2.1 | 3 | A |
| CH3 On Resistance of MOSFET | $R_{DS(ON)}$ | P-MOSFET, $V_{PVDD3}$ = 3.3V | -- | 370 | 500 | mΩ |
| | | N-MOSFET, $V_{PVDD3}$ = 3.3V | -- | 300 | 400 | |
| CH3 Current Limitation (Step-Down) | $I_{LIM3}$ | | 1 | 1.5 | 2 | A |
| CH4 On Resistance of MOSFET | $R_{DS(ON)}$ | P-MOSFET, $V_{PVDD4}$ = 3.3V | -- | 240 | 400 | mΩ |
| | | N-MOSFET, $V_{PVDD4}$ = 3.3V | -- | 140 | 250 | |
| CH4 Current Limitation (Step-Down) | $I_{LIM4}$ | | 1.5 | 2 | 2.4 | A |
| CH6 On Resistance of MOSFET | $R_{DS(ON)}$ | N-MOSFET | -- | 0.75 | 1.1 | Ω |
| CH6 Current Limitation | $I_{LIM6}$ | N-MOSFET | 0.6 | 0.8 | 1 | A |

| Parameter | | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Protection** | | | | | | | |
| Over Voltage Protection PVDD1,PVDD2 (CH2 in Step-Up) | | | | 5.9 | 6.15 | 6.4 | V |
| Over Voltage Protection @ VOUT6 | | $V_{OVP6}$ | Step-Up | 18 | 19.5 | 21 | V |
| Under Voltage Protection @ FB1, FB2, FB3, FB4 | | $V_{UVP1234}$ | | -- | 0.4 | -- | V |
| Under Voltage Protection @ FB5 | | $V_{UVP5}$ | | -- | 0.3 | -- | V |
| VDDM Over Voltage Protection | | | | 5.9 | 6.15 | 6.4 | V |
| VDDM UVLO Threshold | | | VDDM Rising | | 2.4 | 2.7 | V |
| | | | VDDM Falling | 1.7 | 2.1 | 2.4 | |
| BAT UVLO Threshold | | | BAT Rising | 1.3 | 1.4 | 1.5 | V |
| | | | BAT Falling | 1.2 | 1.3 | 1.4 | |
| Protection Fault Delay | | | Except OVP1/2 | -- | 100 | -- | ms |
| **Control** | | | | | | | |
| EN1 to 6, SEL, SEQ Threshold Voltage | Logic-High | $V_{IH}$ | | 1.3 | -- | -- | V |
| | Logic-Low | $V_{IL}$ | | -- | -- | 0.4 | |
| EN1 to 5, SEL, SEQ Sink Current | | | | -- | 1 | 6 | μA |
| EN6 Sink Current | | | | -- | 4 | 20 | μA |
| EN6 Low Time for Shutdown | | $t_{SHDN}$ | | -- | 32.7 | -- | ms |
| EN6 High Time for CH6 Enable | | | | -- | 1.2 | 5 | μs |
| **Thermal Protection** | | | | | | | |
| Thermal Shutdown | | $T_{SD}$ | | 125 | 160 | -- | °C |
| Thermal Shutdown Hysteresis | | $\Delta T_{SD}$ | | -- | 20 | -- | °C |
| **CH5 LDO ($C_{OUT}$ = 1μF for Better Stability)** | | | | | | | |
| Input Voltage Range (PVDD5) | | $V_{PVDD5}$ | | 2.7 | -- | 5.5 | V |
| Output Voltage Range | | $V_{OUT5}$ | By external feedback | 0.6 | -- | 4.5 | V |
| Feedback Regulation Voltage @ FB5 | | $V_{FB5}$ | Using external feedback loop | 0.493 | 0.5 | 0.507 | V |
| Regulated Output Voltage @ VOUT5 | | $V_{REG5}$ | Using internal feedback loop | 2.45 | 2.5 | 2.55 | V |
| FB5 Threshold to Select Internal Feedback Network | | | (Note : before enabled, $V_{FB5}$ > 0.8V. Then CH5 uses internal feedback) | 0.8 | -- | -- | V |
| Max Current Limit | | $I_{LIM5}$ | $V_{PVDD5}$ = 3.3V | 300 | 380 | 500 | mA |
| Dropout Voltage | | | $I_{OUT}$ = 100mA | 60 | 100 | 120 | mV |
| Soft-Start Time | | $t_{SS5}$ | $V_{FB5}$ = 0 to 0.5V | -- | 2.4 | -- | ms |
| PSRR+ | | | $I_{OUT}$ = 10mA, $V_{PVDD5}$ = 3.3V, $V_{OUT}$ = 2.5V, 1kHz | -- | –55 | -- | db |

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **RTC LDO for RTCPWR (Keep On Once Bat Connect)** | | | | | | |
| Input Voltage Range | $V_{DDI}$ | Max of BAT and PVDD6 | -- | -- | 5.5 | V |
| Quiescent Current | $I_Q$ | $V_{DDI}$ = 4.2V | -- | 5 | 8 | μA |
| Regulated Output Voltage @ RTCPWR | | $I_{OUT}$ = 0mA | 3.0 | 3.1 | 3.2 | V |
| Max Output Current (Current Limit) | | $V_{DDI}$ = 4.2V | 60 | 105 | 200 | mA |
| Dropout Voltage | $V_{DROP}$ | $I_{OUT}$ = 50mA | -- | 740 | 1000 | mV |
| | | $I_{OUT}$ = 10mA | -- | 110 | 200 | |
| | | $I_{OUT}$ = 3mA | -- | 60 | 100 | |
| **Power Good Indicator** | | | | | | |
| FB2 Regulation Threshold | | For PGOOD Go Low | 0.6 | 0.66 | 0.74 | V |
| FB2 Hysteresis | | | -- | 40 | -- | mV |
| FB3 Regulation Threshold | | For PGOOD Go Low | 0.6 | 0.66 | 0.74 | V |
| FB3 Hysteresis | | | -- | 40 | -- | mV |
| FB4 Regulation Threshold | | For PGOOD Go Low | 0.6 | 0.66 | 0.74 | V |
| FB4 Hysteresis | | | -- | 40 | -- | mV |
| PGOOD Rising Delay Time | | | 13 | 14.4 | 15.9 | ms |
| PGOOD Sink Capability | | $V_{DDM}$ = 3.3V, $V_{PGOOD}$ = 0.5V | 4 | -- | -- | mA |
| **Soft-Start Time** | | | | | | |
| CH1 Soft-Start Time | $t_{SS1}$ | $V_{FB1}$ = 0 to 0.8V | 2.8 | 3.5 | 4.2 | ms |
| CH2 Soft-Start Time | $t_{SS2}$ | $V_{FB2}$ = 0 to 0.8V | 2.8 | 3.5 | 4.2 | ms |
| CH3 Soft-Start Time | $t_{SS3}$ | $V_{FB3}$ = 0 to 0.8V | 2.8 | 3.5 | 4.2 | ms |
| CH4 Soft-Start Time | $t_{SS4}$ | $V_{FB4}$ = 0 to 0.8V | 2.8 | 3.5 | 4.2 | ms |

**Note 1.** Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

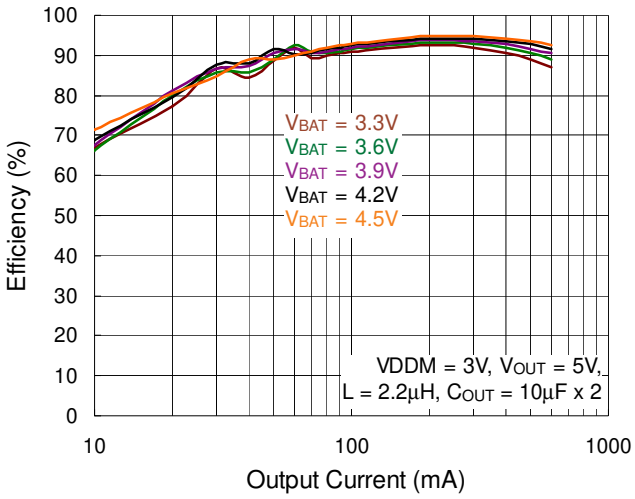
**Note 2.** $\theta_{JA}$ is measured at $T_A$ = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. $\theta_{JC}$ is measured at the exposed pad of the package.

**Note 3.** Devices are ESD sensitive. Handling precaution is recommended.

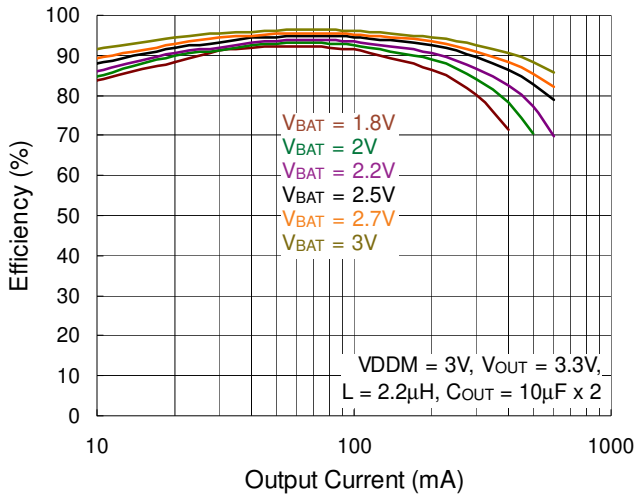
**Note 4.** The device is not guaranteed to function outside its operating conditions.

## Typical Operating Characteristics

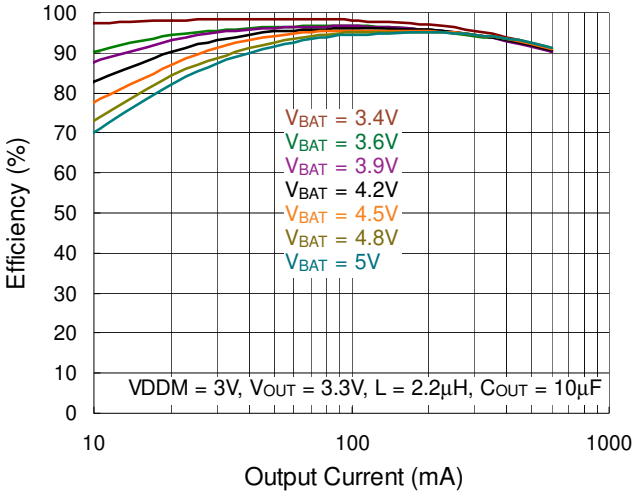
### CH1 Step-Up Efficiency vs. Output Current



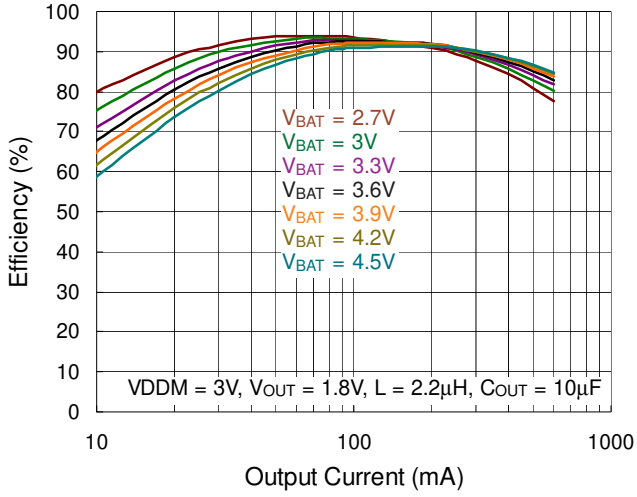

### CH2 Step-Up Efficiency vs. Output Current



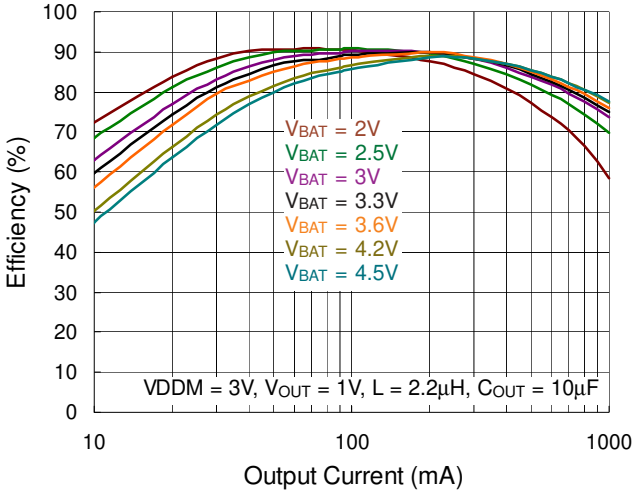

### CH2 Step-Down Efficiency vs. Output Current



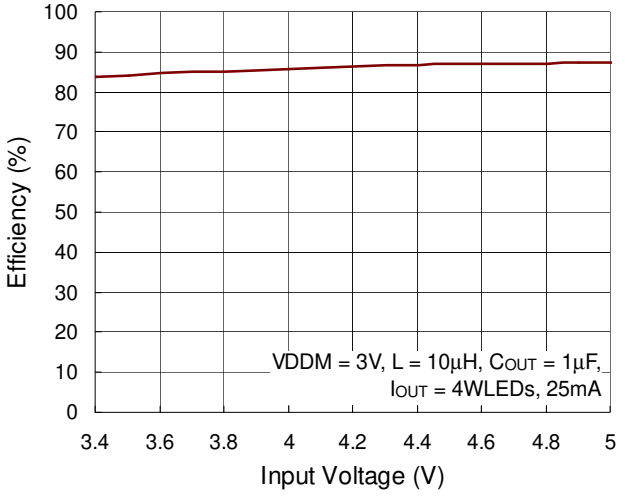

### CH3 Step-Down Efficiency vs. Output Current



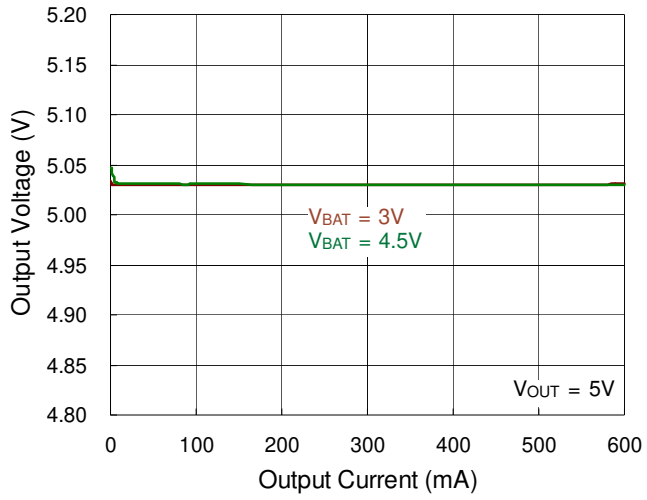

### CH4 Step-Down Efficiency vs. Output Current



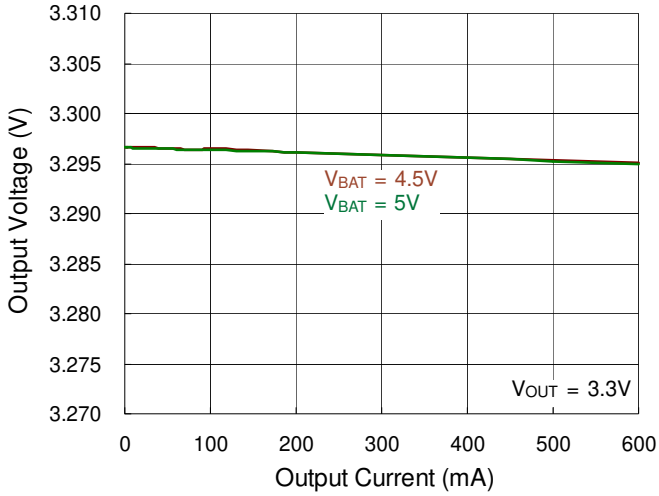

### CH6 Efficiency vs. Input Voltage



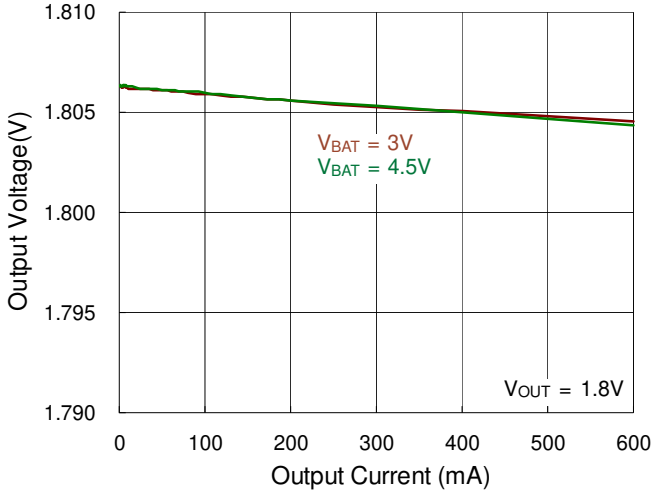
### CH1 Step-Up Output Voltage vs. Output Current



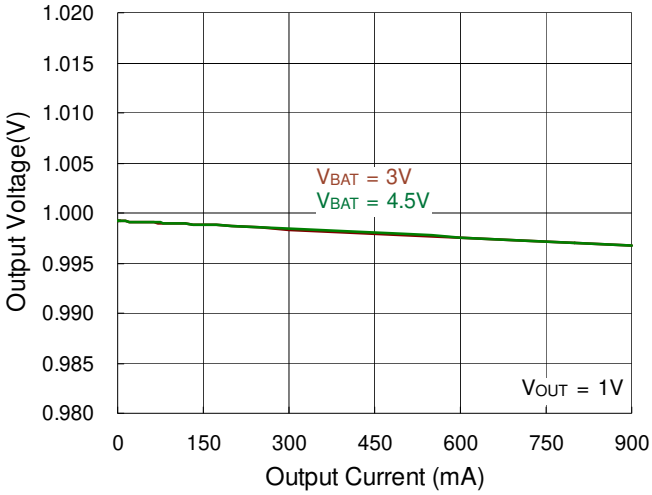

### CH2 Step-Dwon Output Voltage vs. Output Current



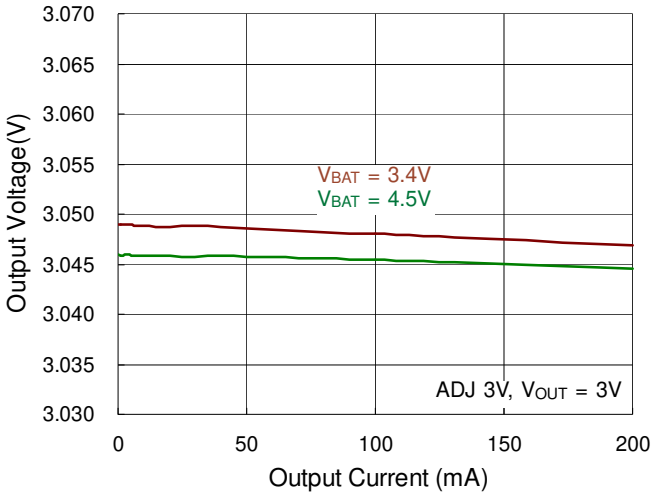

### CH3 Step-Down Output Voltage vs. Output Current



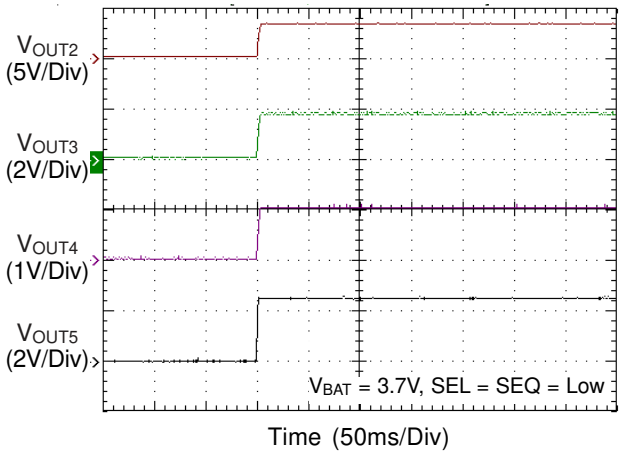

### CH4 Step-Down Output Voltage vs. Output Current



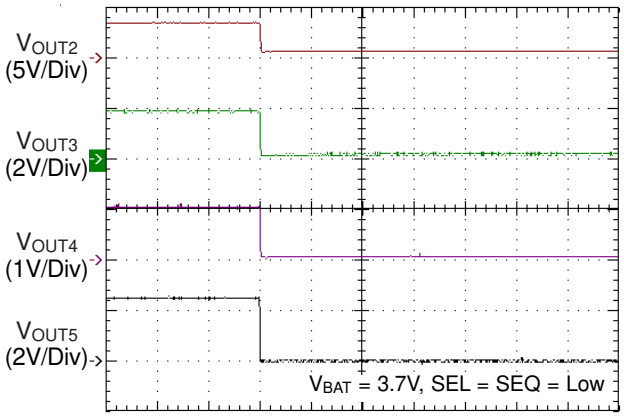

### CH5 LDO Output Voltage vs. Output Current



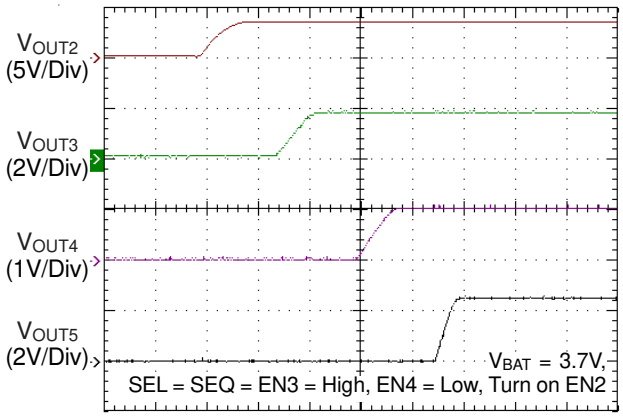

### Power On Sequence Independently



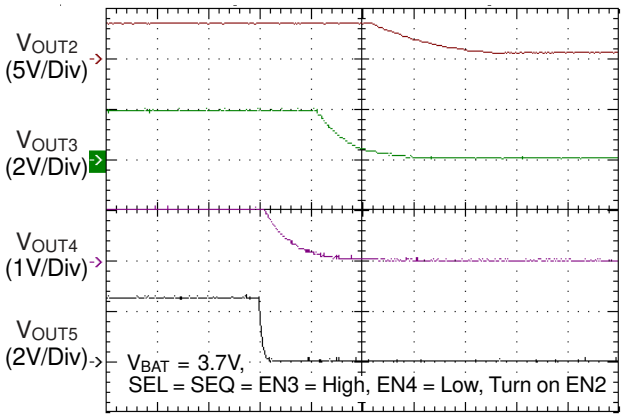
### Power Off Sequence Independently




### Power On Sequence 1




### Power Off Sequence 1

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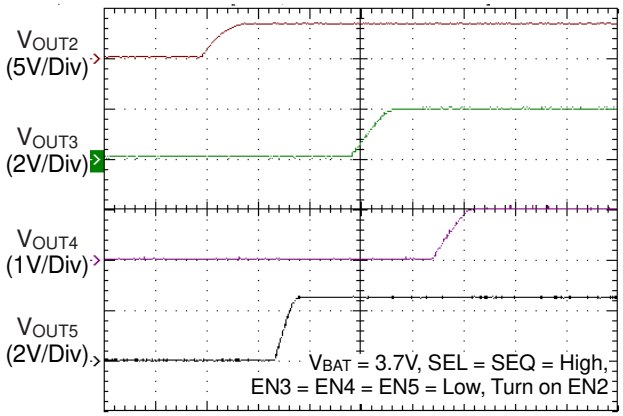
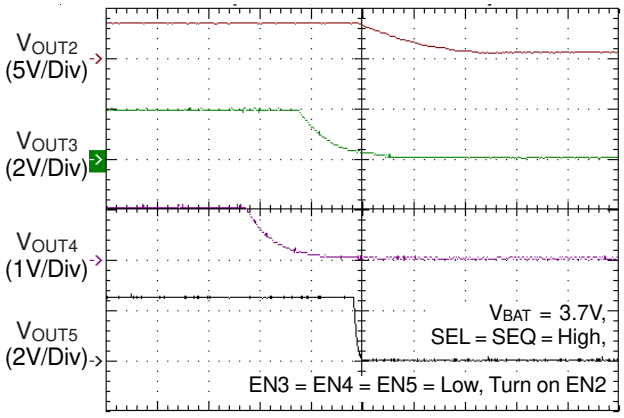
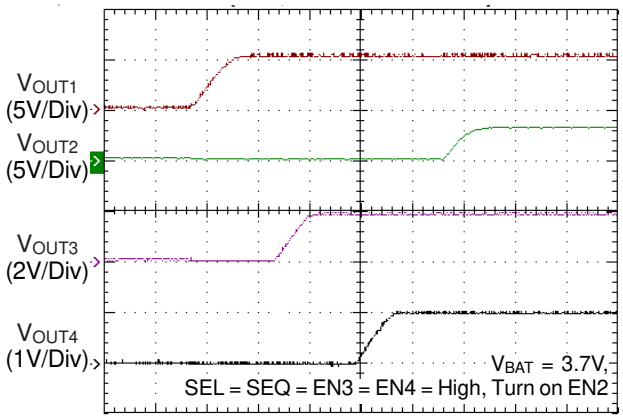


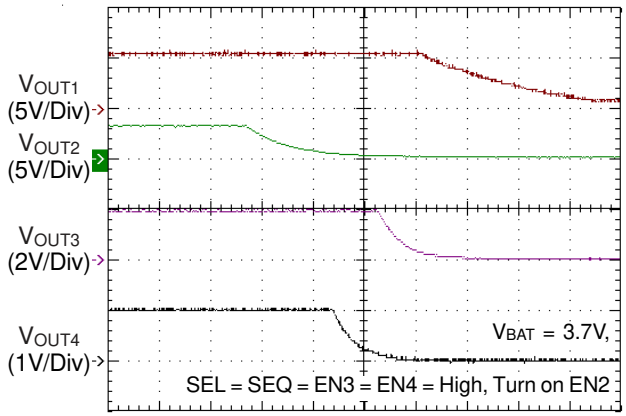

### Power Off Sequence 2



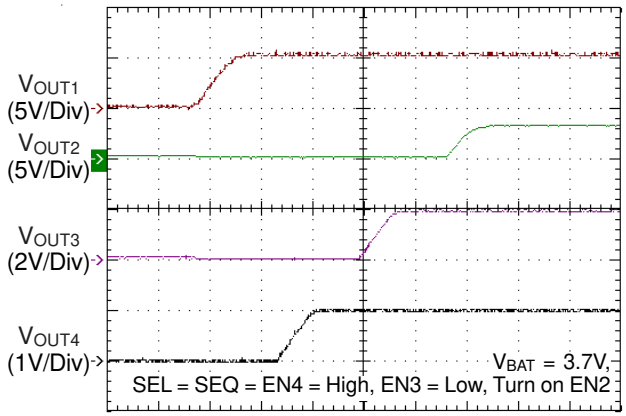

### Power On Sequence 3



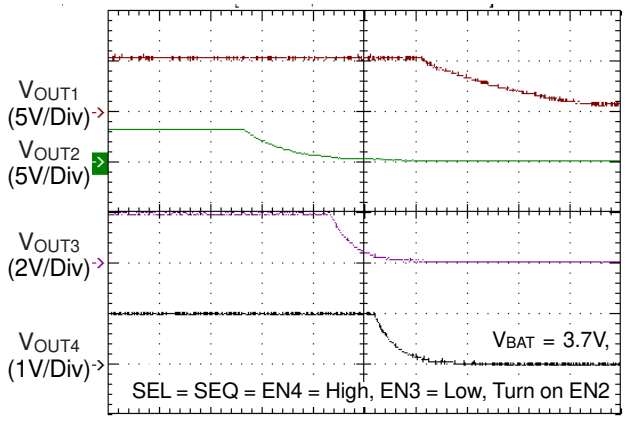
### Power Off Sequence 3



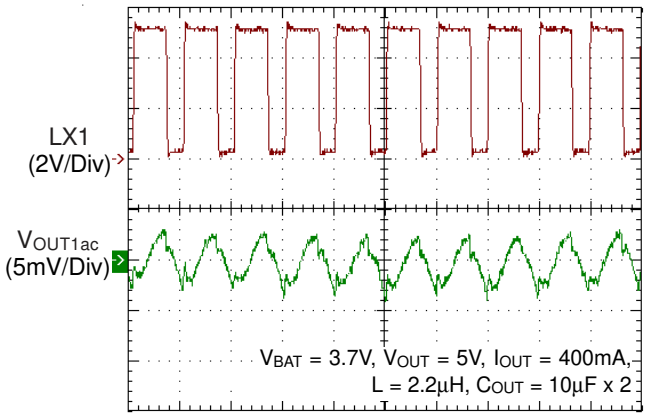

### Power On Sequence 4



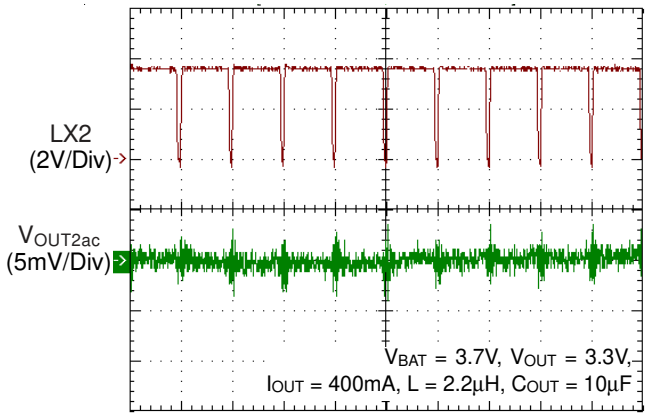

### Power Off Sequence 4



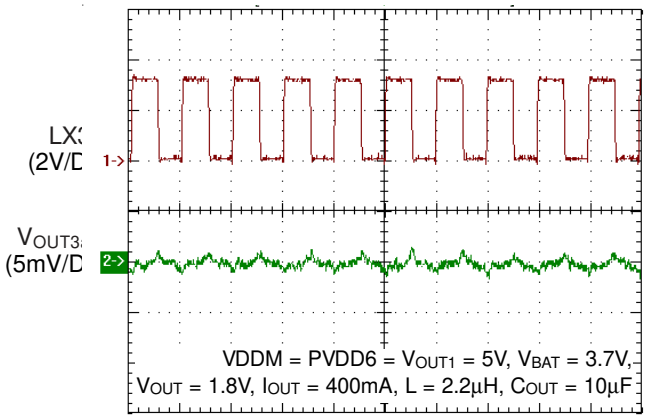

### CH1 Output Voltage Ripple



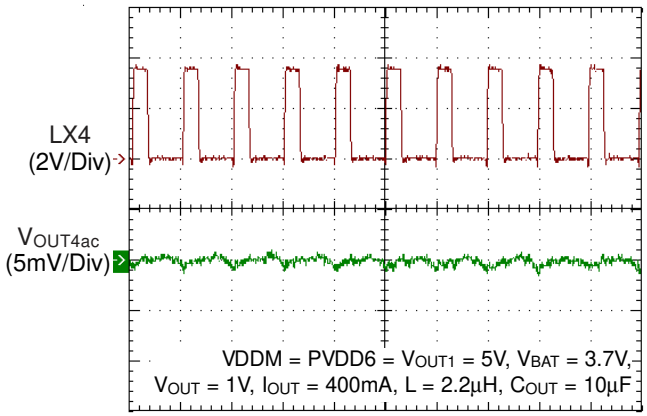

### CH2 Output Voltage Ripple



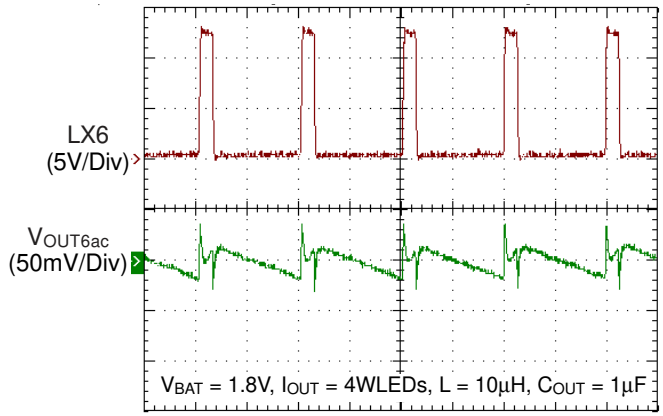

### CH3 Output Voltage Ripple



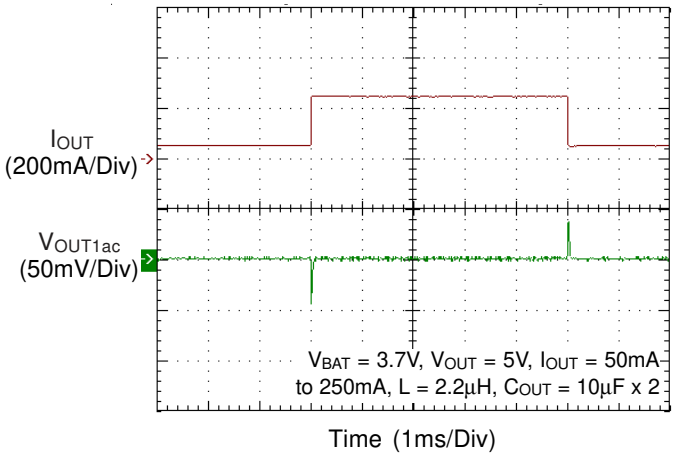
### CH4 Output Voltage Ripple



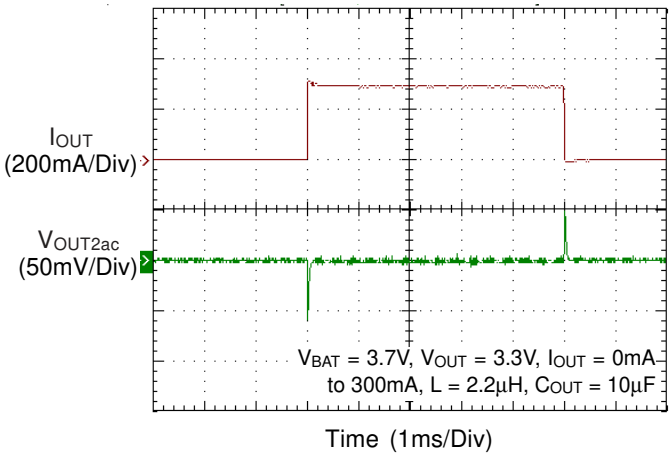

### CH6 Output Voltage Ripple



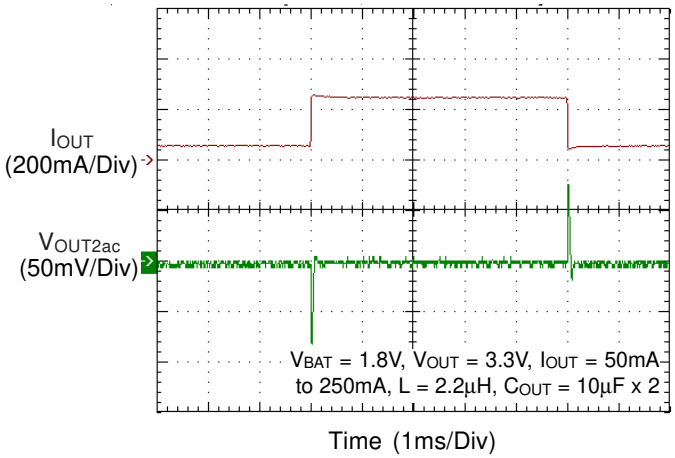

### CH1 Load Transient Response



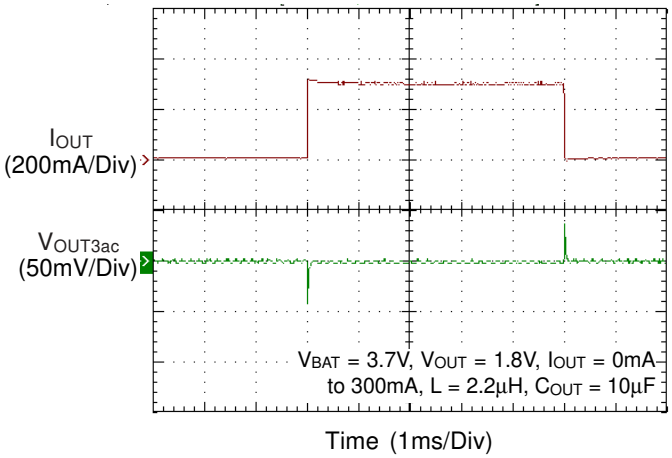

### CH2 Load Transient Response



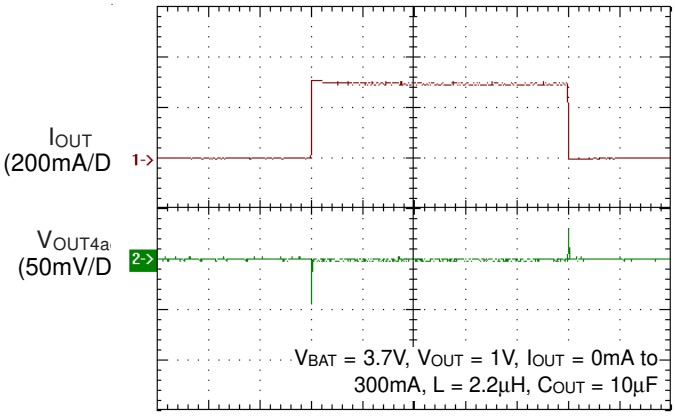

### CH2 Load Transient Response




### CH3 Load Transient Response

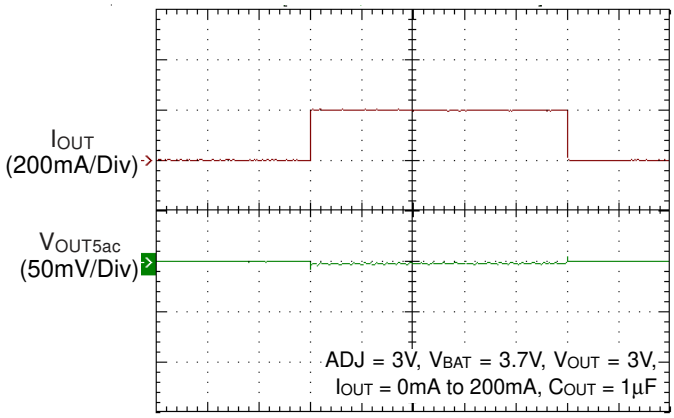


**CH4 Load Transient Response**




Time (1ms/Div)

**CH5 Load Transient Response**




Time (1ms/Div)

## Application Information

The RT9992 includes the following four DC/DC converter channels, two LDOs, and one WLED driver to build a multiple-output power-supply system.

CH1 : Step-up synchronous current mode DC/DC converter with internal power MOSFETs and compensation network. The P-MOSFET body can be controlled to disconnect the load.

CH2 : Selectable step-up or step-down synchronous current mode DC/DC converter with internal power MOSFETs and compensation network. The P-MOSFET body can be controlled to disconnect the load.

CH3 : Step-down synchronous current mode DC/DC converter with internal power MOSFETs and internal compensation network.

CH4 : Step-down synchronous current mode DC/DC converter with internal power MOSFETs and internal compensation network.

CH5 : Generic LDO that provides either fixed 2.5V output or adjustable output voltage via external feedback network, depending on initial by FB5 voltage prior to becoming enabled.

CH6 : WLED driver operable in either current source mode or asynchronous step-up mode with internal power MOSFET and compensation network.

CH1 to CH4 operate in PWM mode with 2MHz, while CH6 operates in step-up mode with 1MHz switching frequency under moderate to heavy loading.

RTC_LDO : 3.1V output LDO with low quiescent current and high output voltage accuracy.

Power Good Indicator : Monitors FB2, FB3, and FB4 status.

### CH1 : Synchronous Step-Up DC/DC Converter

CH1 is a synchronous step-up converter for motor driver power in DSC system. The converter operates at fixed frequency and under PWM Current Mode. The converter integrates internal MOSFETs, compensation network and synchronous rectifier for up to 95% efficiency. It also disconnects the load when CH1 is turned off. Connect BAT to the power input node in front of CH1 inductor.

The output voltage can be set by the following equation :

$V_{OUT\_CH1}$ = (1+R1/R2) x $V_{FB1}$

where $V_{FB1}$ is 0.8V typically.

### CH2 : Synchronous Step-Up / Step-Down Selectable DC/DC Converter

CH2 is a synchronous step-up / step-down selectable converter for system I/O power.

### Mode Setting

CH2 of the RT9992 features flexible step-up/step-down topology setting for 2AA / Li-ion battery. If CH2 operates in step-up mode, the SEL pin should be connected to GND. If CH2 operates in step-down mode, the SEL pin should be connected to $V_{BAT}$. In addition, please note that the logic state can not be changed during operation.

**Table 2. CH2 Mode Setting**

| CH2 Operating Mode | Connection |
|---|---|
| **Step-Up** | Connect the SEL pin to GND. |
| **Step-Down** | Connect the SEL pin to $V_{BAT}$. |

### Step-Up

The converter operates in fixed frequency PWM Mode, Continuous Current Mode (CCM), and Discontinuous Current Mode (DCM) with internal MOSFETs, compensation network and synchronous rectifier for up to 95% efficiency. In step-up mode, CH2 also disconnects the load when it is turned off. Connect VIN2 to the power input node in front of CH2 inductor.

### Step-Down

The converter operates in fixed frequency PWM mode and Continuous Current Mode (CCM) with internal MOSFETs, compensation network and synchronous rectifier for up to 95% efficiency. The CH2 step-down converter can be operated at 100% maximum duty cycle to extend the input operating voltage range. When the input voltage is close to the output voltage, the converter enters low dropout mode. In step-down mode, connect the VIN2 pin to GND via a 470kΩ pull-down resistor.

The output voltage can be set by the following equation :

$V_{OUT\_CH2} = (1+R3/R4) \times V_{FB2}$

where $V_{FB2}$ is 0.8V typically

### CH3 : Synchronous Step-Down DC/DC Converter

CH3 is suitable for DRAM power in DSC system. The converter operates in fixed frequency PWM mode and CCM with integrated internal MOSFETs and compensation network. The CH3 step-down converter can be operated at 100% maximum duty cycle to extend battery operating voltage range. When the input voltage is close to the output voltage, the converter enters low dropout mode with low output ripple.

The output voltage can be set by the following equation :

$V_{OUT\_CH3} = (1 + R5 / R6) \times V_{FB3}$

where $V_{FB3}$ is 0.8V typically.

### CH4 : Synchronous Step-Down DC/DC Converter

CH4 is suitable for processor core power in DSC system. The converter operates in fixed frequency PWM mode and CCM with integrated internal MOSFETs and compensation network. The CH4 step-down converter can be operated at 100% maximum duty cycle to extend battery operating voltage range. When the input voltage is close to the output voltage, the converter enters low dropout mode with low output ripple.

The output voltage can be set by the following equation :

$V_{OUT\_CH4} = (1+R7/R8) \times V_{FB4}$

Where $V_{FB4}$ is 0.8V typically.

### CH5 : Generic LDO

The RT9992 provides a generic LDO with high output voltage accuracy. The LDO outputs either a fixed 2.5V voltage or an adjustable voltage with external feedback network, depending on the initial FB5 voltage. The CH5 adjustable output voltage can be set by the following equation :

$V_{OUT\_CH5} = (1+R11/R12) \times V_{FB5}$

Where $V_{FB5}$ is 0.5V typically.

### CH6: WLED Driver

CH6 is a WLED driver that can operate in either current source mode or asynchronous step-up mode, depending on the initial VOUT6 voltage level. In addition, if CH4 soft-start does not finish, CH6 can not be turned on.

**Table 3. CH6 WLED Setting**

| CH6 Operating Mode | VOUT6 |
|---|---|
| Current Source | <0.3V |
| Asynchronous Step-Up | >0.7V |

When CH6 works in current source mode, it sinks an accurate LED current modulated by EN6 high duty such that it is easily dimmed from 0mA to 30mA. If CH6 works in asynchronous step-up mode, it integrates asynchronous step-up mode with an internal MOSFET and internal compensation, and requires an external schottky diode to output a voltage up to 19V. The LED current is set via an external resistor and controlled via the PWM duty on the EN6 pin. Regardless of the mode, holding EN6 low for more than 32.7ms will turn off CH6.

### CH6 WLED Current Dimming Control

If CH6 is in asynchronous step-up mode, the WLED current is set by an external resistor. And the dimming is controlled by the duty of pulse width modulated signal on the EN6 pin.

The average current through WLED can be set by the following equations :

$I_{LED}$ (mA) = [250mV/R(Ω)] x Duty (%) .....for step-up mode

Or $I_{LED}$ (mA) = 30mA x Duty (%)..... for current source mode

R : Current sense resistor from FB6 to GND.

Duty : PWM dimming via the EN6 pin. Dimming frequency range is from 1kHz to 100kHz but 2kHz to 20kHz should be avoided to prevent audio noise distraction.

### VDDM Power Path

To support bootstrap function, the RT9992 includes a power selection circuit which selects between BAT and PVDD6 for the higher voltage to be used as the internal node, VDDI, that connects to the external decoupling capacitor at the VDDM pin. VDDM is the main power for the RT9992 control circuit. VDDI is the power input for the RTC LDO. To bootstrap VDDM, PVDD6 must connect to the output of the first enabled low voltage synchronous step-up channel (CH1 or CH2). Furthermore, PVDD6 also

provides power to the N-MOSFET driver in CH6. The RT9992 includes UVLO circuits to check VDDM and BAT voltage status.

### RTC LDO

The RT9992 provides a 3.1V output LDO for real time clock. The LDO features low quiescent current (5μA) and high output voltage accuracy. The RTC LDO is always on, even when the system is shut down. For better stability, it is recommended to connect a 0.1μF capacitor to the RTCPWR pin. The RTC LDO includes pass transistor body diode control to avoid the RTCPWR node from back charging into the input node VDDI.

### Power Good

The RT9992 provides a power good indicator to monitor FB2, FB3, and FB4 voltage status. After CH2, CH3, and CH4 are turned on, if any one of them becomes lower than 0.66V (typically), PGOOD will be pulled low. If all are higher than 0.7V (typically), PGOOD will be released and pulled high after 10ms.

### Power On/Off Sequence

SEQ = 0 : CH1 to 5 are independently enabled by EN1 to EN5

SEQ = 1 : CH2 to 5, or CH1 to 4 is enabled in preset on/off sequence. The order is chosen by EN3 and EN4

| SEQ | EN2 | EN3 | EN4 | EN5 | EN1 | Power On Sequence | | | |
|---|---|---|---|---|---|---|---|---|---|
| 0 | indept | indept | indept | indept | indept | independent | | | |
| 1 | EN2345 | 1 | 0 | X | indept | CH2 | CH3 | CH4 | CH5 |
| 1 | EN2345 | 0 | 0 | 0 | indept | CH2 | CH5 | CH3 | CH4 |
| 1 | EN1234 | 1 | 1 | indept | x | CH1 | CH3 | CH4 | CH2 |
| 1 | EN1234 | 0 | 1 | indept | x | CH1 | CH4 | CH3 | CH2 |

X : don't care but suggested to be LOW (0).

### Power On/Off Sequence Example for CH2 to CH5

Sequence 1: SEQ is high, EN3 is high, EN4 is low.

EN2 will turn on/off CH2 to CH5 in preset sequence. CH1 will be turned on by EN1 independently.

CH2 to CH5 Power On Sequence is :

When EN2 goes high, CH2 will be turned on . 7ms after CH2 is turned on, CH3 will be turned on. 7ms after CH3 is turned on, CH4 will be turned on. 7ms after CH4 is turned on, CH5 will be turned on.

CH2 to CH5 Power-Off Sequence is :

When EN2 goes low, CH5 will be turned off and VOUT5 will be internally discharged. When VOUT5 discharging finishes, CH4 will turn off and internally discharge output via LX4 pin. When FB4 < 0.1V, CH3 will turn off and internally discharge output via LX3 pin. Likewise when FB3 < 0.1V, CH2 will turn off and discharge output via LX2 pin. After FB2 < 0.1V, CH2 to 5 shutdown sequence will be completed.

Sequence 2 : SEQ is high, EN3 is low, EN4 is low, EN5 is low.

EN2 will turn on/off CH2 to CH5 in preset sequence. CH1 will be turned on by EN1 independently.

CH2 to CH5 Power On Sequence is :

When EN2 goes high, CH2 will be turned on . 7ms after CH2 is turned on, CH5 will be turned on. About 1ms after Ch5 is turned on, CH3 will be turned on. 7ms after CH3 is turned on, CH4 will be turned on.

CH2 to CH5 Power-Off Sequence is :

When EN2 goes low, CH4 will turn off first and internally discharge output via LX4 pin. When FB4 < 0.1V, CH3 will turn off and internally discharge output via LX3 pin. Likewise, when FB3 < 0.1V, CH5 will turn off and VOUT5 will be internally discharged. When VOUT5 discharging finishes, CH2 will turn off and discharge output via LX2 pin. After FB2 < 0.1V, CH2 to 5 shut down sequence will be completed.

Table 4. CH2 to CH5 Power On/Off Sequence

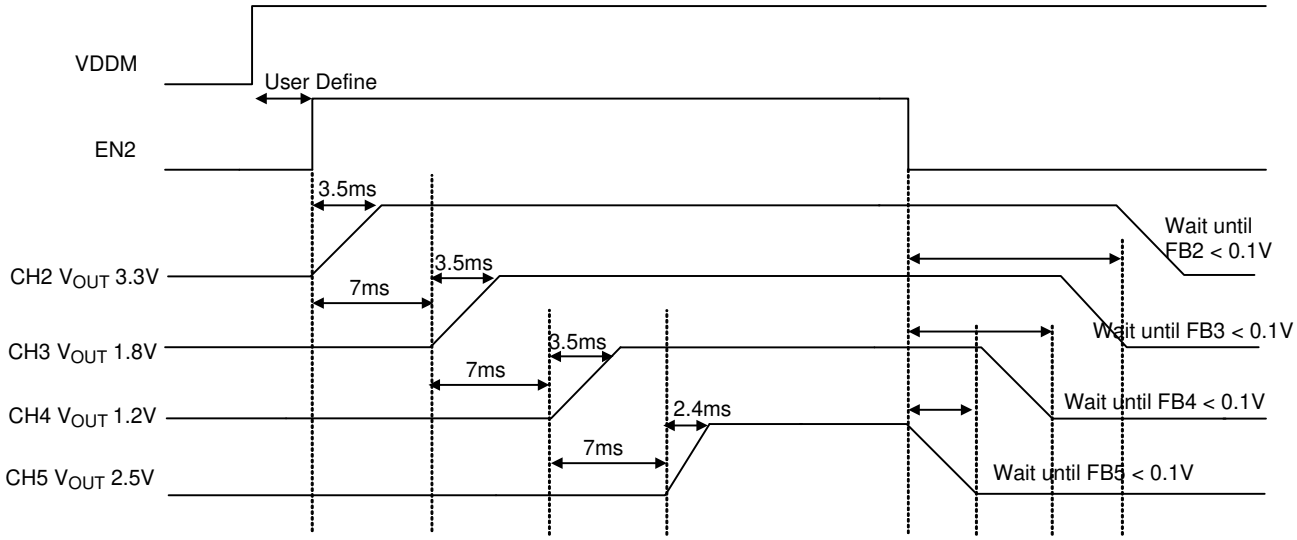
| EN3 to EN5 Setting | Power On Sequence |
|---|---|
| EN3 = H, EN4 = L, EN5 = X | CH2→CH3→CH4→CH5 |
| EN3 = L, EN4 = L, EN5 = L | CH2→CH5→CH3→CH4 |
| **EN3 to EN5 Setting** | **Power Off Sequence** |
| EN3 = H, EN4 = L, EN5 = X | CH5→CH4→CH3→CH2 |
| EN3 = L, EN4 = L, EN5 = L | CH4→CH3→CH5→CH2 |

**Timing Diagram for CH2 to CH5**

Power On Sequence : CH2 Step-Down 3.3V→CH3 Step-Down 1.8V→CH4 Step-Down 1.2V→CH5 LDO 2.5V

Power Off Sequence : CH5 LDO 2.5V→CH4 Step-Down 1.2V→CH3 Step-Down 1.8V→CH2 Step-Down 3.3V

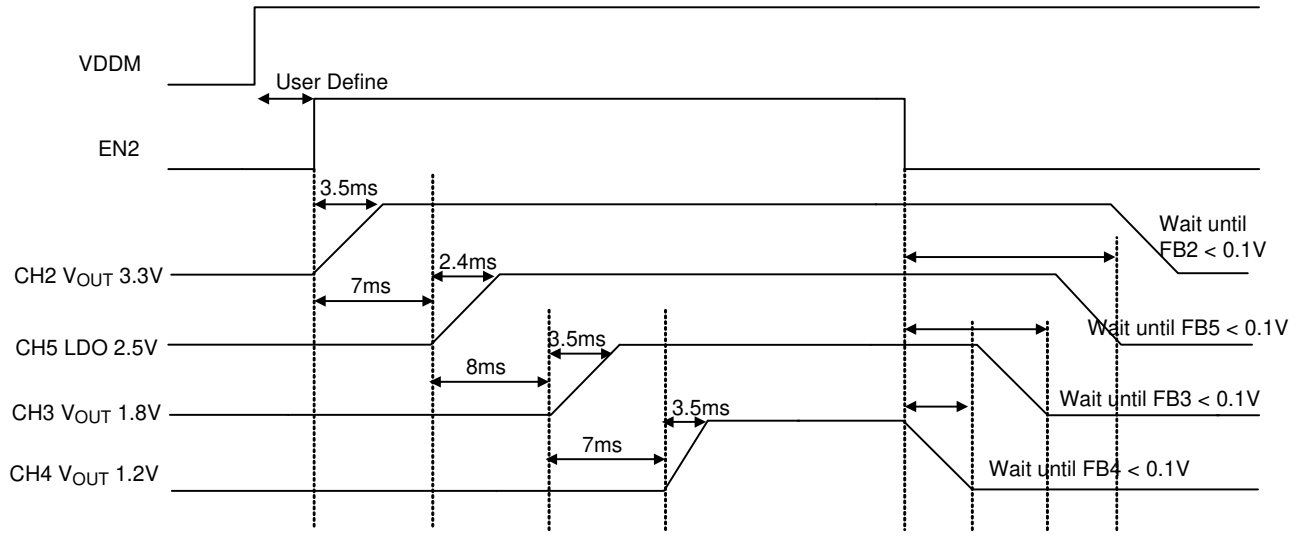
SEL = H, SEQ = H, EN3 = H, EN4 = L




Power On Sequence : CH2 Step-Down 3.3V→CH5 LDO 2.5V→CH3 Step-Down 1.8V→CH4 Step-Down 1.2V

Power Off Sequence : CH4 Step-Down 1.2V→CH3 Step-Down 1.8V→CH5 LDO 2.5V→CH2 Step-Down 3.3V

SEL = H, SEQ = H, EN3 = L, EN4 = L, EN5 = L



**Power on/off sequence for CH1 to CH4**

Sequence 3 : SEQ is high, EN3 is high, EN4 is high.

EN2 will turn on/off CH1 to CH4 in preset sequence. CH5 will be turned on by EN5 independently.

CH1 to CH4 Power On Sequence is :

When EN2 goes high, CH1 will be turned on. 7ms after CH1 is turned on, CH3 will be turned on. 7ms after CH3 is turned on, CH4 will be turned on. 7ms after CH4 is turned on, CH2 will be turned on.

CH1 to CH4 Power-Off Sequence is :

When EN2 goes low, CH2 will turn off first and internally discharge output. When FB2 < 0.1V, CH4 will turn off and also internally discharge output via LX4 pin. When FB4 < 0.1V, CH3 will turn off and internally discharge output via LX3 pin. Likewise, when FB3 < 0.1V, CH1 will turn off and discharge output via LX1 pin. After FB1 < 0.1V, CH1 to 4 shutdown sequence will be completed.

Sequence 4 : SEQ is high, EN3 is low, EN4 is high.

EN2 will turn on/off CH1 to CH4 in preset sequence. CH5 will be turned on by EN5 independently.

CH1 to CH4 Power On Sequence is :

When EN2 goes high, CH1 will be turned on first. 7ms after CH1 is turned on, CH4 will be turned on. 7ms after CH4 is turned on, CH3 will be turned on. 7ms after CH3 is turned on, CH2 will be turned on.

CH1 to CH4 Power Off Sequence is :

When EN2 goes low, CH2 will turn off first and internally discharge output. When FB2 < 0.1V, CH3 will turn off and internally discharge output via LX3 pin. When FB3 < 0.1V, CH4 will turn off and internally discharge output via LX4 pin. Likewise when FB4 < 0.1V, CH1 will turn off and internally discharge output via LX1 pin. After FB1 < 0.1V, Ch1 to 4 shutdown sequence is completed.

**Table 5. CH1 to CH4 Power On/Off Sequence**

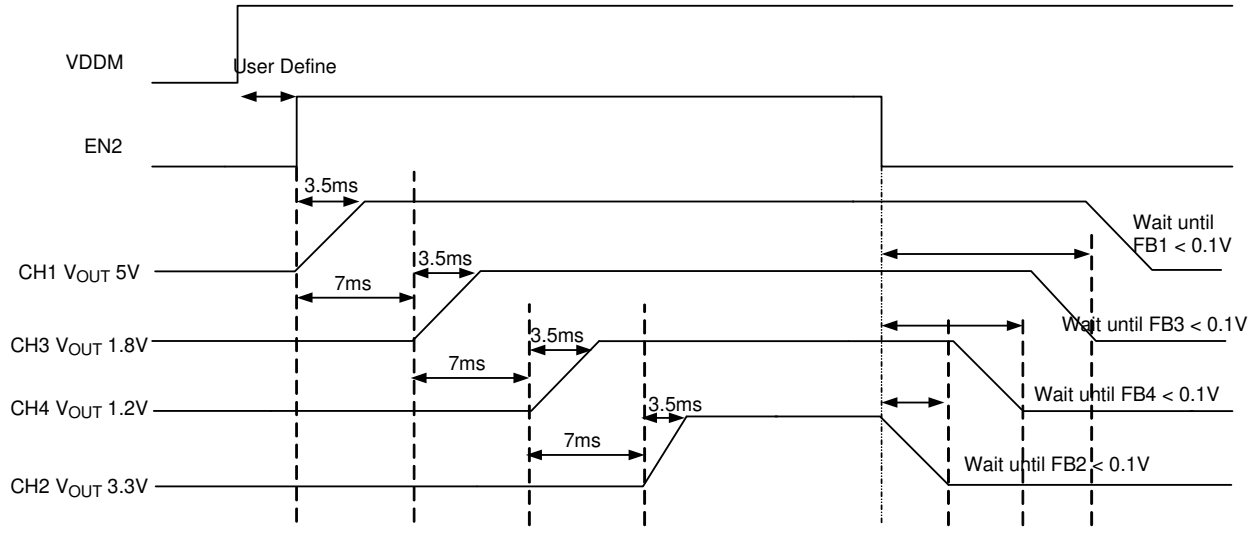
| Enable Setting | Power On Sequence |
|---|---|
| EN3 = H, EN4 = H, EN1 = X | CH1→CH3→CH4→CH2 |
| EN3 = L, EN4 = H, EN5 = X | CH1→CH4→CH3→CH2 |
| **Enable Setting** | **Power Off Sequence** |
| EN3 = H, EN4 = H, EN5 = X | CH2→CH4→CH3→CH1 |
| EN3 = L, EN4 = H, EN5 = X | CH2→CH3→CH4→CH1 |

**Timing Diagram for CH1 to CH4**

Power On Sequence : CH1 Step-Up 5V→CH3 Step-Down 1.8V→CH4 Step-Down 1.2V →CH2 Step-Up 3.3V

Power Off Sequence : CH2 Step-Up 3.3V→CH4 Step-Down 1.2V→CH3 Step-Down 1.8V→CH1 Step-Up 5V

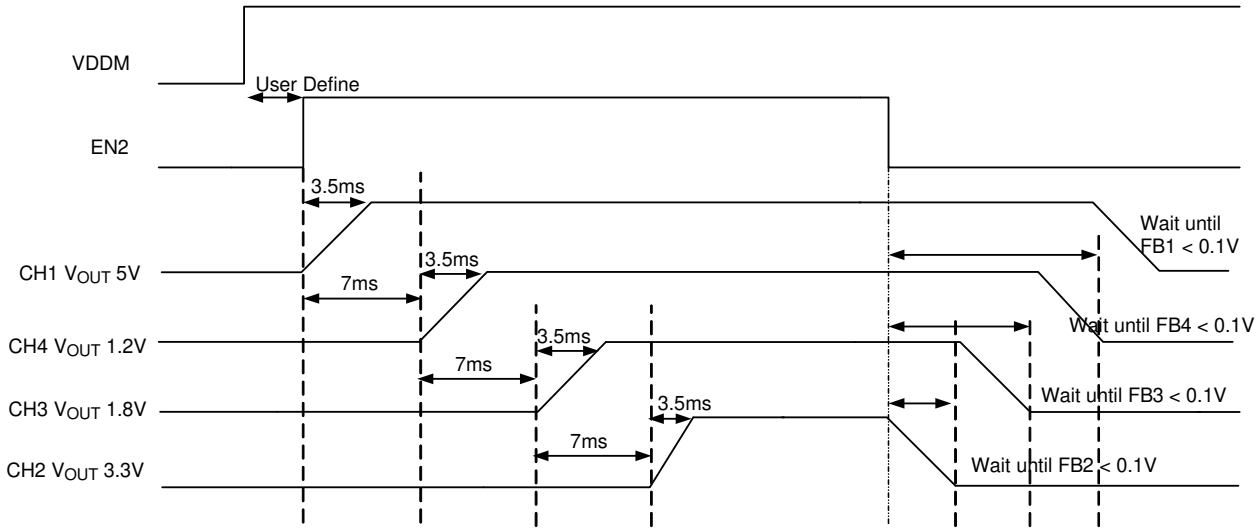
SEL = L, SEQ = H, EN3 = H, EN4 = H



Power On Sequence : CH1 Step-Up 5V →CH4 Step-Down 1.2V→CH3 Step-Down 1.8V→CH2 Step-Up 3.3V

Power Off Sequence : CH2 Step-Up 3.3V→CH3 Step-Down 1.8V→CH4 Step-Down 1.2V →CH1 Step-Up 5V

SEL = L, SEQ = H, EN3 = L, EN4 = H




## Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, $T_A$ is the ambient temperature, and $\theta_{JA}$ is the junction to ambient thermal resistance.

For recommended operating condition specifications of the RT9992, the maximum junction temperature is 125°C and $T_A$ is the ambient temperature. The junction to ambient thermal resistance, $\theta_{JA}$, is layout dependent. For WQFN-32L 4x4 packages, the thermal resistance, $\theta_{JA}$, is 27.8°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at $T_A$ = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C ) / (27.8°C/W) = 3.59W for WQFN-32L 4x4 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, $\theta_{JA}$. For the RT9992 package, the derating curve in Figure 1 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

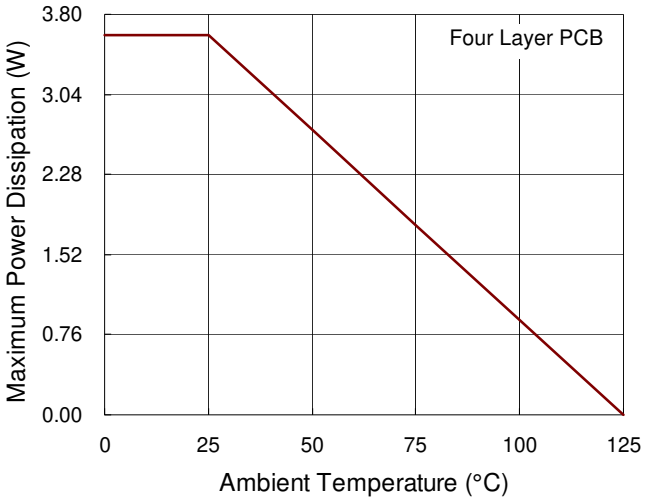



Figure 1. Derating Curve for the RT9992 Package

### Layout Considerations

For the best performance of the RT9992, the following PCB layout guidelines must be strictly followed.

- Place the input and output capacitors as close as possible to the input and output pins respectively for good filtering.
- Keep the main power traces as wide and short as possible.
- The switching node area connected to LX and inductor should be minimized for lower EMI.
- Place the feedback components as close as possible to the FB pin and keep these components away from the noisy devices.
- Connect the GND and Exposed Pad to a strong ground plane for maximum thermal dissipation and noise protection.
- Directly connect the output capacitors to the feedback network of each channel to avoid bouncing caused by parasitic resistance and inductance from the PCB trace.

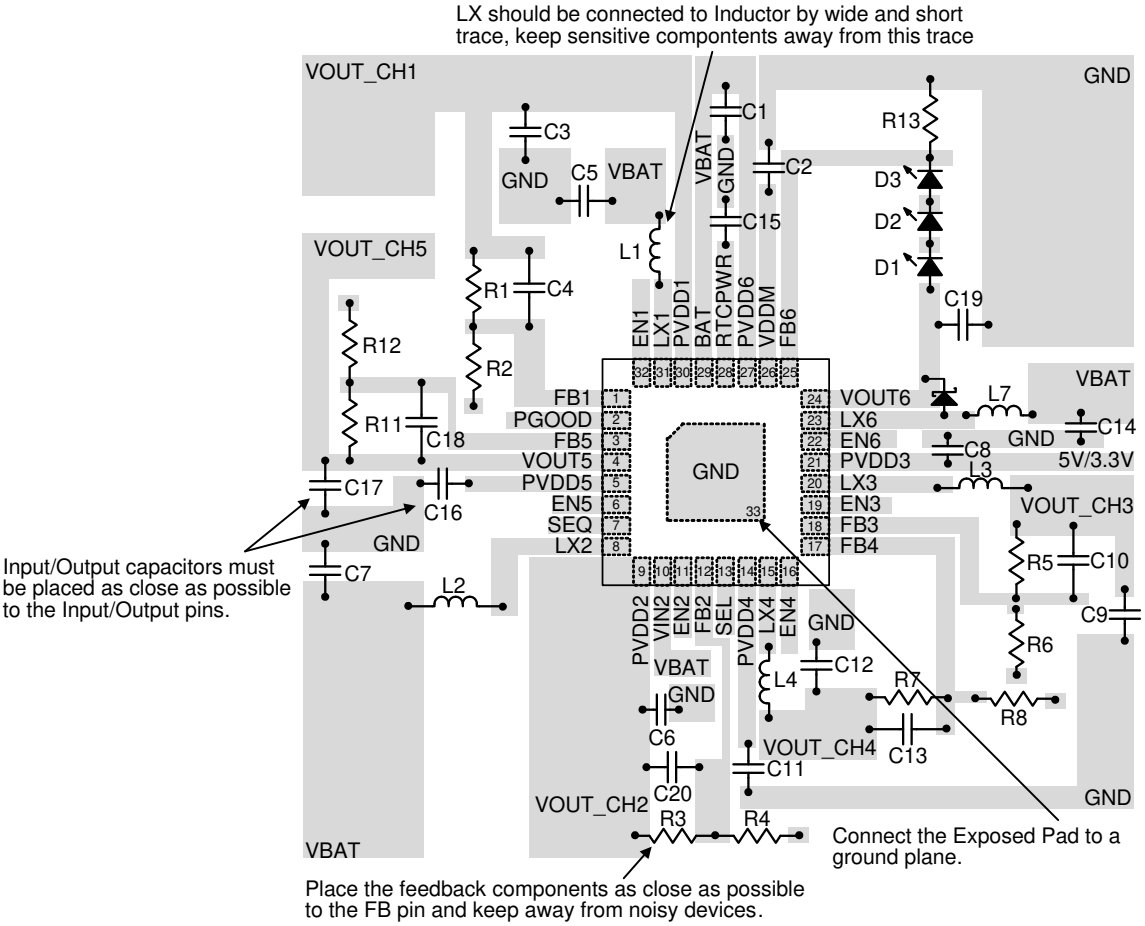
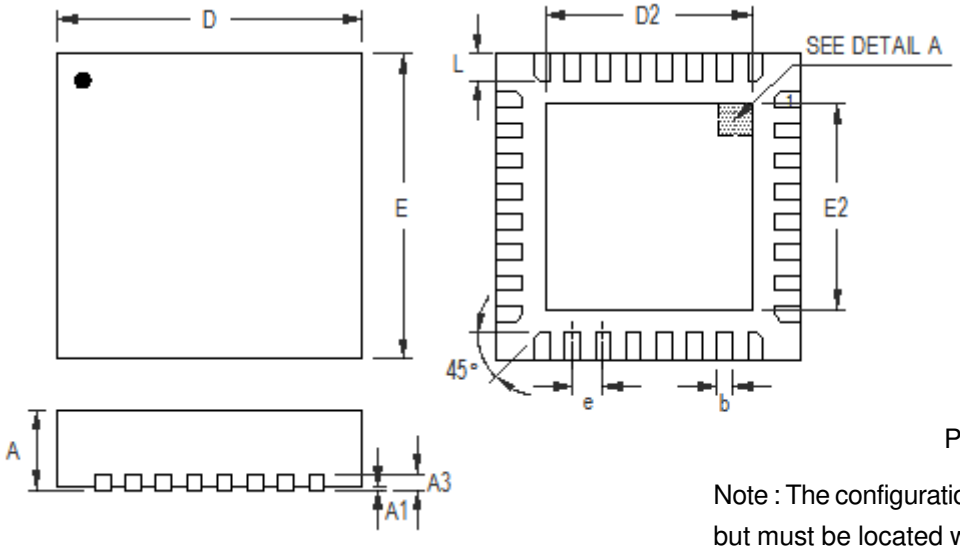


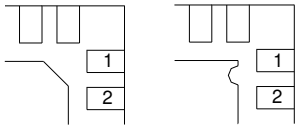

Figure 2. PCB Layout Guide

Table 6. Protection Action

| | Protection Type | Threshold(typical) Refer to Electrical spec | Delay Time | Protection Methods |
|---|---|---|---|---|
| $V_{DDM}$ | UVLO | VDDM < 2.1V | No delay | Disable all channels |
| | OVP | VDDM > 6.15V | 100ms | IC shutdown |
| BAT | UVLO | $V_{BAT}$ < 1.3V | No delay | Disable all channels |
| CH1 : Boost | Current Limit | N-MOSFET current > 3A | 100ms | IC shutdown |
| | PVDD1 UVP | $V_{FB1}$ < 0.4V, or $V_{PVDD1}$ < $V_{BAT}$–0.8V or $V_{PVDD1}$ < 1.3V | 100ms | IC shutdown |
| | PVDD1 OVP | $V_{PVDD1}$ > 6.15V | No delay | IC shutdown |
| CH2 : Boost | Current Limit | N-MOSFET current > 2.1A | 100ms | IC shutdown |
| | PVDD2 UVP | $V_{FB2}$ < 0.4V, or $V_{PVDD2}$ < $V_{IN2}$ – 0.8V or $V_{PVDD2}$ < 1.3V | 100ms | IC shutdown |
| | PVDD2 OVP | $V_{PVDD2}$ > 6.15V | No delay | IC shutdown |
| CH2 : Buck | OCP | P-MOSFET current > 1.5A | 100ms | IC shutdown |
| | UVP | $V_{FB2}$ < 0.4V | 100ms | IC shutdown |
| CH3 : Buck | OCP | P-MOSFET current > 1.5A | 100ms | IC shutdown |
| | UVP | $V_{FB3}$ < 0.4V | 100ms | IC shutdown |
| CH4 : Buck | OCP | P-MOSFET current > 2A | 100ms | IC shutdown |
| | UVP | $V_{FB4}$ < 0.4V | 100ms | IC shutdown |
| CH5 | Current Limit | P-MOSFET current > 0.38A | 100ms | IC shutdown |
| | UVP | $V_{FB5}$ < 0.3V | 100ms | IC shutdown |
| CH6 Asyn Boost | Current Limit | N-MOSFET current > 0.8A | Reset each cycle | |
| | OVP | $V_{OUT6}$ > 19.5V | No delay | Shut down CH6 only |
| Thermal | Thermal shutdown | Temperature > 160°C | No delay | All channels stop switching |

## Outline Dimension




**DETAIL A**

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 0.700 | 0.800 | 0.028 | 0.031 |
| A1 | 0.000 | 0.050 | 0.000 | 0.002 |
| A3 | 0.175 | 0.250 | 0.007 | 0.010 |
| b | 0.150 | 0.250 | 0.006 | 0.010 |
| D | 3.900 | 4.100 | 0.154 | 0.161 |
| D2 | 2.650 | 2.750 | 0.104 | 0.108 |
| E | 3.900 | 4.100 | 0.154 | 0.161 |
| E2 | 2.650 | 2.750 | 0.104 | 0.108 |
| e | 0.400 | | 0.016 | |
| L | 0.300 | 0.400 | 0.012 | 0.016 |

**W-Type 32L QFN 4x4 Package**

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