AXEL LITE

Solo / Dual / Quad
ARM Cortex-A9 MPCore
CPU Module

LITE LINE

HARDWARE MANUAL

DAVE Embedded Systems www.dave.eu info@dave.eu

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1 Preface

1.1 About this manual

This Hardware Manual describes the **AXEL LITE** CPU module design and functions.
Precise specifications for the Freescale i.MX6 processor can be found in the CPU datasheets and/or reference manuals.

1.2 Copyrights/Trademarks

1.3 Standards

DAVE Embedded Systems is certified to ISO 9001 standards.

1.4 Disclaimers

DAVE Embedded Systems does not assume any responsibility about availability, supplying and support regarding all the products mentioned in this manual that are not strictly part of the **AXEL LITE** CPU module.
AXEL LITE CPU Modules are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. **DAVE Embedded Systems** customers who are using or selling these products for use in such applications do so at their own risk and agree to fully indemnify **DAVE Embedded Systems** for any damage resulting from such improper use or sale.

1.5 Warranty

AXEL LITE is warranted against defects in material and workmanship for the warranty period from the date of shipment. During the warranty period, **DAVE Embedded Systems** will at its discretion decide to repair

or replace defective products. Within the warranty period, the repair of products is free of charge as long as warranty conditions are observed. The warranty does not apply to defects resulting from improper or inadequate maintenance or handling by the buyer, unauthorized modification or misuse, operation outside of the product's environmental specifications or improper installation or maintenance.
DAVE Embedded Systems will not be responsible for any defects or damages to other products not supplied by **DAVE Embedded Systems** that are caused by a faulty **AXEL LITE** module.

1.6 Technical Support

We are committed to making our product easy to use and will help customers use our CPU modules in their systems. Technical support is delivered through email to our valued customers. Support requests can be sent to support-axel@dave.eu.
Software upgrades are available for download in the restricted access download area of **DAVE Embedded Systems** web site: http://www.dave.eu/reserved-area. An account is required to access this area and is provided to customers who purchase the development kit (please contact support-axel@dave.eu for account requests)..
Please refer to our Web site to http://www.dave.eu/products/axel-lite for the latest product documentation, utilities, drivers, Product Change Notifications, Board Support Packages, Application Notes, mechanical drawings and additional tools and software.

1.7 Related documents

Document	Location
DAVE Embedded Systems Developers Wiki	http://wiki.dave.eu/index.php/Main_Page
NXP i.MX 6Dual/6Quad Applications Processor Reference Manual	http://cache.freescale.com/files/32bit/doc/ref_manual/IMX6DQRM.pdf?fpsp=1&WT_TYPE=Reference%20Manuals&WT_VENDOR=FREESCALE&WT_FILE_FORMAT=pdf&WT_ASSET=Documentation

Tab. 1: Related documents

1.8 Conventions, Abbreviations, Acronyms

Abbreviation	Definition
i.MX 6 APRM	i.MX 6 Application Processor Reference Manual
IPU	Image Processing Unit
GPI	General purpose input
GPIO	General purpose input and output
GPO	General purpose output
PCB	Printed circuit board
RTC	Real time clock
SOM	System on module
TRM	Technical Reference Manual
XELK	Axel Embedded Linux Kit

Tab. 2: Abbreviations and acronyms used in this manual

Revision History

Version	Date	Notes
0.8.0	February 2014	First Draft
0.8.5	February 2014	First Revision
0.9.0	February 2014	First Release
0.9.1	May 2014	Minor fixes Added J7 pinout Completed Section 5 Added UART4 interface
0.9.2	August 2014	Fixed PGOOD signal description
0.9.3	November 2014	Minor fixes
0.9.4	October 2016	Minor fixes
0.9.5	October 2016	Minor fixes

2 Introduction

AXEL LITE is the new top-class Single - Dual - Quad Core ARM Cortex-A9 CPU module by DAVE Embedded Systems, based on the recent NXP i.MX6 application processor. Thanks to **AXEL LITE**, customers have the chance to save time and resources by using a compact solution that permits to reach scalable performances that perfectly fits the application requirements avoiding complexities on the carrier board. The use of this processor enables extensive system-level differentiation of new applications in many industry fields, where high-performance and extremely compact form factor (67,5 mm x 43 mm) are key factors. Smarter system designs are made possible, following the trends in functionalities and interfaces of the new, state-of-the-art embedded products.

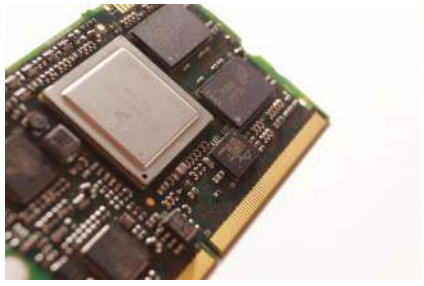


Fig. 1: AXEL-LITE- Powered by I.MX6 processor

Fig. 2: AXEL-LITE – Solo / Dual / Quad core ARM Cortex A9

AXEL LITE enables designers to create smart products suitable for harsh mechanical and thermal environments, allowing the development of high computing and reliable solutions. Thanks to the tight integration between the ARM Core-based processing system, designers are able to share the application through the multi-core platform and/or to divide the task on different cores in order to match with specific application requirements (thanks to AMP is possible to create application where RTOS and Linux works together on different cores). **AXEL LITE** is designed in order to keep full compatibility

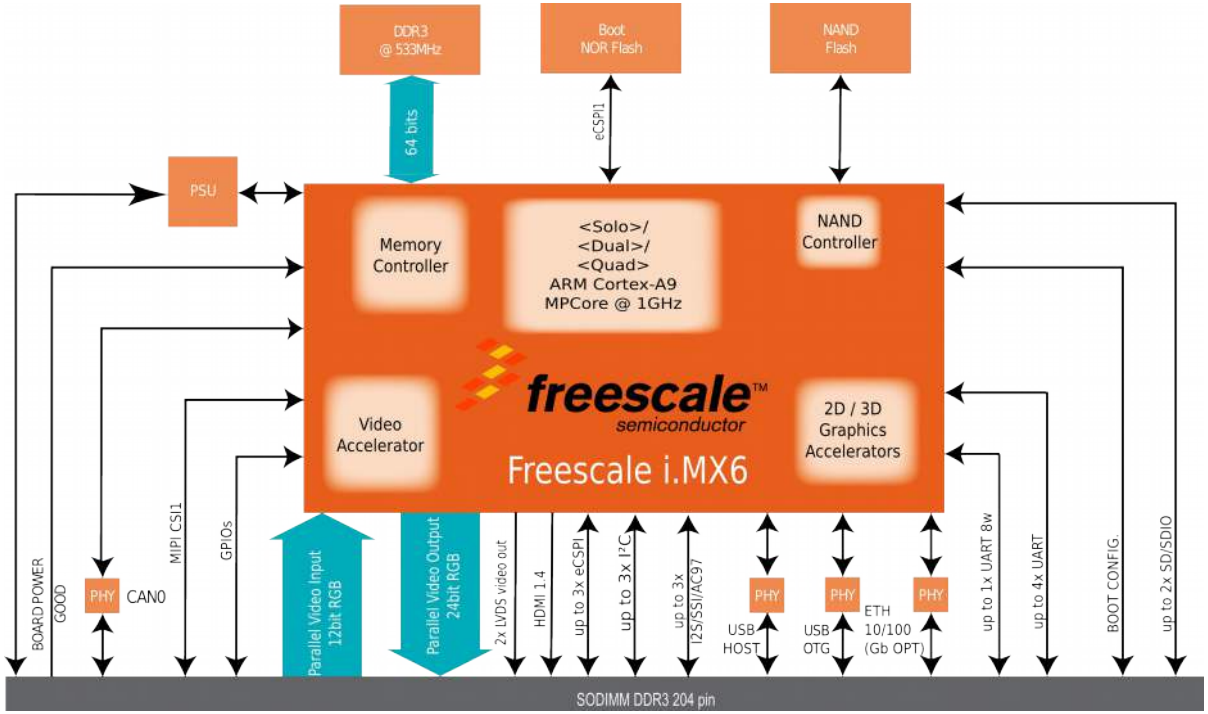
with the **LITE Line** CPU modules where quality and reliability are important factors.

2.1 Product Highlights

- Unmatched performances thanks to Solo / Dual / Quad Core @ 1.2 GHz
- All memories you need on-board
- Boot from NOR for safe applications
- Enabling massive computing applications thanks to wide range DDR3 RAM memory up to 2GB
- Single 3V3 Power Supply
- Reduced carrier complexity: SDIO, dual CAN, USB, Ethernet with on-board PHY, GPIOs
- Multiple video outputs available
- H264 Video encoding and decoding
- Multiple video inputs available

Fig. 3: AXEL LITE SOM (top view)

2.2 Block Diagram



2.3 Feature Summary

Feature	Specifications	Options
CPU	NXP i.MX6 S/D/Q ARM Cortex A9 MPCore @ 1.2 GHz	
Cache	L1: 32Kbyte instruction, 32Kbyte data L2: Unified data/instruction, 1 MByte	
RAM	Default: up to 2GB DDR3 (for 4GB support please contact our sales department) x64 data bus width @ 533 MHz	
Storage	Bootable SPI NOR 16, 32, 64 MB Flash NAND: all sizes, on request	
Expansion bus	One PCI Express 2.0 lane with integrated PHY (5.0 GT/s Endpoint/Root Complex operations)	

Tab. 3: CPU, Memories, Busses

Feature	Specifications	Options
Graphics Controller	16-/24-bit HD Display Port 1x HDMI 1.4 channel + DDC 1x TFT/RGB output port 2x LVDS output ports	
2D/3D Engines	GPU2D cores for raster (R2D, Vivante GC320) and vector (V2D, Vivante GC355) graphics acceleration GPU3D core (Vivante GC2000) for OpenGL/OpenGL ES/OpenVG/OpenCL API acceleration	
Video capture	1x RGB Parallel port 12 bit 1x MIPI CSI port	
Video processing	High performance, multi-standard VPU Up to 1080p60 H264 decode Up to 1080p30 H264 encode	
Coprocessors	Media Processing Engine with NEON™ & VFPv3-D32 Floating-Point Unit	
USB	1x 2.0 OTG port (PHY on board) 1x 2.0 Host port (PHY on board)	
UARTs	5x UART ports (up to 1x full, up to 4x four-wires)	
GPIO	Available lines, shared with other functions	

Feature	Specifications	Options
	(interrupts available)	
Networks	Default: Fast Ethernet 10/100 Mbps with integrated PHY (for Gigabit support please contact our sales department)	
CAN	2x CAN 2.0B ports (1x with integrated PHY)	
SD/MMC	up to 3x SD 3.0 /SDIO 3.0/MMC 4.x compliant controllers	
Serial buses	5x full-duplex SPI ports with four peripheral chip selects 3x master and slave I²C interfaces	
Audio	up to 3x I²S / SSI / AC97	
Timers	Enhanced Periodic Interrupt Timer General Purpose Timer	
Debug	JTAG IEEE 1149.1 Test Access Port CoreSight™ and Program Trace Macrocell (PTM)	

Tab. 4: Peripherals

Feature	Specifications	Options
Supply Voltage	Single 3.3V input, voltage regulation on board	
Active power consumption	See section 8.3 - Power consumption	
Dimensions	67.5mm x 43mm	
Operating temperature range	Commercial: 0°C / +70°C Industrial: -40°C / +85°C	
Connectors	SODIMM 204 pins	

Tab. 5: Electrical, Mechanical and Environmental Specifications

3 Design overview

The heart of **AXEL LITE** module is composed by the following components:

- NXP i.MX6 Solo / Dual / Quad core SoC application processor
- Power supply unit
- DDR memory banks
- NOR and NAND flash banks
- 1x 204 pin SODIMM connector with interfaces signals

This chapter shortly describes the main **AXEL LITE** components.

3.1 Freescale i.MX6 application processor

The i.MX6 Solo/Dual/Quad processors feature NXP's advanced implementation of the ARM® Cortex®-A9 MPCore, which operates at speeds up to 1.2 GHz. They include 2D and 3D graphics processors, 1080p video processing, and integrated power management. As a result, the i.MX6 devices are able to serve a wide range of applications including:

- Automotive driver assistance, driver information, and infotainment
- Multimedia-centric smart mobile devices
- Instrument clusters, and portable medical devices.
- E-Readers, smartbooks, tablets
- Intelligent industrial motor control, industrial networking, and machine vision
- IP and Smart camera
- Human-machine interfaces
- Medical diagnostics and imaging
- Digital signage

- Video and night vision equipment
- Multimedia-focused products
- Entertainment and gaming appliances

The i.MX6 application processor is composed of the following major functional blocks:

- ARM Cortex-A9 MPCore 2x/4x CPU Processor, featuring:
  - 1 Megabyte unified L2 cache shared by all CPU cores
  - NEON MPE co-processor
  - General Interrupt Controller (GIC) with 128 interrupt support
  - Snoop Control Unit (SCU)
  - External memories interconnect
- Hardware accelerators, including:
  - VPU -Video Processing Unit
  - Two IPUv3H -Image Processing Unit (version 3H)
  - 2D/3D/Vector graphics accelerators
- Connectivity peripherals, including
  - PCIe
  - SATA
  - SD/SDIO/MMC
  - Serial buses: USB, UART, I²C, SPI, ...

AXEL LITE can mount three versions of the i.MX6 processor. The following table shows a **comparison** between the processor models, highlighting the differences:

Processor	# cores	Clock	L2 cache	DDR3	Graphics acceleration	IPU	VPU	SATA-II
i.MX6 Solo	1	800 MHz 1 GHz	512 KB	32 bit @ 400 MHz	*3D*: Vivante GC880 *2D*: Vivante GC320 *Vector*: N.A.	1x	1x	N.A.
i.MX6 Dual	2	850 MHz 1 GHz 1.2 GHz	1 MB	64 bit @ 533 MHz	*3D*: Vivante GC2000 *2D*: Vivante GC320 *Vector*: Vivante GC335	2x	2x	Yes
i.MX6 Quad	4	850 MHz 1 GHz 1.2 GHz	1MB	64 bit @ 533 MHz	*3D*: Vivante GC2000 *2D*: Vivante GC320 *Vector*: Vivante GC335	2x	2x	Yes

Tab. 6: i.MX6 comparison

3.2 DDR3 memory bank

DDR3 SDRAM memory bank is composed by 4x 16-bit width chips resulting in a 64-bit combined width bank.
The following table reports the SDRAM specifications:

CPU connection	Multi-mode DDR controller (MMDC)
Size min	512 MB
Size max	2 GB (for 4GB support please contact our sales department)
Width	64 bit
Speed	533 MHz

Tab. 7: DDR3 specifications

3.3 NOR flash bank

NOR flash is a Serial Peripheral Interface (SPI) device. This device is connected to the eCSPI channel 1. Specific models of the **AXEL LITE** SOM provide the SPI NOR as boot memory.

The following table reports the NOR flash specifications:

CPU connection	eCSPI channel 1

Size min	16 MByte
Size max	64 MByte
Chip select	ECSPI1_SS0
Bootable	Yes

Tab. 8: NOR flash specifications

For **AXEL LITE** models that have the NOR flash bank populated, the eCSPI channel 1 is mapped by design on the following multiplexed pins:

NOR signal	Function	I.MX6 signal	I.MX6 ball #
NOR_CS0n	Chip select	EIM_EB2	E22
NOR_DQ0/MOSI	Serial Input	EIM_D18	D24
NOR_DQ1/MISO	Serial Output	EIM_D17	F21
NOR_SCLQ	Serial clock	EIM_D16	C25

Tab. 9: eCSPI1 pin mapping

3.4 NAND flash bank

On board main storage memory is a 8-bit wide NAND flash connected to the CPU's Raw NAND flash controller. Optionally, it can act as boot peripheral.
The following table reports the NAND flash specifications:

CPU connection	Raw NAND flash controller
Page size	512 byte, 2 kbyte or 4 kbyte
Size min	128 MByte
Size max	2 GByte
Width	8 bit
Chip select	NANDF_CS0
Bootable	Yes

Tab. 10: NAND flash specifications

3.5 Memory Map

For detailed information, please refer to chapter 2 “Memory Maps” of the i.MX Applications Processor Reference Manual.

3.6 Power supply unit

AXEL LITE, as the other **LITE Line** CPU modules, embeds all the elements required for powering the unit, therefore power sequencing is self-contained and simplified. Nevertheless, power must be provided from carrier board, and therefore users should be aware of the ranges power supply can assume as well as all other parameters. For detailed information, please refer to Section 5.1 Power Supply Unit (PSU) and recommended power-up sequence.

3.7 CPU module connectors

All interface signals **AXEL LITE** provides are routed through SODIMM DDR3 204 pin (named J2). The dedicated carrier board must mount the mating connector and connect the desired peripheral interfaces according to **AXEL LITE** pinout specifications.

For mechanical information, please refer to Section 4 (Mechanical specifications). For pinout and peripherals information, please refer to Sections 6 (Pinout table) and 7 (Peripheral interfaces).

4 Mechanical specifications

This chapter describes the mechanical characteristics of the **AXEL LITE** module.

> *Mechanical drawings are available in DXF format from the Axel page on DAVE Embedded Systems website (http://www.dave.eu/products/axel-lite)*

4.1 Board Layout

The following figure shows the physical dimensions of the **AXEL LITE** module:

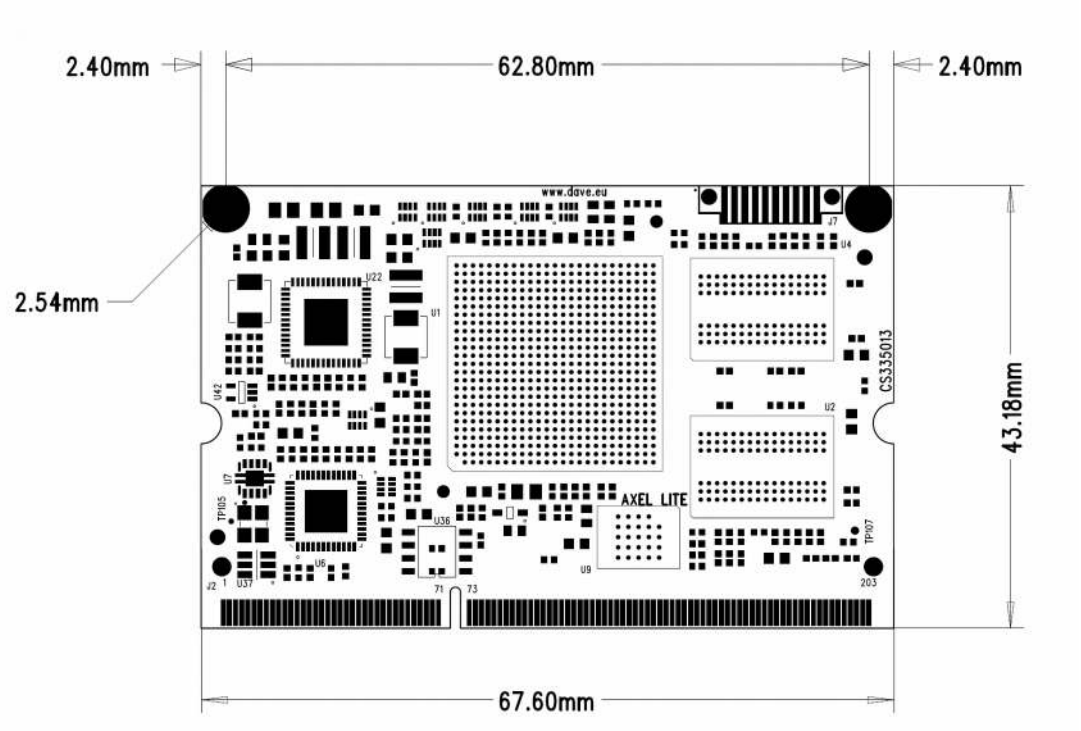


Fig. 4: Board layout - Top view

- Board width: 43.18 mm

- Board height: 67.6 mm
- Maximum components height is 3.4 mm
- PCB thickness is 1.0 mm

4.2 Connectors

The following figure shows the **AXEL LITE** connectors layout:

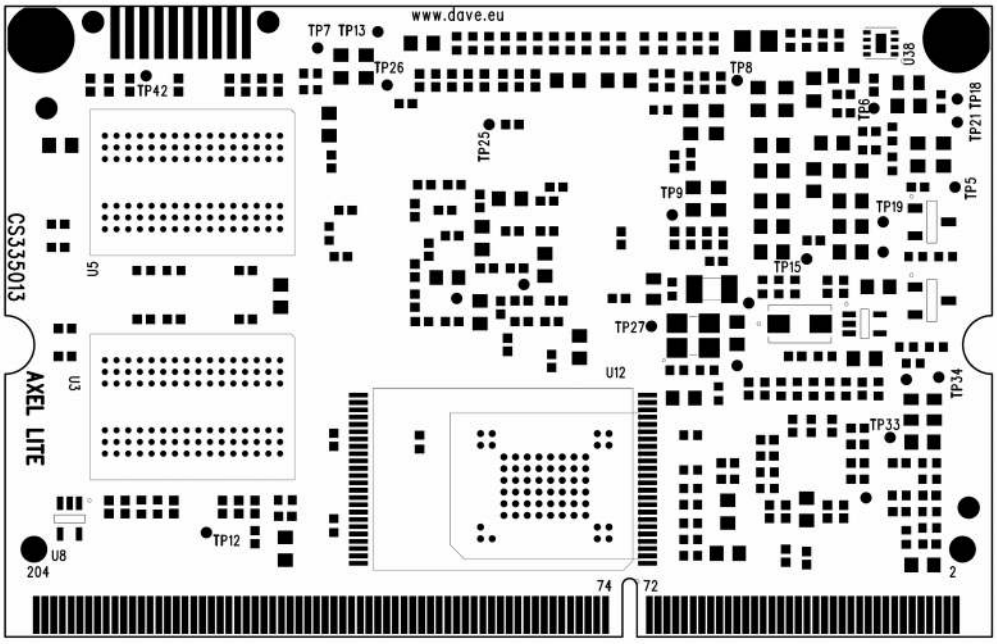


Fig. 5: Board layout - Bottom view

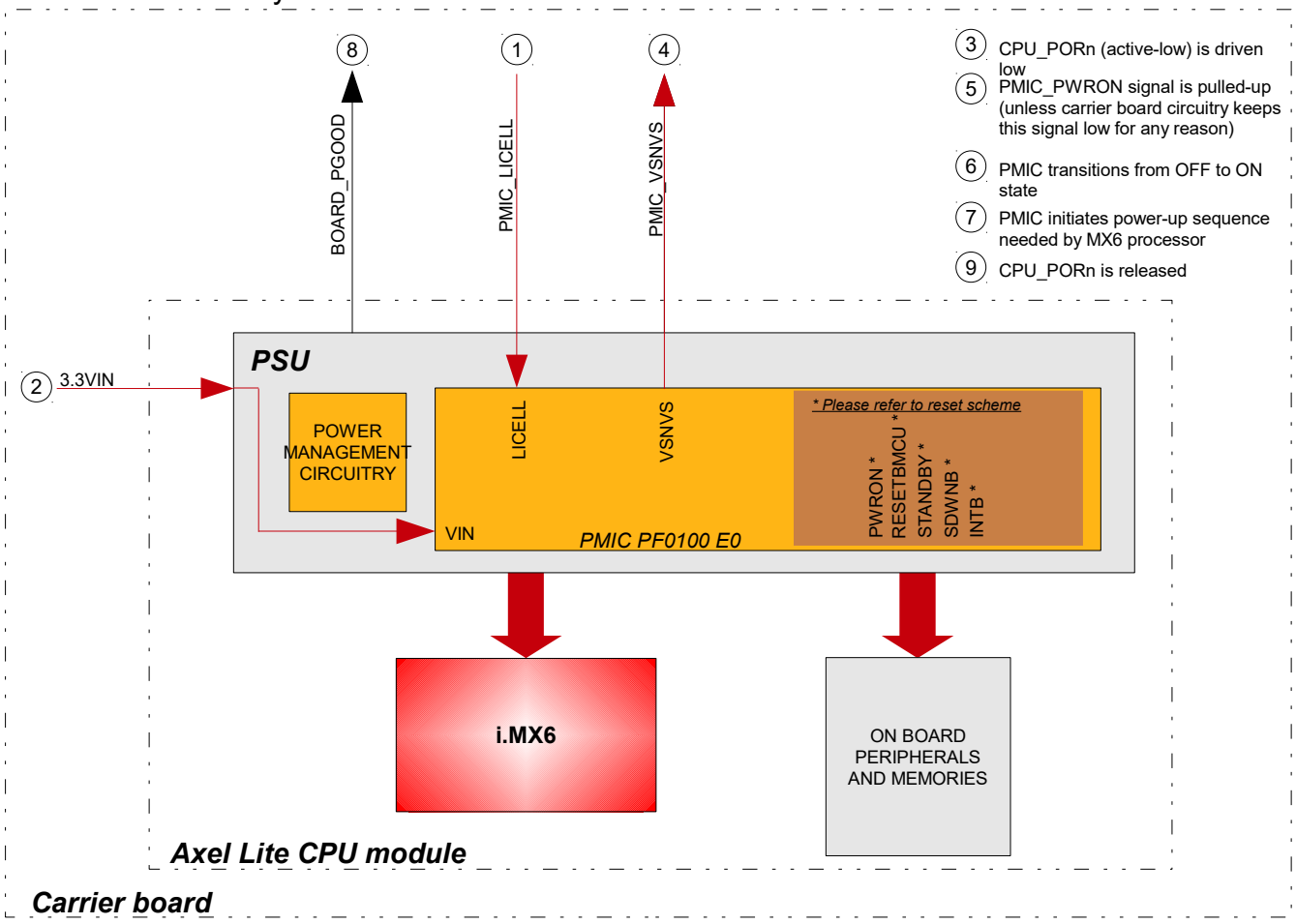
The following table reports connectors specifications:

Part number	Standard SO-DIMM 204-pin (DDR3)
Mating connectors	DDR3 SO-DIMM SOCKET Part number : TE Connectivity 2013289-1

5 Power, reset and control

5.1 Power Supply Unit (PSU) and recommended power-up sequence

Implementing correct power-up sequence for i.MX6 processors is not a trivial task because several power rails are involved. **AXEL LITE** SOM simplifies this task by embedding all the required circuitry. The following picture shows a simplified block diagram of PSU/voltage monitoring circuitry:



The PSU is composed of two main blocks:

- power management integrated circuit (PMIC, NXP PF0100E0 - on request this part is available in automotive grade)
- additional generic power management circuitry that completes PMIC functionalities.

The PSU:

- generates the proper power-up sequence required by i.MX processor and surrounding memories and peripherals
- synchronizes the powering up of carrier board in order to prevent back power
- provides some spare regulated voltages that can be used to power carrier board devices

5.1.1 Power-up sequence

The typical power-up sequence is the following:

1. (optional) PMIC_LICELL is powered
2. 3.3VIN main power supply rail is powered
3. CPU_PORn (active-low) is driven low
4. PMIC activates PMIC_VSNVS power output
5. PMIC_PWRON signal is pulled-up (unless carrier board circuitry keeps this signal low for any reason)
6. PMIC transitions from OFF to ON state
7. PMIC initiates power-up sequence needed by MX6 processor
8. BOARD_PGOOD signal is raised; this active-high signal indicates that SoM's I/O is powered. This signal can be used to manage carrier board power up sequence in order to prevent back powering (from SoM to carrier board or vice versa)
9. CPU_PORn is released.

5.1.2 Power rails and related signals

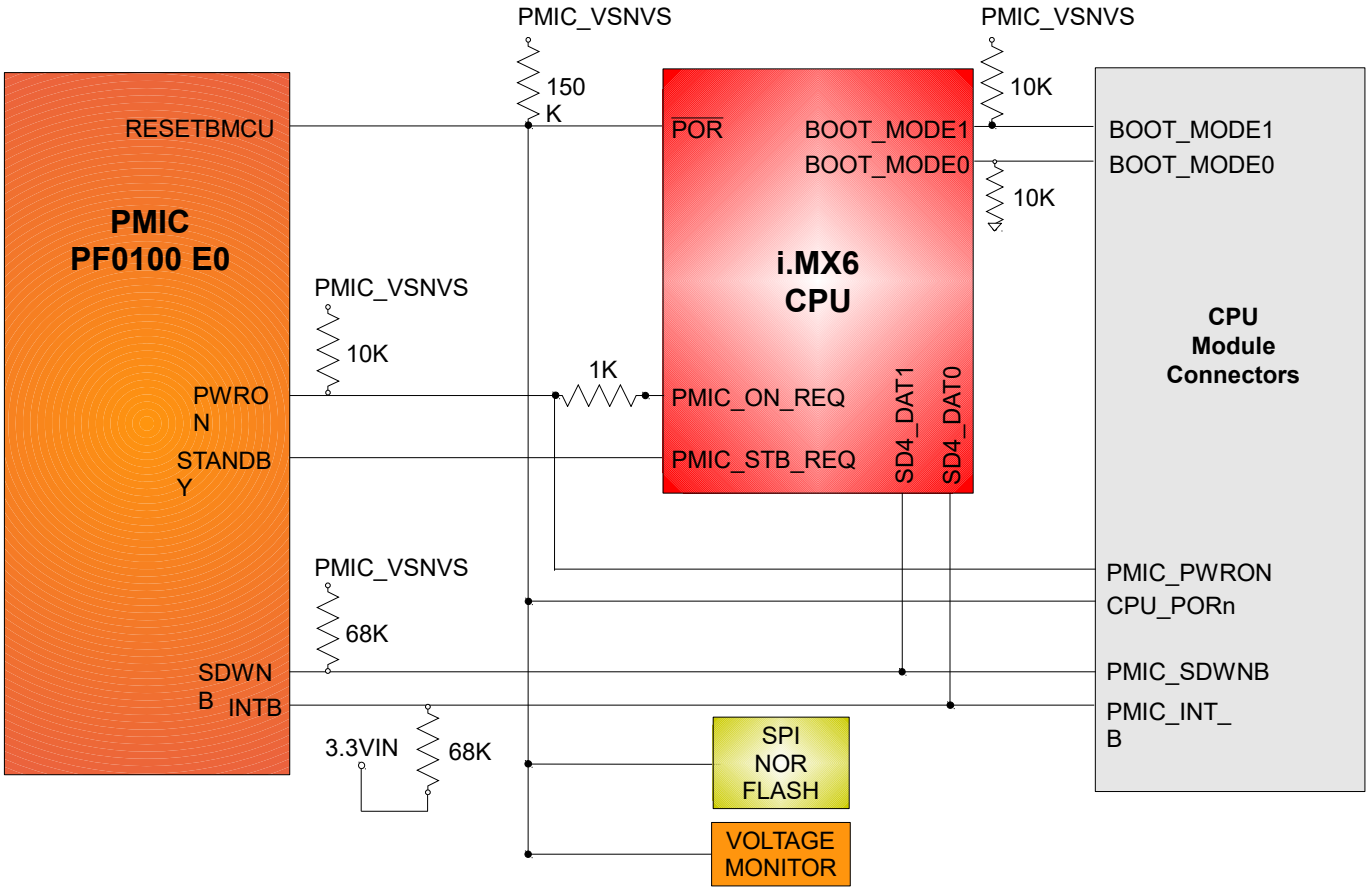
The following list describes in detail power rails and power related signals. **Please note that PMIC regulators output voltages can be changed only if explicitly allowed.**

- 3.3VIN: this is external main power rail. Voltage range is 3.3V ±5%
- PMIC_CELL: PMIC's coin cell supply input/output
- BOARD_PGOOD: this output signal is used to indicate when carrier board's circuitry interfacing **AXEL LITE**'s I/Os has to be powered up

For further details, please refer to the PMIC documentation: *http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=MMPF0100%7CPF0100*

5.2 Reset scheme and control signals

The following picture shows the simplified block diagram of reset scheme and voltage monitoring.



The available reset signals are described in detail in the following sections.

5.2.1 CPU_PORn

The following devices can assert this active-low signal:

- PMIC
- multiple-voltage monitor: this device monitors several critical power voltages and triggers a reset pulse in case any of these exhibits a brownout

condition.

Since SPI NOR flash can be used as boot device, CPU_PORn is connected to this device too. This guarantees it is in a known state when reset signal is released.

5.3 System boot

The boot process begins at Power On Reset (POR) where the hardware reset logic forces the ARM core to begin execution starting from the on-chip boot ROM. The boot ROM:

- determines whether the boot is secure or non-secure
- performs some initialization of the system and clean-ups
- reads the mode pins to determine the primary boot device
- once it is satisfied, it executes the boot code

5.3.1 Boot options

Two options are available related to system boot. They are identified by the Boot field of the ordering code as follows:

- 0: SPI NOR / SD option (SOM code: **DXLxxxx0xxR**)
- 1: NAND / SD option (SOM code: **DXLxxxx1xxR**)

For both options, the selection of primary boot device is determined by the BOOT_MODE_SEL signal as described in the following sections. BOOT_MODE_SEL is latched when processor reset is released.

In any case, boot process is managed by on-chip boot ROM code that is described in detail in processor's Reference Manual.

5.3.1.1 SPI NOR / SD option

Selection of primary boot device is determined by the BOOT_MODE_SEL signal as described in the table below:

BOOT_MODE_SEL	0	1 or floating
Primary boot device	Primary boot device is SD1 (see section 5.5.3 for more details)	Primary boot device is SPI NOR flash connected to eCSPI1 (see section 3.3 for

		more details)
Fallback	In case no valid image is found in SD card, boot ROM shall enable USB serial download mode automatically	In case no valid image is found in NOR flash, boot ROM shall enable USB serial download mode automatically

5.3.1.2 NAND / SD option

Selection of primary boot device is determined by the BOOT_MODE_SEL signal as described in the table below:

BOOT_MODE_SEL	0	1 or floating
Primary boot device	Primary boot device is SD1 (see section 5.5.3 for more details)	Primary boot device is NAND flash (see section 3.4 for more details)
Fallback	In case no valid image is found in SD card, boot ROM shall enable USB serial download mode automatically	In case no valid image is found in NAND flash, boot ROM shall enable USB serial download mode automatically

5.4 Clock scheme

This section will be completed in a future version of this manual.

5.5 Recovery

For different reason, starting from image corruption due power loss during upgrade or unrecoverable bug while developing a new U-Boot feature, the user will need, sooner or later, to recover (*bare-metal* restore) the **AXEL LITE** SOM without using the bootloader itself. The following paragraphs introduce the available options. For further information, please refer to **DAVE Embedded Systems** Developers Wiki or contact the Technical Support Team.

5.5.1 JTAG Recovery

JTAG recovery, though very useful (especially in development or production environment), requires dedicated hardware and software tools. **AXEL LITE** provides an internal connector for the JTAG interface, which, besides the debug purpose, can be used for programming and

recovery operations. For further information on how to use the JTAG interface, please contact the Technical Support Team.

5.5.2 USB Recovery

The USB Serial Downloader provides a means to download the bootloader image to the chip over USB serial connection. Please refer to the XELK Quick Start Guide for further details.

5.5.3 SD/MMC Recovery

MMC recovery is a valuable options that requires no special hardware at all, apart a properly formatted MMC. When SD/MMC boot option is selected, bootrom looks for a valid bootloader on SD/MMC. Once the board is running after booting from SD, reprogramming the flash memory is straightforward. The SD peripheral used for boot is MMC/SD/SDIO1 (please refer to 7.11.1).

5.6 Multiplexing

Most of the i.MX 6 processor pins have multiple signal options. These signal to pin and pin to signal options are selected by the input output multiplexer called IOMUX. The IOMUX enables flexible IO multiplexing and is also used to configure other pin characteristics, such as voltage level, drive strength, and hysteresis. Each IO pad has default and up to seven alternate functions, which are software configurable.

Please refer to the following sections of the i.MX6 APRM for further information pin assignment:

- chapter 4 “External Signals and Pin Multiplexing”
- section 4.1 “Pin assignments”
- section 4.2 “Muxing options”
- chapter 36 “IOMUX Controller (IOMUXC)”

6 Pinout table

This chapter contains the pinout description of the **AXEL LITE** module, grouped in two tables (odd and even pins) that report the pin mapping of the 204-pin SO-DIMM **AXEL LITE** connector.
Each row in the pinout tables contains the following information:

Pin	Reference to the connector pin
Pin Name	Pin (signal) name on the **AXEL LITE** connectors
Internal Connections	Connections to the **AXEL LITE** components: CPU.<x> : pin connected to CPU (PS, processing system) pad named <x> CAN.<x> : pin connected to the CAN transceiver PMIC.<x> : pin connected to the Power Manager IC LAN.<x> : pin connected to the LAN PHY SV.<x>: pin connected to voltage supervisor MTR: pin connected to voltage monitors NOR: pin connected to SPI NOR flash
Ball/pin #	Component ball/pin number connected to signal
Supply Group	Power Supply Group
Type	Pin type: I = Input, O = Output, D= Differential, Z = High impedance, S = Supply voltage, G = Ground, A = Analog signal
Voltage	I/O voltage

6.1 Carrier board mating connector J2

J2 – ODD [1-203]							
Pin	**Pin Name**	**Internal Connections**	**Ball/ pin #**	**Supply Group**	**Type**	**Voltage**	**Note**
J2.1	DGND	DGND	-				
J2.3	3.3VIN	INPUT VOLTAGE					
J2.5	3.3VIN	INPUT VOLTAGE					
J2.7	3.3VIN	INPUT VOLTAGE					
J2.9	3.3VIN	INPUT VOLTAGE					
J2.11	DGND	DGND	-				
J2.13	ETH0_LED1	LAN.LED1/PME_N1	17				
J2.15	ETH0_LED2	LAN.LED2	15				
J2.17	DGND	DGND	-				
J2.19	ETH0_TXRX0_P	LAN.TXRXP_A	2				
J2.21	ETH0_TXRX0_M	LAN.TXRXM_A	3				
J2.23	ETH0_TXRX1_P	LAN.TXRXP_B	5				
J2.25	ETH0_TXRX1_M	LAN.TXRXM_B	6				
J2.27	ETH0_TXRX2_P	LAN.TXRXP_C	7				
J2.29	ETH0_TXRX2_M	LAN.TXRXM_C	8				
J2.31	ETH0_TXRX3_P	LAN.TXRXP_D	10				
J2.33	ETH0_TXRX3_M	LAN.TXRXM_D	11				
J2.35	DGND	DGND	-				
J2.37	SD3_RST	CPU.SD3_RST	D15				
J2.39	SD3_DATA0	CPU.SD3_DATA0	E14				
J2.41	SD3_DATA1	CPU.SD3_DATA1	F14				
J2.43	SD3_DATA2	CPU.SD3_DATA2	A15				
J2.45	SD3_DATA3	CPU.SD3_DATA3	B15				
J2.47	SD3_DATA4	CPU.SD3_DATA4	D13				
J2.49	SD3_DATA5	CPU.SD3_DATA5	C13				
J2.51	SD3_DATA6	CPU.SD3_DATA6	E13				

J2 – ODD [1-203]							
Pin	**Pin Name**	**Internal Connections**	**Ball/ pin #**	**Supply Group**	**Type**	**Voltage**	**Note**
J2.53	SD3_DATA7	CPU.SD3_DATA7	F13				
J2.55	SD3_CMD	CPU.SD3_CMD	B13				
J2.57	DGND	DGND	-				
J2.59	SD3_CLK	CPU.SD3_CLK	D14				
J2.61	SD2_DATA0	CPU.SD2_DATA0	A22				
J2.63	SD2_DATA1	CPU.SD2_DATA1	E20				
J2.65	SD2_DATA2	CPU.SD2_DATA2	A23				
J2.67	SD2_DATA3	CPU.SD2_DATA3	B22				
J2.69	SD2_CMD	CPU.SD2_CMD	F19				
J2.71	SD2_CLK	CPU.SD2_CLK	C21				
J2.73	DGND	DGND	-				
J2.75	SD1_DAT0	CPU.SD1_DAT0	A21	NVCC_			
J2.77	SD1_DAT1	CPU.SD1_DAT1	C20	NVCC_			
J2.79	SD1_DAT2	CPU.SD1_DAT2	E19	NVCC_			
J2.81	SD1_DAT3	CPU.SD1_DAT3	F18	NVCC_			
J2.83	SD1_CMD	CPU.SD1_CMD	B21	NVCC_			
J2.85	SD1_CLK	CPU.SD1_CLK	D20	NVCC_			
J2.87	DGND	DGND	-				
J2.89	KEY_COL0/ECSPI1_SCLK	CPU.KEY_COL0	W5				Not available as ECSPI1 signals on AXEL LITE's models which mount the NOR SPI flash. For further details, please refer to section 3.3.
J2.91	KEY_ROW0/ECSPI1_MOSI	CPU.KEY_ROW0	V6				
J2.93	KEY_COL1/ECSPI1_MISO	CPU.KEY_COL1	U7				
J2.95	KEY_ROW1/ECSPI1_SS0	CPU.KEY_ROW1	U6				
J2.97	KEY_COL2/ECSPI1_SS1	CPU.KEY_COL2	W6				
J2.99	KEY_ROW2	CPU.KEY_ROW2	W4				
J2.101	KEY_COL3/I2C2_SCL	CPU.KEY_COL3	U5				Used internally. Please refer to 7.8.2.
J2.103	KEY_ROW3/I2C2_SDA	CPU.KEY_ROW3	T7				Used internally. Please refer to 7.8.2.
J2.105	KEY_COL4	CPU.KEY_COL4	T6				
J2.107	KEY_ROW4	CPU.KEY_ROW4	V5				
J2.109	DGND	DGND	-				
J2.111	HDMI_CLKN	CPU.HDMI_CLKN	J5				
J2.113	HDMI_CLKP	CPU.HDMI_CLKP	J6				
J2.115	HDMI_D0N	CPU.HDMI_D0N	K5				

J2 – ODD [1-203]							
Pin	**Pin Name**	**Internal Connections**	**Ball/ pin #**	**Supply Group**	**Type**	**Voltage**	**Note**
J2.117	HDMI_D0P	CPU.HDMI_D0P	K6				
J2.119	HDMI_D1N	CPU.HDMI_D1N	J3				
J2.121	HDMI_D1P	CPU.HDMI_D1P	J4				
J2.123	HDMI_D2N	CPU.HDMI_D2N	K3				
J2.125	HDMI_D2P	CPU.HDMI_D2P	K4				
J2.127	HDMI_CEC_IN	CPU.HDMI_DDCCEC	K2				
J2.129	HDMI_HPD	CPU.HDMI_HPD	K1				
J2.131	DGND	DGND	-				
J2.133	LVDS0_CLK_N	CPU.LVDS0_CLK_N	V4				
J2.135	LVDS0_CLK_P	CPU.LVDS0_CLK_P	V3				
J2.137	LVDS0_TX0_N	CPU.LVDS0_TX0_N	U2				
J2.139	LVDS0_TX0_P	CPU.LVDS0_TX0_P	U1				
J2.141	LVDS0_TX1_N	CPU.LVDS0_TX1_N	U4				
J2.143	LVDS0_TX1_P	CPU.LVDS0_TX1_P	U3				
J2.145	LVDS0_TX2_N	CPU.LVDS0_TX2_N	V2				
J2.147	LVDS0_TX2_P	CPU.LVDS0_TX2_P	V1				
J2.149	LVDS0_TX3_N	CPU.LVDS0_TX3_N	W2				
J2.151	LVDS0_TX3_P	CPU.LVDS0_TX3_P	W1				
J2.153	DGND	DGND	-				
J2.155	LVDS1_CLK_N	CPU.LVDS1_CLK_N	Y3				
J2.157	LVDS1_CLK_P	CPU.LVDS1_CLK_P	Y4				
J2.159	LVDS1_TX0_N	CPU.LVDS1_TX0_N	Y1				
J2.161	LVDS1_TX0_P	CPU.LVDS1_TX0_P	Y2				
J2.163	LVDS1_TX1_N	CPU.LVDS1_TX1_N	AA2				
J2.165	LVDS1_TX1_P	CPU.LVDS1_TX1_P	AA1				
J2.167	LVDS1_TX2_N	CPU.LVDS1_TX2_N	AB1				
J2.169	LVDS1_TX2_P	CPU.LVDS1_TX2_P	AB2				
J2.171	LVDS1_TX3_N	CPU.LVDS1_TX3_N	AA3				

J2 – ODD [1-203]							
Pin	**Pin Name**	**Internal Connections**	**Ball/ pin #**	**Supply Group**	**Type**	**Voltage**	**Note**
J2.173	LVDS1_TX3_P	CPU.LVDS1_TX3_P	AA4				
J2.175	DGND	DGND	-				
J2.177	EIM_D19	CPU.EIM_D19	G21				
J2.179	EIM_D20	CPU.EIM_D20	G20				
J2.181	EIM_D21	CPU.EIM_D21	H20				
J2.183	EIM_D22	CPU.EIM_D22	E23				
J2.185	EIM_D23	CPU.EIM_D23	D25				
J2.187	EIM_D24	CPU.EIM_D24	F22				
J2.189	EIM_D25	CPU.EIM_D25	G22				
J2.191	EIM_D26	CPU.EIM_D26	E24				
J2.193	EIM_D27	CPU.EIM_D27	E25				
J2.195	EIM_D28	CPU.EIM_D28	G23				
J2.197	EIM_D29	CPU.EIM_D29	J19				
J2.199	EIM_D30	CPU.EIM_D30	J20				
J2.201	EIM_D31	CPU.EIM_D31	H21				
J2.203	DGND	DGND	-				

J2 – EVEN [2-204]							
Pin	**Pin Name**	**Internal Connections**	**Ball/ pin #**	**Supply Group**	**Type**	**Voltage**	**Note**
J2.2	DGND	DGND	-				
J2.4	3.3VIN	INPUT VOLTAGE					
J2.6	3.3VIN	INPUT VOLTAGE					
J2.8	3.3VIN	INPUT VOLTAGE					
J2.10	3.3VIN	INPUT VOLTAGE					

J2 – EVEN [2-204]							
Pin	**Pin Name**	**Internal Connections**	**Ball/ pin #**	**Supply Group**	**Type**	**Voltage**	**Note**
J2.12	DGND	DGND	-				
J2.14	PMIC_LICELL	PMIC.LICELL	42				
J2.16	CPU_ONOFF	CPU.CPU_ONOFF	D12				
J2.18	BOARD_PGOOD		-				
J2.20	BOOT_MODE_SEL	BOOT MODE SELECTION	-				
J2.22	CPU_PORN	CPU.CPU_PORN	C11				
J2.24	PMIC_PWRON	PMIC.PWRON	56				
J2.26	GPIO_0	CPU.GPIO_0	T5				
J2.28	GPIO_1	CPU.GPIO_1	T4				
J2.30	DGND	DGND	-				
J2.32	GPIO_2	CPU.GPIO_2	T1				
J2.34	GPIO_3/I2C3_SCL	CPU.GPIO_3	R7				
J2.36	GPIO_4	CPU.GPIO_4	R6				
J2.38	GPIO_5	CPU.GPIO_5	R4				
J2.40	GPIO_6/I2C3_SDA	CPU.GPIO_6	T3				
J2.42	GPIO_7//FLEXCAN1_H	CPU.GPIO_7	R3				Mount option. Please refer to section 7.9.1.
J2.44	GPIO_8//FLEXCAN1_L	CPU.GPIO_8	R5				Mount option. Please refer to section 7.9.1.
J2.46	GPIO_9	CPU.GPIO_9	T2				
J2.48	GPIO_16	CPU.GPIO_16	R2				
J2.50	GPIO_17	CPU.GPIO_17	R1				
J2.52	GPIO_18	CPU.GPIO_18	P6				
J2.54	GPIO_19	CPU.GPIO_19	P5				
J2.56	DGND	DGND	-				
J2.58	CSI0_PIXCLK	CPU.CSI0_PIXCLK	P1				
J2.60	CSI0_MCLK	CPU.CSI0_MCLK	P4				
J2.62	CSI0_VSYNC	CPU.CSI0_VSYNC	N2				
J2.64	CSI0_DATA_EN	CPU.CSI0_DATA_EN	P3				
J2.66	CSI0_DAT4	CPU.CSI0_DAT4	N1				
J2.68	CSI0_DAT5	CPU.CSI0_DAT5	P2				
J2.70	CSI0_DAT6	CPU.CSI0_DAT6	N4				
J2.72	CSI0_DAT7	CPU.CSI0_DAT7	N3				
J2.74	CSI0_DAT8	CPU.CSI0_DAT8	N6				

J2 – EVEN [2-204]							
Pin	**Pin Name**	**Internal Connections**	**Ball/ pin #**	**Supply Group**	**Type**	**Voltage**	**Note**
J2.76	CSI0_DAT9	CPU.CSI0_DAT9	N5				
J2.78	CSI0_DAT10	CPU.CSI0_DAT10	M1				
J2.80	CSI0_DAT11	CPU.CSI0_DAT11	M3				
J2.82	DGND	DGND	-				
J2.84	CLK1_N	CPU.CLK1_N	C7				
J2.86	CLK1_P	CPU.CLK1_P	D7				
J2.88	CLK2_N	CPU.CLK2_N	C5				
J2.90	CLK2_P	CPU.CLK2_P	D5				
J2.92	PCIE_RXN	CPU.PCIE_RXN	B1				
J2.94	PCIE_RXP	CPU.PCIE_RXP	B2				
J2.96	PCIE_TXN	CPU.PCIE_TXN	A3				
J2.98	PCIE_TXP	CPU.PCIE_TXP	B3				
J2.100	DGND	DGND	-				
J2.102	CSI_CLK0M	CPU.CSI_CLK0M	F4				
J2.104	CSI_CLK0P	CPU.CSI_CLK0P	F3				
J2.106	CSI_D0M	CPU.CSI_D0M	E4				
J2.108	CSI_D0P	CPU.CSI_D0P	E3				
J2.110	CSI_D1M	CPU.CSI_D1M	D1				
J2.112	CSI_D1P	CPU.CSI_D1P	D2				
J2.114	CSI_D2M	CPU.CSI_D2M	E1				
J2.116	CSI_D2P	CPU.CSI_D2P	E2				
J2.118	CSI_D3M	CPU.CSI_D3M	F2				
J2.120	CSI_D3P	CPU.CSI_D3P	F1				
J2.122	DGND	DGND	-				
J2.124	DI0_PIN15	CPU.DI0_PIN15	N21	NVCC_			
J2.126	DI0_PIN4	CPU.DI0_PIN4	P25	NVCC_			
J2.128	DI0_PIN3	CPU.DI0_PIN3	N20	NVCC_			
J2.130	DI0_PIN2	CPU.DI0_PIN2	N25	NVCC_			
J2.132	DI0_DISP_CLK	CPU.DI0_DISP_CLK	N19	NVCC_			
J2.134	DISP0_DAT0	CPU.DISP0_DAT0	P24	NVCC_			
J2.136	DISP0_DAT1	CPU.DISP0_DAT1	P22	NVCC_			
J2.138	DISP0_DAT2	CPU.DISP0_DAT2	P23	NVCC_			

J2 – EVEN [2-204]							
Pin	**Pin Name**	**Internal Connections**	**Ball/ pin #**	**Supply Group**	**Type**	**Voltage**	**Note**
J2.140	DISP0_DAT3	CPU.DISP0_DAT3	P21	NVCC_			
J2.142	DISP0_DAT4	CPU.DISP0_DAT4	P20	NVCC_			
J2.144	DISP0_DAT5	CPU.DISP0_DAT5	R25	NVCC_			
J2.146	DGND	DGND	-				
J2.148	DISP0_DAT6	CPU.DISP0_DAT6	R23	NVCC_			
J2.150	DISP0_DAT7	CPU.DISP0_DAT7	R24	NVCC_			
J2.152	DISP0_DAT8	CPU.DISP0_DAT8	R22	NVCC_			
J2.154	DISP0_DAT9	CPU.DISP0_DAT9	T25	NVCC_			
J2.156	DISP0_DAT10	CPU.DISP0_DAT10	R21	NVCC_			
J2.158	DISP0_DAT11	CPU.DISP0_DAT11	T23	NVCC_			
J2.160	DISP0_DAT12	CPU.DISP0_DAT12	T24	NVCC_			
J2.162	DISP0_DAT13	CPU.DISP0_DAT13	R20	NVCC_			
J2.164	DGND	DGND	-				
J2.166	DISP0_DAT14	CPU.DISP0_DAT14	U25	NVCC_			
J2.168	DISP0_DAT15	CPU.DISP0_DAT15	T22	NVCC_			
J2.170	DISP0_DAT16	CPU.DISP0_DAT16	T21	NVCC_			
J2.172	DISP0_DAT17	CPU.DISP0_DAT17	U24	NVCC_			
J2.174	DISP0_DAT18	CPU.DISP0_DAT18	V25	NVCC_			
J2.176	DISP0_DAT19	CPU.DISP0_DAT19	U23	NVCC_			
J2.178	DISP0_DAT20	CPU.DISP0_DAT20	U22	NVCC_			
J2.180	DISP0_DAT21	CPU.DISP0_DAT21	T20	NVCC_			
J2.182	DISP0_DAT22	CPU.DISP0_DAT22	V24	NVCC_			
J2.184	DISP0_DAT23	CPU.DISP0_DAT23	W24	NVCC_			
J2.186	USB_OTG_VBUS	CPU.USB_OTG_VBUS	E9	NVCC_			
J2.188	USB_H1_VBUS	CPU.USB_H1_VBUS	D10	NVCC_			
J2.190	DGND	DGND	-				
J2.192	ENET_RX_ER	CPU.ENET_RX_ER	W23				
J2.194	ENET_RXD0	CPU.ENET_RXD0	W21				
J2.196	USB_OTG_DN	CPU.USB_OTG_DN	B6	NVCC_			
J2.198	USB_OTG_DP	CPU.USB_OTG_DP	A6	NVCC_			
J2.200	USB_HOST_DP	CPU.USB_HOST_DP	E10	NVCC_			
J2.202	USB_HOST_DN	CPU.USB_HOST_DN	F10	NVCC_			

J2 – EVEN [2-204]							
Pin	**Pin Name**	**Internal Connections**	**Ball/ pin #**	**Supply Group**	**Type**	**Voltage**	**Note**
J2.204	DGND	DGND	-				

7 Peripheral interfaces

AXEL LITE modules implement a number of peripheral interfaces through the SO-DIMM connector. The following notes apply to those interfaces:

- Some interfaces/signals are available only with/without certain configuration options of the **AXEL LITE** module. Each signal's availability is noted in the "Notes" column on the table of each interface.

- The peripherals described in the following sections represent the default configuration for the **AXEL LITE** SOM, which match with the features provided by the electronics implemented on the module.

The signals for each interface are described in the related tables. The following notes summarize the column headers for these tables:

- "Pin name" – The symbolic name of each signal
- "Conn. Pin" – The pin number on the module connectors
- "Function" – Signal description
- "Notes" – This column summarizes configuration requirements and recommendations for each signal.

7.1 Notes on pin assignment

For further information, please refer to section 5.6 "Multiplexing".

7.2 Gigabit Ethernet

On-board Ethernet PHY (Micrel KSZ9031RNX) provides interface signals required to implement the 10/100/1000 Mbps Ethernet port. The transceiver is connected to the triple speed Ethernet MAC (ENET module) through RGMII interface.

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
ETH0_TXRX0_P	J2.19	Media Dependent Interface[0], positive pin	

Pin name	Conn. Pin	Function	Notes
ETH0_TXRX0_M	J2.21	Media Dependent Interface[0], negative pin	
ETH0_TXRX1_P	J2.23	Media Dependent Interface[1], positive pin	
ETH0_TXRX1_M	J2.25	Media Dependent Interface[1], negative pin	
ETH0_TXRX2_P	J2.27	Media Dependent Interface[2], positive pin	
ETH0_TXRX2_M	J2.29	Media Dependent Interface[2], negative pin	
ETH0_TXRX3_P	J2.31	Media Dependent Interface[3], positive pin	
ETH0_TXRX3_M	J2.33	Media Dependent Interface[3], negative pin	
ETH0_LED1	J2.13	Activity LED	
ETH0_LED2	J2.15	Link LED	

7.3 USB

AXEL LITE provides two USB ports with integrated PHY, one USB Host 2.0 (High Speed, up to 480 Mbps) and one USB 2.0 On-The-Go (OTG).

7.3.1 USB Host

Pin name	Conn. Pin	Function	Notes
USB_HOST_DP	J2.200	D+ pin of the USB cable	
USB_HOST_DN	J2.202	D- pin of the USB cable	
USB_H1_VBUS	J2.188	VBUS pin of the USB cable	

7.3.2 USB OTG

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
USB_OTG_DN	J2.196	D- pin of the USB cable	
USB_OTG_DP	J2.198	D+ pin of the USB cable	
USB_OTG_VBUS	J2.186	VBUS pin of the USB cable	
USB_OTG_ID	J2.28	USB OTG ID	

7.4 Video Output ports

i.MX6 implements two (identical) Image Processing Units (IPUs), which provide connectivity to displays and related processing, synchronization and control. Each IPU has two display ports - each controlled by a DI module - providing a connection to displays and external devices, either directly (parallel interface) or via bridges (MIPI, LVDS, HDMI). Each IPU has 2 display ports, up to four external ports can be active at any given time. (Additional asynchronous data flows can be sent though the parallel ports and the MIPI/DSI port.). The following is a list of the available interfaces:

- One parallel port, driven by first IPU
- Two LVDS channels, driven by the LDB
- One HDMI port (ver. 1.4), driven by the HDMI transmitter
- One MIPI/DSI port, driven by the MIPI/DSI transmitter; 2 data lanes at 1 GHz

Each IPU display port (DI) can be connected to each of the above ports.

7.4.1 LVDS

The LVDS Display Bridge (LDB) connects the IPU (Image Processing Unit) to an External LVDS Display Interface. There are 2 LVDS channels. These outputs are used to communicate RGB data and controls to external LCD displays.

The LVDS ports may be used as follows:

- Single channel output
- Dual channel output (one input source, two channels outputs for two

displays)

- Split channel output (one input source, split to 2 channels on output)
- Separate 2 channel output (2 input sources from IPU).

The output LVDS port complies to the EIA-644-A standard.

7.4.1.1 LVDS0

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
LVDS0_TX0_N	J2.137	LVDS0 negative data 0 signal	
LVDS0_TX0_P	J2.139	LVDS0 positive data 0 signal	
LVDS0_TX1_N	J2.141	LVDS0 negative data 1 signal	
LVDS0_TX1_P	J2.143	LVDS0 positive data 1 signal	
LVDS0_TX2_N	J2.145	LVDS0 negative data 2 signal	
LVDS0_TX2_P	J2.147	LVDS0 positive data 2 signal	
LVDS0_TX3_N	J2.149	LVDS0 negative data 3 signal	
LVDS0_TX3_P	J2.151	LVDS0 positive data 3 signal	
LVDS0_CLK_N	J2.133	LVDS0 negative clock signal	
LVDS0_CLK_P	J2.135	LVDS0 positive clock signal	

7.4.1.2 LVDS1

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
LVDS1_TX0_N	J2.159	LVDS1 negative data 0	

Pin name	Conn. Pin	Function	Notes
		signal	
LVDS1_TX0_P	J2.161	LVDS1 positive data 0 signal	
LVDS1_TX1_N	J2.163	LVDS1 negative data 1 signal	
LVDS1_TX1_P	J2.165	LVDS1 positive data 1 signal	
LVDS1_TX2_N	J2.167	LVDS1 negative data 2 signal	
LVDS1_TX2_P	J2.169	LVDS1 positive data 2 signal	
LVDS1_TX3_N	J2.171	LVDS1 negative data 3 signal	
LVDS1_TX3_P	J2.173	LVDS1 positive data 3 signal	
LVDS1_CLK_N	J2.155	LVDS1 negative clock signal	
LVDS1_CLK_P	J2.157	LVDS1 positive clock signal	

7.4.2 HDMI

The HDMI interface available on **AXEL LITE** is based on the HDMI transmitter and the HDMI 3D Tx PHY integrated into the i.MX6 SoC. The HDMI port supports the following standards and features:

- High-Definition Multimedia Interface Specification, Version 1.4a
- Support for up to 1080p at 60Hz HDTV display resolutions and up to QXGA graphic display resolutions.
- Support for 4k x 2k and 3D video formats
- Support for up to 16-bit Deep Color modes

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
HDMI_CLK_N	J2.111	HDMI negative clock	

Pin name	Conn. Pin	Function	Notes
		signal	
HDMI_CLK_P	J2.113	HDMI positive clock signal	
HDMI_D0_N	J2.115	HDMI negative data 0	
HDMI_D0_P	J2.117	HDMI positive data 0	
HDMI_D1_N	J2.119	HDMI negative data 1	
HDMI_D1_P	J2.121	HDMI positive data 1	
HDMI_D2_N	J2.123	HDMI negative data 2	
HDMI_D2_P	J2.125	HDMI positive data 2	
HDMI_CEC	J2.127	HDMI CEC signal	
HDMI_DDC_SCL	J2.101	HDMI I2C clock signal	
HDMI_DDC_SDA	J2.103	HDMI I2C data signal	
HDMI_HPD	J2.129	HDMI HPD signal	

7.4.3 Parallel RGB

The Parallel Display interface provided by **AXEL LITE** is derived directly from the DI0 port of the IPU, bypassing all the i.MX6 integrated display bridges.

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
DI0_DISP_CLK	J2.132	Pixel clock	
DI0_PIN2	J2.130	Horizontal synchronization	
DI0_PIN3	J2.128	Vertical synchronization	
DI0_PIN15	J2.124	Data valid/blank, data enable	
DISP0_DAT0	J2.134	Pixel data bit 0	
DISP0_DAT1	J2.136	Pixel data bit 1	
DISP0_DAT2	J2.138	Pixel data bit 2	
DISP0_DAT3	J2.140	Pixel data bit 3	
DISP0_DAT4	J2.142	Pixel data bit 4	

Pin name	Conn. Pin	Function	Notes
DISP0_DAT5	J2.144	Pixel data bit 5	
DISP0_DAT6	J2.148	Pixel data bit 6	
DISP0_DAT7	J2.150	Pixel data bit 7	
DISP0_DAT8	J2.152	Pixel data bit 8	
DISP0_DAT9	J2.154	Pixel data bit 9	
DISP0_DAT10	J2.156	Pixel data bit 10	
DISP0_DAT11	J2.158	Pixel data bit 11	
DISP0_DAT12	J2.160	Pixel data bit 12	
DISP0_DAT13	J2.162	Pixel data bit 13	
DISP0_DAT14	J2.166	Pixel data bit 14	
DISP0_DAT15	J2.168	Pixel data bit 15	
DISP0_DAT16	J2.170	Pixel data bit 16	
DISP0_DAT17	J2.172	Pixel data bit 17	
DISP0_DAT18	J2.174	Pixel data bit 18	
DISP0_DAT19	J2.176	Pixel data bit 19	
DISP0_DAT20	J2.178	Pixel data bit 20	
DISP0_DAT21	J2.180	Pixel data bit 21	
DISP0_DAT22	J2.182	Pixel data bit 22	
DISP0_DAT23	J2.184	Pixel data bit 23	

7.5 Video Input ports

This section will be completed in a future version of this manual.

7.5.1 Parallel RGB

This section will be completed in a future version of this manual.

7.5.2 MIPI CSI

This section will be completed in a future version of this manual.

7.6 UARTs

Five UART ports are routed to **AXEL LITE** connectors. UART1 provides

full Modem Control Signals, while UART2, UART3, and UART5 are 4-wire interfaces. UART4 is a 2-wire interface. Each port can be programmed separately (also in IrDA mode).

7.6.1 UART1

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Note
UART1_CTS	J2.177 J2.39	Clear to send	
UART1_DCD	J2.185	Data carrier detected	
UART1_DSR	J2.193	Data set ready	
UART1_DTR	J2.187	Data terminal ready	
UART1_RI	-	Ring indicator	A GPIO should be used for this purposes
UART1_RTS	J2.179 J2.41	Request to send	
UART1_RX_DATA	J2.80 J2.51	Serial/infrared data receive	
UART1_TX_DATA	J2.78 J2.53	Serial/infrared data transmit	

7.6.2 UART2

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
UART2_CTS	J2.195 J2.55	Clear to send	
UART2_RTS	J2.197 J2.59	Request to send	
UART2_RX_DATA	J2.193 J2.44 J2.47	Serial/infrared data receive	
UART2_TX_DATA	J2.191 J2.42 J2.49	Serial/infrared data transmit	

7.6.3 UART3

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
UART3_CTS	J2.185 J2.199 J2.45	Clear to send	
UART3_RTS	J2.201 J2.37	Request to send	
UART3_RX_DATA	J2.189	Serial/infrared data receive	
UART3_TX_DATA	J2.187	Serial/infrared data transmit	

7.6.4 UART4

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
UART4_RX_DATA	J2.91	Serial/infrared data receive	
UART4_TX_DATA	J2.89	Serial/infrared data transmit	

7.6.5 UART5

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
UART5_CTS	J2.107	Clear to send	
UART5_RTS	J2.105	Request to send	
UART5_RX_DATA	J2.95	Serial/infrared data receive	
UART5_TX_DATA	J2.93	Serial/infrared data transmit	

7.7 SPI

AXEL LITE provides up to five SPI ports connected to the I.MX6 integrated Enhanced Configurable SPI (ECSPI) controller, featuring:

- Full-duplex synchronous serial interface
- Master/Slave configurable
- Up to four Chip Select (SS) signals to support multiple peripherals
- Transfer continuation function allows unlimited length data transfers
- 32-bit wide by 64-entry FIFO for both transmit and receive data
- Configurable Polarity and phase of the Chip Select (SS) and SPI Clock (SCLK)
- Direct Memory Access (DMA) support

7.7.1 ECSPI1

AXEL LITE on-board bootable SPI Flash is interfaced with the i.MX6 SoC through the eCSPI1 port on chip select 0. For further details, please refer to Section 3.3.

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
ECSPI1_MISO	J2.93 J2.70 J2.182	Master data in; slave data out	
ECSPI1_MOSI	J2.91 J2.68 J2.180	Master data out; slave data in	
ECSPI1_RDY	J2.54	Data ready signal	
ECSPI1_SCLK	J2.89 J2.66 J2.178	Clock signal	
ECSPI1_SS0	J2.95 J2.72 J2.184	Chip select 0 signal	
ECSPI1_SS1	J2.97	Chip select 1 signal	

Pin name	Conn. Pin	Function	Notes
	J2.168 J2.177		
ECSPI1_SS2	J2.99 J2.187	Chip select 2 signal	
ECSPI1_SS3	J2.101 J2.189	Chip select 3 signal	

7.7.2 ECSPI2

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
ECSPI2_MISO	J2.78 J2.172	Master data in; slave data out	
ECSPI2_MOSI	J2.76 J2.170	Master data out; slave data in	
ECSPI2_SCLK	J2.74 J2.176	Clock signal	
ECSPI2_SS0	J2.80 J2.174	Chip select 0 signal	
ECSPI2_SS1	J2.168	Chip select 1 signal	
ECSPI2_SS2	J2.187	Chip select 2 signal	
ECSPI2_SS3	J2.189	Chip select 3 signal	

7.7.3 ECSPI3

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
ECSPI3_MISO	J2.138	Master data in; slave data out	
ECSPI3_MOSI	J2.136	Master data out; slave data in	
ECSPI3_RDY	J2.150	Data ready signal	
ECSPI3_SCLK	J2.134	Clock signal	
ECSPI3_SS0	J2.140	Chip select 0 signal	

Pin name	Conn. Pin	Function	Notes
ECSPI3_SS1	J2.142	Chip select 1 signal	
ECSPI3_SS2	J2.144	Chip select 2 signal	
ECSPI3_SS3	J2.148	Chip select 3 signal	

7.7.4 ECSPI4

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
ECSPI4_MISO	J2.183	Master data in; slave data out	
ECSPI4_MOSI	J2.195	Master data out; slave data in	
ECSPI4_SCLK	J2.181	Clock signal	
ECSPI4_SS0	J2.179 J2.197	Chip select 0 signal	
ECSPI4_SS1	-	Chip select 1 signal	Not available
ECSPI4_SS2	J2.187	Chip select 2 signal	
ECSPI4_SS3	J2.189	Chip select 3 signal	

7.7.5 ECSPI5

ECSPI5 is not available on the **AXEL LITE** models that mount the i.MX6 Solo SOC.

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
ECSPI5_MISO	J2.75 J2.61	Master data in; slave data out	
ECSPI5_MOSI	J2.83 J2.69	Master data out; slave data in	
ECSPI5_RDY	J2.42	Data ready signal	
ECSPI5_SCLK	J2.85 J2.71	Clock signal	
ECSPI5_SS0	J2.77	Chip select 0 signal	

Pin name	Conn. Pin	Function	Notes
	J2.63		
ECSPI5_SS1	J2.79 J2.65	Chip select 1 signal	
ECSPI5_SS2	J2.81	Chip select 2 signal	
ECSPI5_SS3	J2.67	Chip select 3 signal	

7.8 I²C

Three I²C channels are available on **AXEL LITE** to provide an interface to other devices compliant with Philips Semiconductors Inter-IC bus (I2C-bus™) specification version 2.1. The I²C ports support standard mode (up to 100K bits/s) and fast mode (up to 400K bits/s).

7.8.1 I²C1

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
I2C1_SCL	J2.76 J2.181	I2C clock	
I2C1_SDA	J2.74 J2.195	I2C data	

7.8.2 I²C2

The I²C2 bus is used for connecting the i.MX6 SOC to the PMIC. The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
I2C2_SCL	J2.101	I2C clock	
I2C2_SDA	J2.103	I2C data	

7.8.3 I²C3

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
I2C3_SCL	J2.34 J2.38	I2C clock	
I2C3_SDA	J2.40 J2.48	I2C data	

7.9 CAN

AXEL LITE provides two CAN interfaces (FLEXCAN1 and FLEXCAN2) for supporting distributed realtime control with a high level of reliability. The FLEXCAN module implements the CAN protocol version 2.0 part B and supports bit rates up to 1 Mbit/s.

7.9.1 FLEXCAN1

FLEXCAN1 port is connected to on-board transceiver (TI SN65HVD232) which converts the single-ended CAN signals of the controller to the differential signals of the physical layer. When required, the on-board transceiver can be excluded by dedicated mount options. Please contact our Sales Department for more information about this hardware option.

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
CAN_H	J2.42	High bus output	
CAN_L	J2.44	Low bus output	

The following table describes FLEXCAN1 interface signals:

Pin name	Conn. Pin	Function	Notes
FLEXCAN1_RX	J2.44 J2.99 J2.59	Receive data pin	
FLEXCAN1_TX	J2.42 J2.97 J2.55	Transmit data pin	

7.9.2 FLEXCAN2

When required, FLEXCAN2 must be connected to an external PHY on the carrier board.

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
FLEXCAN2_RX	J2.107 J2.41	Receive data pin	
FLEXCAN2_TX	J2.105 J2.39	Transmit data pin	

7.10 JTAG

The i.MX6 provides debug access via a standard JTAG (IEEE 1149.1) debug interface. The signals are routed to the on-board J7 connector. The connector is placed on the top side of the PCB, at the upper-right corner (please see the picture below).

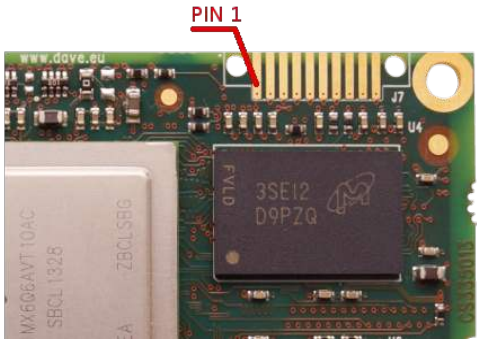


Fig. 6: On board JTAG connector J7

J7 footprint mates with Samtec FSI-110-03-G-S connector. The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
JTAG_TDO	J7.4	JTAG TDO	On board connector
JTAG_TDI	J7.5	JTAG TDI	On board connector

Pin name	Conn. Pin	Function	Notes
JTAG_TMS	J7.3	JTAG TMS	On board connector
JTAG_TCK	J7.2	JTAG clock	On board connector
JTAG_VREF	J7.10	JTAG VREF	On board connector
JTAG_nTRST	J7.6	JTAG TRST	On board connector
DGND	J7.1	Ground	On board connector
CPU_PORn	J7.7	Please refer to Section 5.2.1.	

J7.8 and J7.9 pin are not connected.

7.11 SD/SDIO/MMC

The processor provides 4 MMC/SD/SDIO ports through the Ultra Secured Digital Host Controller (USDHC), compliant with MMC V4.41, Secure Digital Memory Card Specification V3.00 and Secure Digital Input Output (SDIO) V3.00 specifications. The controller supports 1-bit / 4-bit SD and SDIO modes, 1-bit / 4-bit / 8-bit MMC modes. High capacity SD cards (SDHC) are supported.

Three MMC/SD/SDIO interfaces are available on **AXEL LITE** SOM.

7.11.1 MMC/SD/SDIO1

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
SD1_CD	J2.28	Card detection pin	If not used(for the embedded memory),tie low to indicate there is a card attached.
SD1_CLK	J2.85	Clock for MMC/SD/SDIO card	
SD1_CMD	J2.83	CMD line	
SD1_DATA0	J2.75	DATA0 line in all modes	Also used to detect busy state
SD1_DATA1	J2.77	DATA1 line in 4/8-bit mode	Also used to detect interrupt in 1/4-bit mode

Pin name	Conn. Pin	Function	Notes
SD1_DATA2	J2.79	DATA2 line or Read Wait in 4-bit mode	Read Wait in 1-bit mode
SD1_DATA3	J2.81	DATA3 line in 4/8-bit mode or configured as card detection pin	May be configured as card detection pin in 1-bit mode
SD1_LCTL	J2.48	LED control used to drive an external LED Active high	Fully controlled by the driver Optional output
SD1_VSELECT	J2.93 J2.101	IO power voltage selection signal	
SD1_WP	J2.126 J2.46	Card write protect detect	If not used(for the embedded memory), tie low to indicate it's not write protected.

7.11.2 MMC/SD/SDIO2

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
SD2_CD	J2.36	Card detection pin	If not used(for the embedded memory),tie low to indicate there is a card attached.
SD2_CLK	J2.71	Clock for MMC/SD/SDIO card	
SD2_CMD	J2.69	CMD line	
SD2_DATA0	J2.61	DATA0 line in all modes	Also used to detect busy state
SD2_DATA1	J2.63	DATA1 line in 4/8-bit mode	Also used to detect interrupt in 1/4-bit mode
SD2_DATA2	J2.65	DATA2 line or Read Wait in 4-bit mode	Read Wait in 1-bit mode

Pin name	Conn. Pin	Function	Notes
SD2_DATA3	J2.67	DATA3 line in 4/8-bit mode or configured as card detection pin	May be configured as card detection pin in 1-bit mode
SD2_LCTL	J2.40	LED control used to drive an external LED Active high	Fully controlled by the driver Optional output
SD2_VSELECT	J2.95 J2.99	IO power voltage selection signal	
SD2_WP	J2.32	Card write protect detect	If not used(for the embedded memory), tie low to indicate it's not write protected.

7.11.3 MMC/SD/SDIO3

The following table describes the interface signals:

Pin name	Conn. Pin	Function	Notes
SD3_CLK	J2.59	Clock for MMC/SD/SDIO card	
SD3_CMD	J2.55	CMD line	
SD3_DATA0	J2.39	DATA0 line in all modes	Also used to detect busy state
SD3_DATA1	J2.41	DATA1 line in 4/8-bit mode	Also used to detect interrupt in 1/4-bit mode
SD3_DATA2	J2.43	DATA2 line or Read Wait in 4-bit mode	Read Wait in 1-bit mode
SD3_DATA3	J2.45	DATA3 line in 4/8-bit mode or configured as card detection pin	May be configured as card detection pin in 1-bit mode
SD3_DATA4	J2.47	DATA4 line in 8-bit mode, not used in other modes	

Pin name	Conn. Pin	Function	Notes
SD3_DATA5	J2.49	DATA5 line in 8-bit mode, not used in other modes	
SD3_DATA6	J2.51	DATA6 line in 8-bit mode, not used in other modes	
SD3_DATA7	J2.53	DATA7 line in 8-bit mode, not used in other modes	
SD3_RST	J2.37	Card hardware reset signal, active LOW	
SD3_VSELECT	J2.52	IO power voltage selection signal	

7.12 PCI Express

The SOM supports connections to PCIe-compliant devices via the integrated PCIe master/slave bus interface. The i.MX6 integrated PCIe module implements a single one-lane PCIe 2.0 (5.0 GT/s) Dual Mode/Endpoint/Root Complex port.

The following table describes the interface signals:

Connector Pin	Pin name	Function	Notes
PCIE_TXN	J2.96	PCIE Transmit Data Lane 0	
PCIE_TXP	J2.98		
PCIE_RXN	J2.92	PCIE Receive Data Lane 0.	
PCIE_RXP	J2.94		

7.13 Audio interface

This section will be completed in a future version of this manual.

7.14 Keypad

This section will be completed in a future version of this manual.

7.15 GPIO

The i.MX6 GPIO module provides general-purpose pins that can be configured as either inputs or outputs, for connections to external devices. In addition, the GPIO peripheral can produce CORE interrupts. The device contains eight GPIO blocks and each GPIO block is made up of 32 identical channels.

The device GPIO peripheral supports up to 256 3.3-V GPIO pins. Each channel must be properly configured, since GPIO signals are multiplexed with other interfaces signals. For more information on how to configure and use GPIOs, please refer to section 5.6. For additional details, please refer to section 27 of the i.MX 6 APRM.

8 Operational characteristics

8.1 Maximum ratings

This section will be completed in a future version of this manual.

Parameter	Min	Typ	Max	Unit
Main power supply voltage		3.3		V

8.2 Recommended ratings

This section will be completed in a future version of this manual.

Parameter	Min	Typ	Max	Unit
Main power supply voltage		3.3		V

8.3 Power consumption

Providing theoretical maximum power consumption value would be useless for the majority of system designers building their application upon **AXEL LITE** module because, in most cases, this would lead to an over-sized power supply unit.
Several configurations have been tested in order to provide figures that are measured on real-world use cases instead. Please note that **AXEL LITE** platform is so flexible that it is virtually impossible to test for all possible configurations and applications on the market. The use cases here presented should cover most of real-world scenarios. However actual customer application might require more power than values reported here. Generally speaking, application specific requirements have to be taken into consideration in order to size power supply unit and to implement thermal management properly.

8.3.1 Set 1

This section will be completed in a future version of this manual.

8.3.2 Set 2

This section will be completed in a future version of this manual.

8.4 Heat Dissipation

Qualification of the microprocessors has been deeply changed with respect to some years ago. Silicon manufactures today qualify ICs measuring the temperature at dye level, that is conceptually correct since we are dealing with silicon. On the other hand, users are loosing the straightforward relationship with the “ambient temperature”, that is the end- user parameter still popular and evaluated when they must choose a platform for their needs.

Therefore, a deep knowledge of the heat transfer mechanism from junction to environment is absolutely needed. Also, to know how to save power consumption and to dissipate heating is of primary importance.

Application Note AN4579[1] released by NXP is a fundamental guide in understanding thermal dissipation of iMX6 components.
We strongly recommend to read, understand, and follow all suggestions described in that guide.

AN4579 deals with the twofold aspects of the problem. The first aspect is related to the power saving strategy to be implemented. That are implemented in software on an hardware properly set.
DAVE Embedded Systems has implemented in the Linux BSP, and maintained in the time, many of the Software Thermal Management Techniques listed in the Application Notes. Check with your DAVE Embedded Systems' Technical Support which are currently maintained and which are the default settings.

Once power has been managed at best as mentioned above, heat dissipation is also to be managed. Starting from the standard consumption described in the “use cases” above [see also AN4576[2], AN4509[3] and AN4715[4] and http://wiki.dave.eu/index.php/Power_consumption_(AxelLite)] , using

1 AN4579: Thermal Management Guidelines
2 AN4576: i.MX6 Dual Lite Power Consumption Measurement
3 AN4509: i.MX6 Dual/Quad Power Consumption Measurement
4 AN4715: i.MX6 Solo Consumption Measurement

fundamental formula.

$$T_j = T_a + R_{ja} * P$$

and knowing that R_{ja} =22 °C/W for no-lid i.MX6 case, you can verify that natural convection with no heat sink make CPU working only around 20-25°C (see table 11) To lower R_{ja} - the only available parameter – you must use of a Axel Hardware Manual v.1.0.5 (passive) heatsink in such a way you can dissipate same power at a considerably high ambient temperature. If you add an air flow on the heatsink you can dissipate at an even higher temperature.
The following table shows an example, on how much power can be dissipated with T_j =105°C and T_a =25°C without heatsink/still air (a), with heatsink[5]/still air (b), with heatsink/air flow 1m/s (c), with heatsink/air flow 4m/s (d):

Use Case	T_j	T_a	R_{ja}	P [W]
a	105° C	25° C	22	3,64
b	105° C	25° C	12,9	6,20
c	105° C	25° C	6,9 (1m/s)	11,60
d	105° C	25° C	4,5 (4m/s)	17,78

Tab. 11: Power dissipation Vs.Thermal Resistance

The following table shows the T_a the system can work at, in the same “use case” when the CPU is supposed to consume 4W

Use Case	T_j	T_a	R_{ja}	P [W]
a	105° C	25° C	22	4
b	105° C	53° C	12,9	4
c	105° C	77° C	6,9 (1m/s)	4
d	105° C	87° C	4,5 (4m/s)	4

Tab. 12: Ambient Temperature Vs.Thermal Resistance

5 Heat Sink: AAVID 30x30x9,4mm

It is mandatory to understand that Thermal Management Techniques are under the responsability of the system integrator. Even if these notes try to help also with some quantitative suggestion, every solution must be validated by the System Integrator itself at the end of the integration process. That is due to the fact that too many parameters that are affecting simulations are not taken in account because it very difficult to modelize them. Therefore, even if customers may afford these kind of design, the simulation itself would be affected by huge uncertainty.

9 Application notes

Please refer to the following documents available on **DAVE Embedded Systems** Developers Wiki:

Document	Location
Integration Guide	http://wiki.dave.eu/index.php/Integration_guide_%28Axel%29
Carrier board design guidelines	http://wiki.dave.eu/index.php/Carrier_board_design_guidelines_%28SOM%29