19-2831; Rev 0; 4/03

EVALUATION KIT AVAILABLE

Complete Power IC for Low-Cost PDAs

General Description

The MAX1552 is a complete power-management chip for low-cost personal digital assistants (PDAs) and portable devices operating from a 1-cell lithium-ion (Li+), or 3-cell NiMH, battery. It includes all the regulators, outputs, and voltage monitors necessary for small PDAs while requiring a bare minimum of external components. This device features four linear regulators, a step-up DC-to-DC converter for LCD bias, a microprocessor reset output, and low battery detection in a miniature QFN package. For a compatible Li+ charger for both USB and AC adapter inputs, refer to the MAX1551.

The four linear regulators feature PMOS pass elements for efficient low-dropout operation. The MAIN LDO supplies 3.3V at over 300mA. An SD card slot output supplies 3.3V at 200mA. The COR1 LDO outputs 1.5V at 200mA and the COR2 LDO supplies 1.8V at 20mA. The SD output and COR2 LDOs have pin-controlled shutdown. For other output voltage combinations, contact Maxim.

The step-up DC-to-DC converter features an on-board MOSFET and true shutdown when off. This means that during shutdown, input power is disconnected from the inductor so the boost output falls to 0V rather than remaining one diode drop below the input voltage.

A µP reset output clears when the input voltage rises to 3.4V to ensure an orderly start. A low-battery output warns the system of impending power loss for safe shutdown. Thermal shutdown protects the die from overheating.

The MAX1552 operates from a 3.1V to a 5.5V supply voltage and consumes 50µA no-load supply current. It is packaged in a 1.3W, 16-pin thin QFN with a power pad on the underside of the package. The MAX1552 is specified for operation from -40°C to +85°C.

Applications

PDAs
Organizers
Cellular and Cordless Phones
MP3 Players
Hand-Held Devices

Pin Configuration appears at end of data sheet.

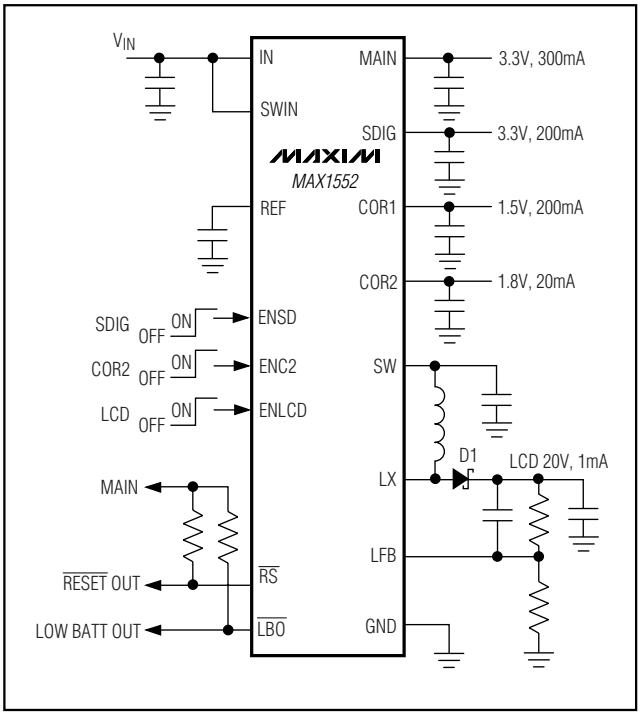
Features

- **Minimum External Components**
- **4 Linear Regulator Outputs**
  Main LDO 3.3V, 300mA
  SD Card Output 3.3V, 200mA
  Core LDO 1.5V, 200mA
  2nd Core LDO 1.8V, 30mA
- **High-Efficiency LCD Step-Up DC-to-DC Output**
  Up to 28V
  LCD 0V True Shutdown When Off
- **50µA Quiescent Supply Current**
- **1.3W Thin QFN Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1552ETE	-40°C to +85°C	16 Thin QFN

Typical Application Circuit



Complete Power IC for Low-Cost PDAs

ABSOLUTE MAXIMUM RATINGS

IN, SWIN, ENSD, ENC2, ENLCD, $\overline{RS}$, $\overline{LBO}$, SDIG, to GND .....-0.3V to +6V
LX to GND .....-0.3V to +30V
MAIN, COR1, COR2, REF, LFB to GND .....-0.3V to (V_{IN} + 0.3V)
SWIN to IN .....-0.3V to +0.3V
Current into LX or SWIN .....300mA_{RMS}
Current Out of SW .....300mA_{RMS}
Output Short-Circuit Duration .....Continuous

Continuous Power Dissipation (T_A = +70°C)
16-Pin Thin QFN (derate 16.9mW/°C above +70°C) ...1.349W
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = V_{SWIN} = V_{ENSD} = V_{ENC2} = V_{ENLCD} = 4.0V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL					
IN, SWIN Voltage Range	Operating	3.1		5.5	V
$\overline{RS}$ and Complete Shutdown Threshold	V_{IN} falling	2.96	3	3.04	V
$\overline{RS}$ Release and Restart Threshold	V_{IN} rising	3.4025	3.4	3.4400	V
$\overline{LBO}$ and Sleep Threshold	V_{IN} falling	3.55	3.6	3.65	V
$\overline{LBO}$ Release and Restart to Full On	V_{IN} rising	3.75	3.8	3.85	V
IN, SWIN Operating Current—All On	V_{LFB} = 1.3V		100	125	µA
IN Operating Current—All On Except LCD	ENLCD = GND		90	110	µA
IN Operating Current—MAIN and COR1 On	ENLCD = ENC2 = ENSD = GND, LDO loads = 0µA		50	65	µA
IN, SWIN Operating Current—Shut Down	V_{SWIN} = V_{IN} = 2.9V		2	10	µA
LDOs					
MAIN Output Voltage	I_{LOAD} = 100µA to 300mA, V_{IN} = 3.6V to 5.5V	3.2175	3.3	3.3825	V
MAIN Current Limit		350	650	1200	mA
MAIN Dropout Voltage	I_{LOAD} = 1mA		1		mV
	I_{LOAD} = 300mA		210	310	
SDIG Output Voltage	I_{LOAD} = 100µA to 200mA, V_{IN} = 3.6V to 5.5V	3.2175	3.3	3.3825	V
SDIG Current Limit		250	310	390	mA
SDIG Dropout Voltage	I_{LOAD} = 1mA		1		mV
	I_{LOAD} = 200mA		170	300	
SDIG Reverse Leakage Current	V_{SDIG} = 5V, ENSD = V_{IN} = GND		7	15	µA
COR1 Output Voltage	I_{LOAD} = 100µA to 200mA, V_{IN} = 3.6V to 5.5V	1.4625	1.5	1.5375	V
COR1 Current Limit		250	450	800	mA
COR2 Output Voltage	I_{LOAD} = 100µA to 20mA, V_{IN} = 3.6V to 5.5V	1.755	1.8	1.845	V
COR2 Current Limit		30	50	100	mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{SWIN} = V_{ENSD} = V_{ENC2} = V_{ENLCD} = 4.0V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LCD					
LX Voltage Range				28	V
LX Current Limit	L1 = 10µH	210	250	275	mA
LX On-Resistance			1.7		Ω
LX Leakage Current	V_{LX} = 28V			2	µA
Maximum LX On-Time		8	11	14	µs
Minimum LX Off-Time	V_{LFB} > 1.1V	0.8	1	1.2	µs
	V_{LFB} < 0.8V (soft-start)	4.0	5	6.0	
LFB Feedback Threshold		1.23	1.25	1.27	V
LFB Input Bias Current	V_{LFB} = 1.3V		5	100	nA
SW Off-Leakage Current	SW = GND, V_{SWIN} = 5.5V, ENLCD = GND		0.01	1	µA
SW PMOS On-Resistance			1		Ω
SW PMOS Peak Current Limit			750		mA
SW PMOS Average Current Limit			300		mA
Soft-Start Time	C_{SW} = 1µF		0.13		ms
LOGIC IN AND OUT					
EN_ Input Low Level	V_{IN} = 3.0V to 5.5V			0.4	V
EN_ Input High Level	V_{IN} = 3.0V to 5.5V	1.4			V
EN_ Input Leakage Current			0.01	1	µA
$\overline{RS}$, $\overline{LBO}$ Output Low Level	Sinking 1mA, V_{IN} = 2.5V		0.25	0.4	V
$\overline{RS}$, $\overline{LBO}$ Output High Leakage	V_{OUT} = 5.5V			1	µA
THERMAL PROTECTION					
Thermal-Shutdown Temperature	Rising temperature		160		°C
Thermal-Shutdown Hysteresis			15		°C

ELECTRICAL CHARACTERISTICS

(V_{IN} = V_{SWIN} = V_{ENSD} = V_{ENC2} = V_{ENLCD} = 4.0V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	MAX	UNITS
GENERAL				
IN, SWIN Voltage Range	Operating	3.1	5.5	V
$\overline{RS}$ and Complete Shutdown Threshold	V_{IN} falling	2.96	3.04	V
$\overline{RS}$ Release and Restart Threshold	V_{IN} rising	3.36	3.44	V
$\overline{LBO}$ and Sleep Threshold	V_{IN} falling	3.525	3.675	V
$\overline{LBO}$ Release and Restart to Full On	V_{IN} rising	3.725	3.875	V
IN, SWIN Operating Current—All On	V_{LFB} = 1.3V		125	µA
IN Operating Current—All On Except LCD	ENLCD = GND		110	µA
IN Operating Current—MAIN and COR1 On	ENLCD = ENC2 = ENSD = GND, LDO loads = 0µA		65	µA
IN, SWIN Operating Current—Shut Down	V_{SWIN} = V_{IN} = 2.925V		10	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{SWIN} = V_{ENSD} = V_{ENC2} = V_{ENLCD} = 4.0V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 1)

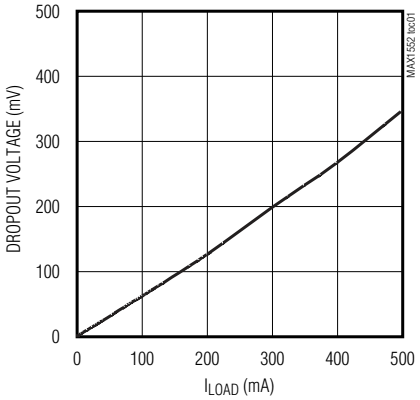
PARAMETER	CONDITIONS	MIN	MAX	UNITS
LDOs				
MAIN Output Voltage	I_{LOAD} = 100µA to 300mA, V_{IN} = 3.6V to 5.5V	3.2175	3.3825	V
MAIN Current Limit		350	1200	mA
MAIN Dropout Voltage	I_{LOAD} = 300mA		310	mV
SDIG Output Voltage	I_{LOAD} = 100µA to 200mA, V_{IN} = 3.6V to 5.5V	3.2175	3.3825	V
SDIG Current Limit		250	390	mA
SDIG Dropout Voltage	I_{LOAD} = 200mA		300	mV
SDIG Reverse Leakage Current	V_{SDIG} = 5V, ENSD = V_{IN} = GND		15	µA
COR1 Output Voltage	I_{LOAD} = 100µA to 20mA, V_{IN} = 3.6V to 5.5V	1.4625	1.5375	V
COR1 Current Limit		250	800	mA
COR2 Output Voltage	I_{LOAD} = 100µA to 20mA, V_{IN} = 3.6V to 5.5V	1.755	1.845	V
COR2 Current Limit		30	100	mA
LCD				
LX Voltage Range			28	V
LX Current Limit		200	275	mA
LX Leakage Current	V_{LX} = 28V		2	µA
Maximum LX On-Time		8	14	µs
Minimum LX Off-Time	V_{LFB} > 1.1V	0.8	1.2	µs
	V_{LFB} < 0.8V (soft-start)	4.0	6.0	
LFB Feedback Threshold		1.22	1.27	V
LFB Input Bias Current	V_{LFB} = 1.3V		100	nA
SW Off-Leakage Current	SW = GND, V_{SWIN} = 5.5V, ENLCD = GND		1	µA
LOGIC IN AND OUT				
EN_ Input Low Level	V_{IN} = 3.0V to 5.5V		0.4	V
EN_ Input High Level	V_{IN} = 3.0V to 5.5V	1.4		V
EN_ Input Leakage Current			1	µA
$\overline{RS}$, $\overline{LBO}$ Output Low Level	Sinking 1mA, V_{IN} = 2.5V		0.4	V
$\overline{RS}$, $\overline{LBO}$ Output High Leakage	V_{OUT} = 5.5V		1	µA

Note 1: Specifications to -40°C are guaranteed by design and not production tested.

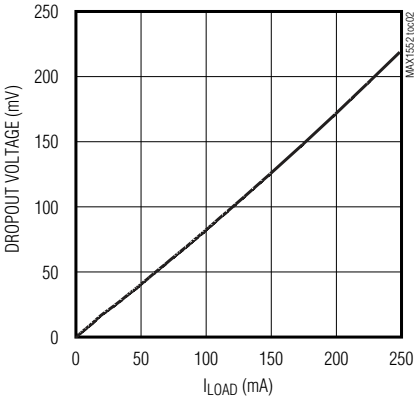
Typical Operating Characteristics

(Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

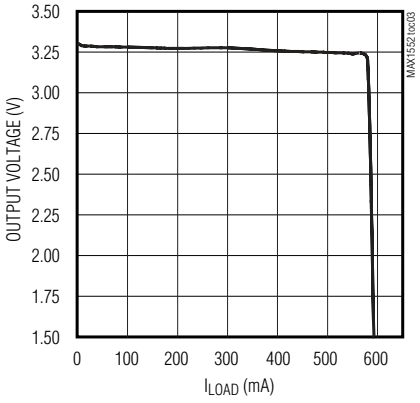
MAIN DROPOUT VOLTAGE vs. LOAD CURRENT



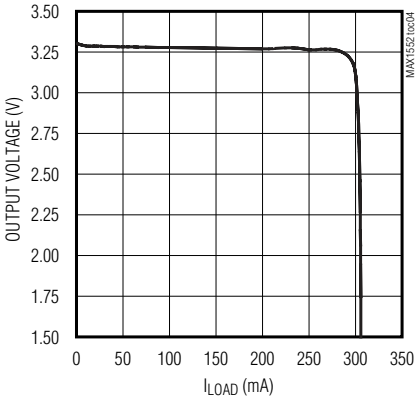
SDIG DROPOUT VOLTAGE vs. LOAD CURRENT



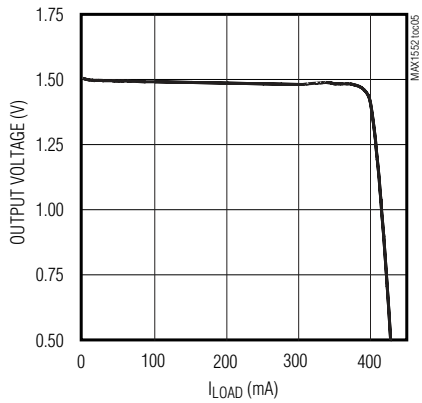
MAIN OUTPUT VOLTAGE vs. LOAD CURRENT



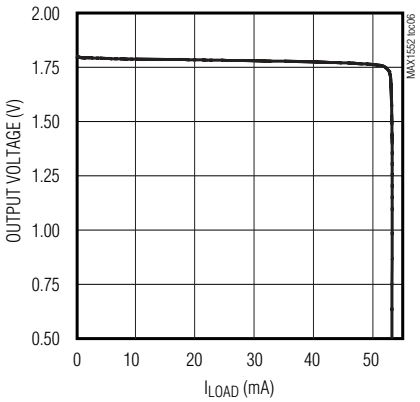
SDIG OUTPUT VOLTAGE vs. LOAD CURRENT



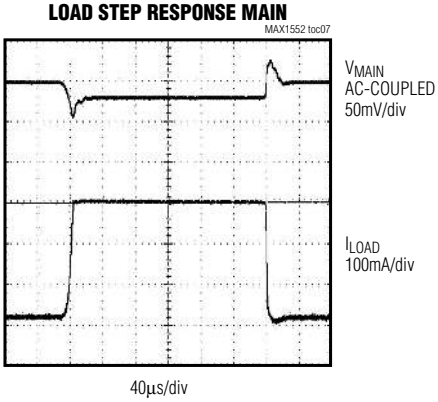
COR1 OUTPUT VOLTAGE vs. LOAD CURRENT



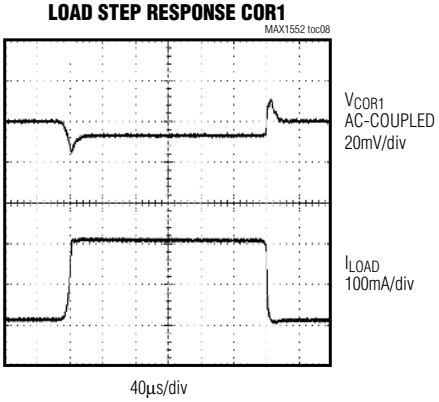
COR2 OUTPUT VOLTAGE vs. LOAD CURRENT



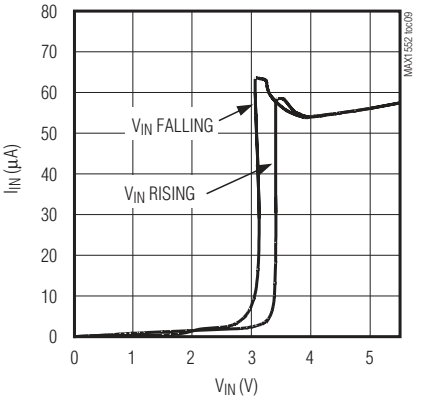
LOAD STEP RESPONSE MAIN



LOAD STEP RESPONSE COR1



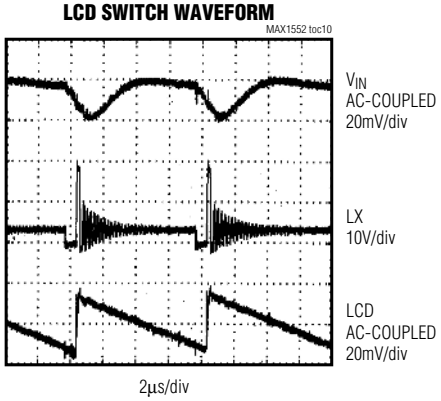
INPUT CURRENT vs. INPUT VOLTAGE



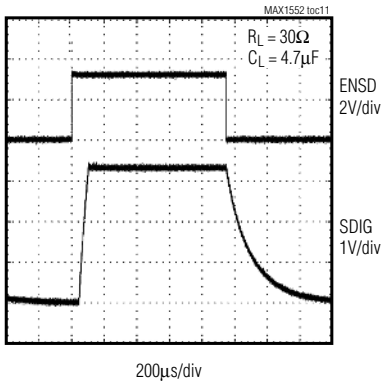
Typical Operating Characteristics (continued)

(Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

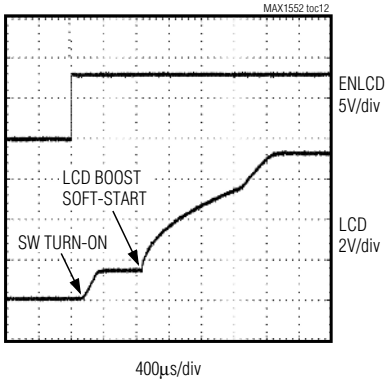
LCD SWITCH WAVEFORM



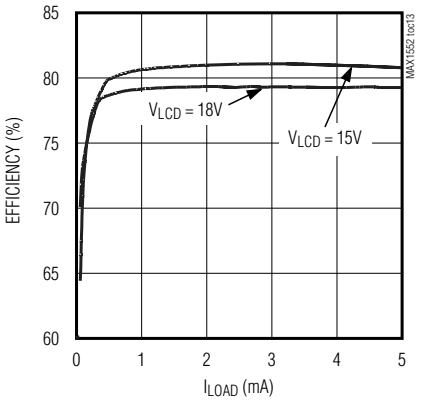
ENABLE RESPONSE TO ENSD



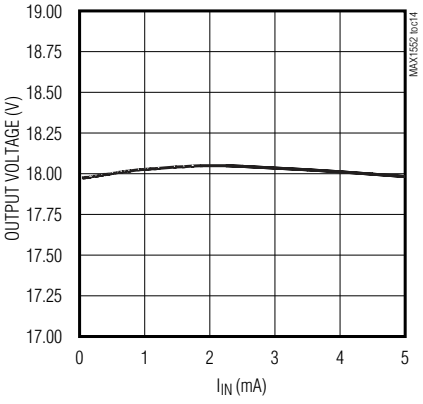
ENABLE RESPONSE TO LCD



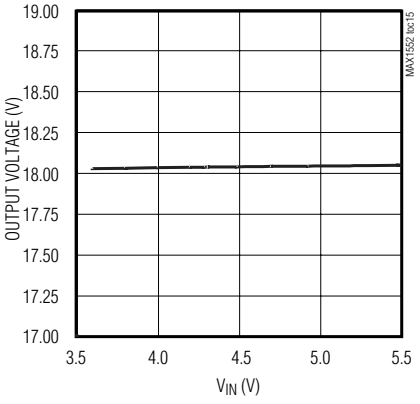
EFFICIENCY vs. LOAD CURRENT



LCD OUTPUT VOLTAGE vs. LOAD CURRENT



LCD OUTPUT VOLTAGE vs. INPUT VOLTAGE



Pin Description

PIN	NAME	FUNCTION
1	COR1	1.5V, 200mA LDO Output for CPU Core. COR1 turns off when V_{IN} < 3V.
2	IN	Input Voltage to the Device. Bypass IN to GND with a 1µF capacitor.
3	SDIG	3.3V, 200mA LDO Output for Secure Digital Card Slot. SDIG has reverse-current protection so SDIG can be biased when no power is present at IN. SDIG output turns off when V_{IN} < 3V or when ENSD goes low.
4	ENSD	SDIG Enable Input. Drive ENSD low to turn off the SDIG output. Drive ENSD high to turn on the SDIG output.
5	REF	1.25V Reference. Bypass REF with a 0.1µF capacitor to GND.
6	$\overline{RS}$	Reset Output. $\overline{RS}$ is an active-low, open-drain output that goes low when V_{IN} falls below 3.0V. $\overline{RS}$ deasserts when V_{IN} goes above 3.4V. Connect a 1MΩ pullup resistor from $\overline{RS}$ to MAIN.
7	$\overline{LBO}$	Low-Battery Output. $\overline{LBO}$ is an active-low, open-drain output that goes low when V_{IN} falls below 3.6V. $\overline{LBO}$ deasserts when V_{IN} goes above 3.8V. Connect a 1MΩ pullup resistor from $\overline{LBO}$ to MAIN.
8	GND	Ground
9	LX	LCD Boost Switch. Connect LX to a boost inductor and a rectifying Schottky diode. See Figure 1.
10	SW	LCD True Shutdown Switch Output. SW is the power source for the boost inductor. SW turns on when ENLCD is high.
11	SWIN	LCD True Shutdown Switch Input. The SWIN-to-SW switch turns off when ENLCD goes low or when V_{IN} < 3V. Connect SWIN to IN.
12	LFB	LCD Feedback Input. Connect LFB to a resistor-divider network between the LCD output and GND. The feedback threshold is 1.25V.
13	ENLCD	Enable Input for LCD (Boost Regulator). Drive ENLCD high to activate the LCD boost. Drive ENLCD low to shut down the LCD output.
14	ENC2	Enable Input for Secondary Core LDO (COR2). Drive ENC2 high to turn on COR2. Drive low to turn off COR2.
15	COR2	1.8V, 30mA LDO Output for Secondary Core. COR2 output turns off when V_{IN} < 3V or when ENC2 goes low.
16	MAIN	3.3V, 300mA LDO Output for Main Supply. MAIN output turns off when V_{IN} < 3V.

Detailed Description

Linear Regulators

The MAX1552 contains all power blocks and voltage monitors for a small PDA. Power for logic and other subsystems is provided by four LDOs:

- MAIN—Provides 3.3V at a guaranteed 350mA with a typical current limit of 650mA.
- SDIG—Provides 3.3V at a guaranteed 250mA for secure digital cards with a typical current limit at 310mA.
- COR1—1.5V for CPU core guarantees 250mA and typically current limits at 450mA.
- COR2—1.8V for CODEC core guarantees 30mA and typically current limits at 50mA.

MAIN and COR1 regulators are always on as long as the IC is not in low-voltage shutdown (V_{IN} < 3V). COR2 and SDIG can be turned on and off independently through logic signals at ENC2 and ENSD, respectively.

When SDIG is turned off, reverse current is blocked so the SDIG output can be biased with an external source when no power is present at IN. Leakage current is typically 3µA with 3.3V at SDIG.

LCD Boost DC-to-DC

In addition to the LDOs, the MAX1552 also includes a low-current, high-voltage-boost DC-to-DC converter for LCD bias. This circuit can output up to 28V and can be adjusted with either an analog or PWM control signal using external components.

SW provides an input-power disconnect for the LCD when ENLCD is low (off). The input-power disconnect function is ideal for applications that require the output voltage to fall to 0V in shutdown (true shutdown). If true shutdown is not required, the SW switch can be bypassed by connecting the boost inductor directly to IN and removing the bypass capacitor on SW (C9 in Figure 1).

Complete Power IC for Low-Cost PDAs

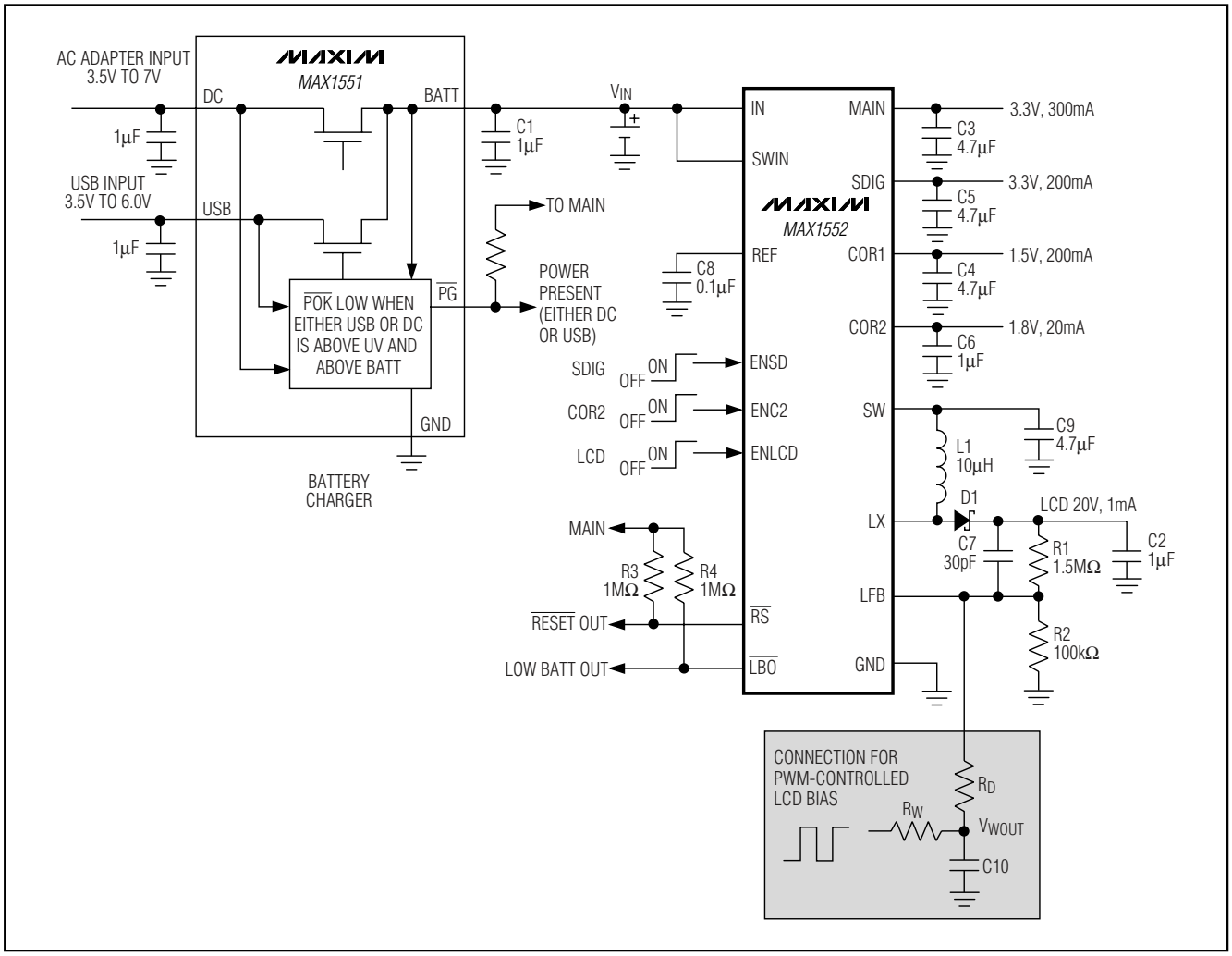


Figure 1. Typical Operating Circuit with Charger and External PWM LCD Control

Voltage Monitors ($\overline{LBO}$)—System Sleep

The MAX1552 monitors the battery voltage at IN. When V_{IN} falls below 3.6V, $\overline{LBO}$ goes low, typically putting the system (µP) into a sleep state. The MAX1552 remains fully functional in this state and all outputs maintain normal operation. However, when in sleep mode, the system (µP) typically drives ENSD, ENC2, and ENLCD low, turning off COR2, SDIG, and the LCD boost output. Sleep can be set by the system (µP) even without a low battery event. The MAX1552 consumes 50µA when the system is in sleep mode. The $\overline{LBO}$ output is deasserted when the battery voltage rises above 3.8V

All regulated outputs turn off when V_{IN} falls below 3V. The MAX1552 resumes normal operation when V_{IN} rises above 3.4V.

Reset Output ($\overline{RS}$)

Reset ($\overline{RS}$) asserts when V_{IN} goes below 3V. The reset output remains asserted until V_{IN} rises above 3.4V. $\overline{RS}$ is an open-drain, active-low output. Connect a 1MΩ resistor from $\overline{RS}$ to MAIN.

Applications Information

LDO Output Capacitors (MAIN, SDIG, COR1, and COR2)

Capacitors are required at each output of the MAX1552 for stable operation over the full load and temperature range. See Figure 1 for recommended capacitor values for each output. To reduce noise and improve load transients, use large output capacitors, up to 10µF. Surface-mount ceramic capacitors have very low ESR

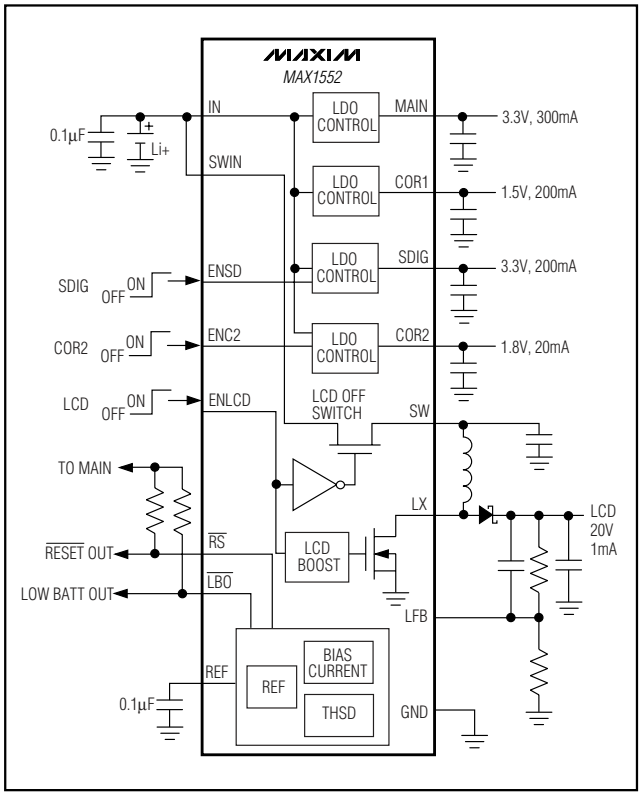


Figure 2. Block Diagram

and are commonly available in values up to 10µF. X7R and X5R dielectrics are recommended. Note that some ceramic dielectrics, such as Z5U and Y5V, exhibit large capacitance and ESR variation with temperature and require larger than the recommended values to maintain stability over temperature.

LCD Boost Output

Selecting an Inductor

The LCD boost is designed to operate with a wide range of inductor values (4.7µH to 22µH). Smaller inductance values typically offer smaller physical size for a given series resistance or saturation current. Smaller values make LX switch more frequently for a given load and can reduce efficiency at low load currents. Larger values reduce switching losses due to less frequent switching for a given load, but higher resistance may then reduce efficiency. A 10µH inductor provides a good balance and works well for most applications. The inductor's saturation current rating should be greater than the peak switching current (250mA); however, it is generally acceptable to bias some inductors into saturation by as much as 20%, although this slightly reduces efficiency.

Selecting a Diode

Schottky diodes rated at 250mA or more, such as the Motorola MBRS0530 or Nihon EP05Q03L, are recommended. The diode reverse-breakdown voltage rating must be greater than the LCD output voltage.

Selecting Capacitors

For most applications, use a small 1µF LCD output capacitor. This typically provides an output ripple of $30mV_{P-P}$. In addition, bypass IN with 1µF, and SW with 4.7µF ceramic capacitors.

An LCD feed-forward capacitor, connected from the output to FB, improves stability over a wide range of battery voltages. A 33pF capacitor is sufficient for most applications; however, this value is also affected by PC board layout.

Setting the LCD Voltage

Adjust the output voltage by connecting a voltage-divider from the output (V_{OUT}) to FB (see Figure 1). Select R2 between 10kΩ and 200kΩ. Calculate R1 with the following equation:

$$R1 = R2\ [(V_{OUT} / V_{FB}) - 1]$$

where V_{FB} = 1.25V and V_{OUT} can range from V_{IN} to 28V. The input bias current of FB is typically only 5nA, which allows large-value resistors to be used. For less than 1% error, the current through R2 should be greater than 100 times the feedback input bias current (I_{FB}).

LCD Adjustment

The LCD boost output can be digitally adjusted by either a DAC or PWM signal.

DAC Adjustment

Adding a DAC and a resistor, R_D, to the divider circuit (Figure 3) provides DAC adjustment of V_{OUT}. Ensure that $V_{OUT(MAX)}$ does not exceed the LCD panel rating. The output voltage (V_{OUT}) as a function of the DAC voltage (V_{DOUT}) can be calculated using the following formula:

$$V_{OUT} = 1.25 \times \left(1+\left(\frac{R1}{R2}\right)\right)+\frac{(1.25 - V_{DOUT}) \times R1}{R_D}$$

Using PWM Signals

Many microprocessors have the ability to create PWM outputs. These are digital outputs, based on either 16-bit or 8-bit counters, with programmable duty cycle. In many applications they are suitable for adjusting the output of the MAX1552 (Figure 1).

Complete Power IC for Low-Cost PDAs

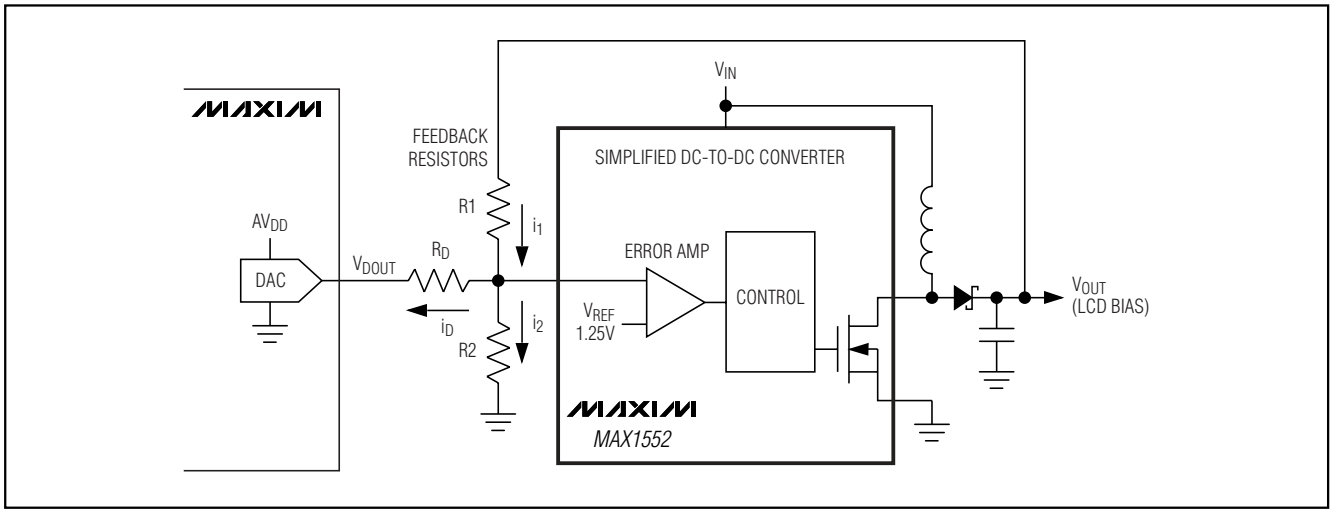


Figure 3. Adjusting the Output Voltage with a DAC

The circuit consists of the PWM source, capacitor C10, and resistors R_D and R_W. To analyze the transfer function of the PWM circuit, it is easiest to first simplify it to its Thevenin equivalent. The Thevenin voltage can be calculated using the following formula:

$$V_{THEV} = (D \times V_{OH}) + (1 - D) \times V_{OL}$$

where D is the duty cycle of the PWM signal, V_{OH} is the PWM output high level (often 3.3V), and V_{OL} is the PWM output low level (usually 0V). For CMOS logic this equation simplifies to:

$$V_{THEV} = D \times V_{DD}$$

where V_{DD} is the I/O voltage of the PWM output. The Thevenin impedance is the sum of resistors R_W and R_D:

$$R_{THEV} = R_D + R_W$$

The output voltage (V_{OUT}) as a function of the PWM average voltage (V_{THEV}) is:

$$V_{OUT} = 1.25 \times \left(1+\left(\frac{R1}{R2}\right)\right)+\frac{(1.25 - V_{THEV}) \times R1}{R_{THEV}}$$

When using the PWM adjustment method, R_D isolates the capacitor from the feedback loop of the MAX1552. The cutoff frequency of the lowpass filter is defined as:

$$f_C = \frac{1}{2 \times \pi \times R_{THEV} \times C10}$$

The cutoff frequency should be at least two decades below the PWM frequency to minimize the induced AC ripple at the output.

An important consideration is the turn-on transient created by the initial charge on filter capacitor C10. This capacitor forms a time constant with R_{THEV}, which causes the output to initialize at a higher-than-intended voltage. This overshoot can be minimized by scaling R_D as high as possible compared to R1 and R2. Alternatively, the µP can briefly keep the LCD disabled until the PWM voltage has had time to stabilize.

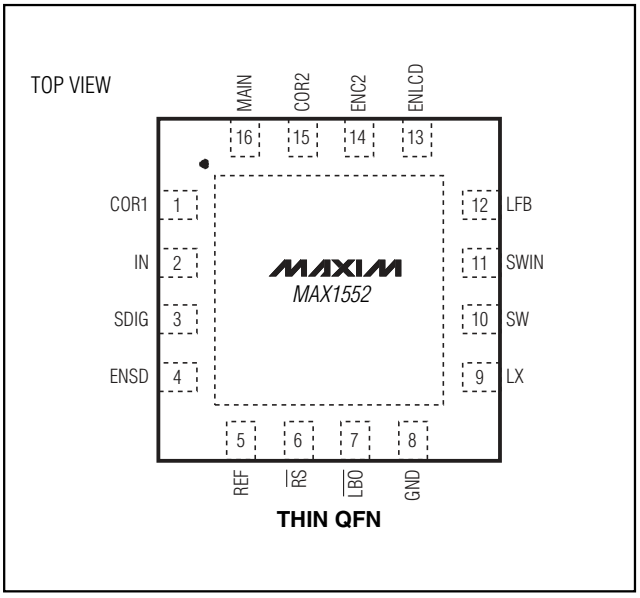
PC Board Layout and Grounding

Careful PC board layout is important for minimizing ground bounce and noise. Keep the MAX1552's ground pin and the ground leads of the input and output capacitors less than 0.2in (5mm) apart. In addition, keep all connections to FB and LX as short as possible. In particular, external feedback resistors should be as close to FB as possible. To minimize output voltage ripple, and to maximize output power and efficiency, use a ground plane and solder GND directly to the ground plane. Refer to the MAX1552 evaluation kit for a layout example.

Thermal Considerations

In most applications, the circuit is located on a multilayer board and full use of the four or more layers is recommended. For heat dissipation, connect the exposed backside pad of the QFN package to a large analog ground plane, preferably on a surface of the board that receives good airflow. Typical applications use multiple ground planes to minimize thermal resistance. Avoid large AC currents through the analog ground plane.

Pin Configuration



THIN QFN

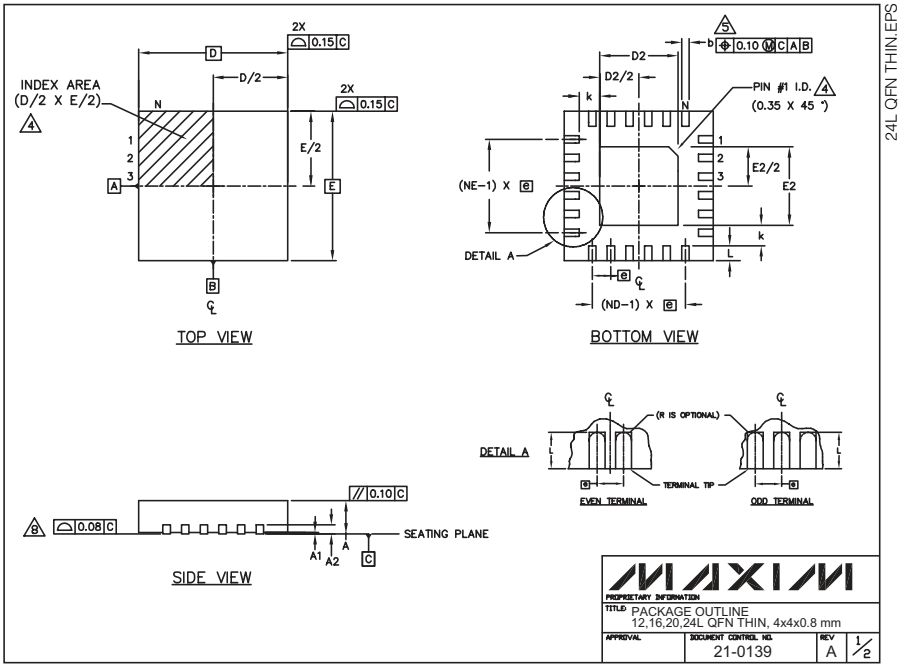
Chip Information

TRANSISTOR COUNT: 1872

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



COMMON DIMENSIONS												
PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.		
k	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50
N	12			16			20			24		
ND	3			4			5			6		
NE	3			4			5			6		
Jedec Var.	WGGB			WGGC			WGGD-1			WGGD-2		

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1244-2	1.95	2.10	2.25	1.95	2.10	2.25
T1644-2	1.95	2.10	2.25	1.95	2.10	2.25
T2044-1	1.95	2.10	2.25	1.95	2.10	2.25
T2444-1	2.45	2.60	2.63	2.45	2.60	2.63

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220.

PROPRIETARY INFORMATION
TITLE PACKAGE OUTLINE 12,16,20,24L QFN THIN, 4x4x0.8 mm
APPROVAL
DOCUMENT CONTROL NO. 21-0139
REV A
2/2

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