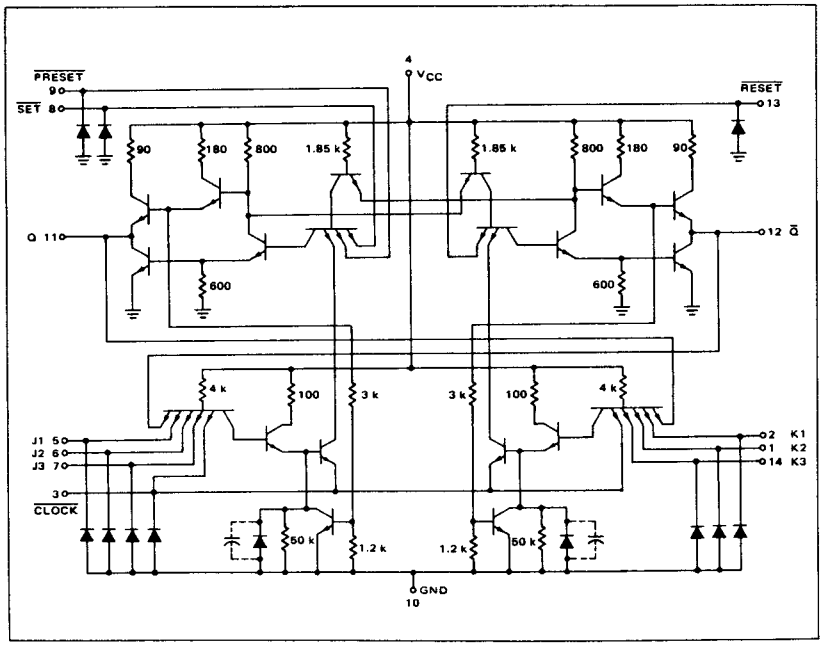
MC2125 • MC2175
MC2025 • MC2075

The MC2025, MC2075, MC2125, and MC2175 are clocked flip-flops that toggle at 50 MHz, trigger on the negative edge of the clock pulse, and perform the J-K logic function. Each flip-flop has an AND-input gating configuration consisting of three J inputs ANDed together and three K inputs ANDed together. The multiple J and K inputs minimize the requirements for external gating in counters and certain other applications. A direct $\overline{SET}$, $\overline{PRESET}$, and $\overline{RESET}$ are also available. These devices are pin compatible with the MC2109 series of devices. Electrical differences include input loading factors for the $\overline{SET}$, $\overline{PRESET}$, and $\overline{RESET}$ inputs which are approximately twice the loading factors of the MC2109 series.

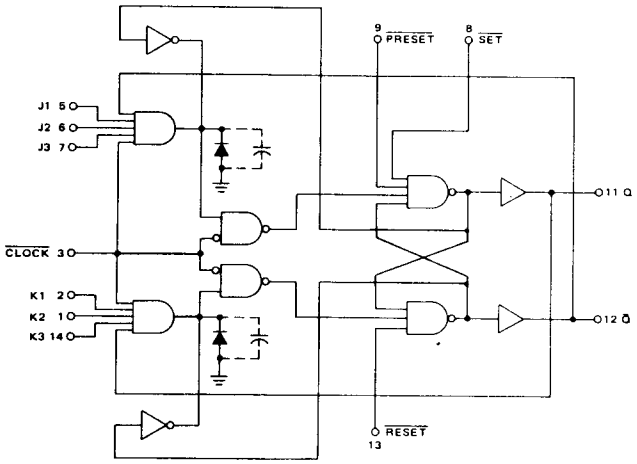
Information is changed on the J and K inputs while the clock is in the low state, since the inputs are inhibited in this condition. Information is transferred into a temporary memory when the clock goes to a high state. When the clock returns low, the information is transferred to the bistable section and the Q and $\overline{Q}$ outputs respond accordingly. The information on the J and K inputs should not be changed while the clock is high.

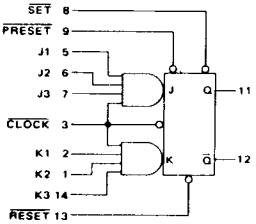
Each flip-flop can be set or reset directly by the direct $\overline{SET}$, $\overline{PRESET}$, or $\overline{RESET}$ inputs. Since these flip-flops are charge-storage devices, there is a restriction on the clock fall time that must be observed.

TYPE NO.	INPUT LOADING FACTOR (I_F)						OUTPUT DRIVE (I_{OL})	TEMPERATURE RANGE
	$\overline{CLOCK}$	$\overline{SET}$ $\overline{PRESET}$ $\overline{RESET}$	J,K	$\overline{CLOCK}$	$\overline{SET}$ $\overline{PRESET}$ $\overline{RESET}$	J,K		
MC2125 MC2175	1.0	1.2	0.67	(−1.33 mA)	(−2.4 mA)	(−1.33 mA)	11 MC2100 series Gates (22.0 mA) 6 MC2100 series Gates (12.0 mA)	−55°C to +125°C
MC2025 MC2075	1.0	1.2	0.67	(−1.66 mA)	(−2.8 mA)	(−1.66 mA)	9 MC2000 series Gates (22.5 mA) 5 MC2000 series Gates (12.5 mA)	0°C to +75°C



LOGIC DIAGRAM





J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Where J = J1 • J2 • J3
K = K1 • K2 • K3

Total Power Dissipation = 50 mW typ/pkg
Switching Times:
t_{pd-} = 11 ns typ
t_{pd+} = 9.0 ns typ
Operating Frequency = 70 MHz typ

OPERATING CHARACTERISTICS

Clock fall time ≤ 100 ns.

Triggers on clock pulse widths ≥ 10 ns.

Provides direct $\overline{SET}$, $\overline{PRESET}$, and $\overline{RESET}$ inputs. The application of a "0" state to the $\overline{SET}$ or $\overline{PRESET}$ will cause Q to go to the "1" state; application of a "0" state to the $\overline{RESET}$ will cause Q to go to the "0" state. The clock must be in the low state when these functions are performed. Since there is almost no post time associated with these devices, the direct inputs can be applied 15 ns after the clock signal has fallen.

Data at the J and K inputs must be present before the clock goes to a high state. If the information on the J and K inputs is changed while the clock is in a high state, the flip-flop will require typically 1.0 μs to recognize a "1" state to "0" state information change on the J and K terminals. The flip-flop typically requires 10 ns to recognize a "0" state to "1" state change.

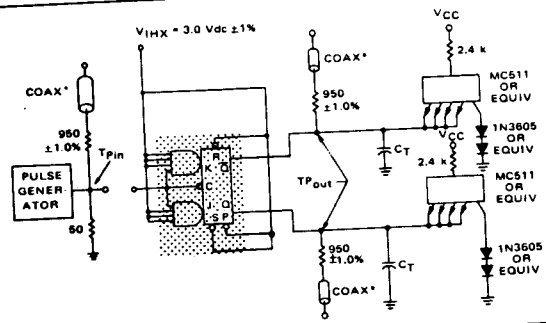
By using an internally cross-coupled network and buffered outputs, the propagation delays (t_{pd-} and t_{pd+}) are nearly symmetrical. The outputs are capable of driving high capacitive loads without degrading the frequency of operation.

Negative edge triggering – When the clock goes from the high state to the low state, the information in the temporary storage section is transferred to the bistable network and the data appears at the Q and $\overline{Q}$ outputs. While the clock is in a low state, the J and K terminals are inhibited.

Unused J and K inputs should be tied to the clock or to a voltage between 2.0 and 5.0 Vdc. Other unused inputs should be tied to a voltage between 2.0 and 5.0 Vdc.

The maximum allowable clock skew time is 9.0 ns. This is the total of the minimum time to recognize a "0" state to "1" state change (4.0 ns) and the minimum propagation delay (5.0 ns).

FIGURE 1 – SWITCHING AND TRIGGER CHARACTERISTICS TEST CIRCUIT



*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedence constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

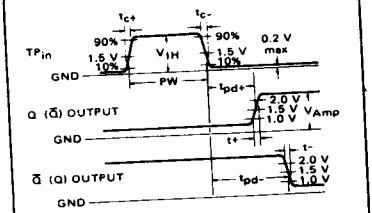
SWITCHING TIMES

TEST	TEST SYMBOL	INPUT PULSE	MIN	MAX	UNIT
Delay Time Off	t_{pd+}	V	–	15	ns
Delay Time On	t_{pd-}	V	–	15	ns
Rise Time	t_+	V	–	4.0	ns
Fall Time	t_-	V	–	2.5	ns
Amplitude	V_{Amp}	V	3.0	–	Volt

WORST-CASE TESTS
(Device must toggle with each clock pulse)

TEST	SYMBOL	LIMITS	INPUT CONDITIONS
Toggle Frequency	f_{Tog}	60 MHz max	W
Pulse Width	PW	10 ns min	X
Input High Voltage	V_{IH}	1.8 V min	Y
Fall Time	t_f	100 ns max	Z

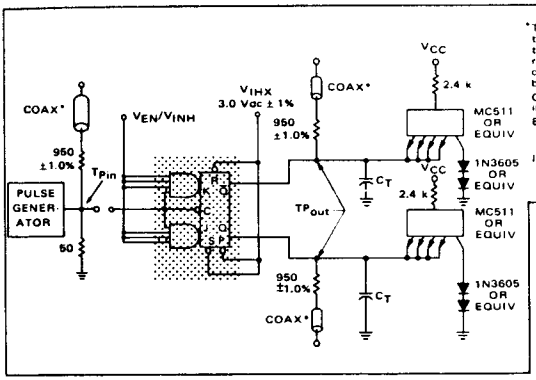
VOLTAGE WAVEFORMS AND DEFINITIONS



INPUT PULSE CONDITIONS

SYMBOL	V	W	X	Y	Z	UNIT
PRF	5.0	50	5.0	5.0	1.0	MHz
PW	10	10	10	10	200	ns
t_+	≤2.0	≤5.0	≤5.0	≤5.0	≤50	ns
t_-	≤2.0	≤5.0	≤5.0	≤5.0	100	ns
V_{IH}	3.0	3.0	3.0	2.4	3.0	Volt

FIGURE 2 – J-K TERMINAL CHARACTERISTICS TEST CIRCUIT



*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

Enable Mode Test
The device under test shall toggle when V_{EN} = 1.8 Vdc ± 1.0% is applied.

Inhibit Mode Test
The device under test shall NOT toggle when V_{INH} = 1.2 Vdc ± 1.0% is applied.

INPUT VOLTAGE WAVEFORMS AND DEFINITIONS

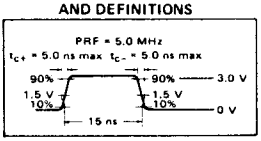
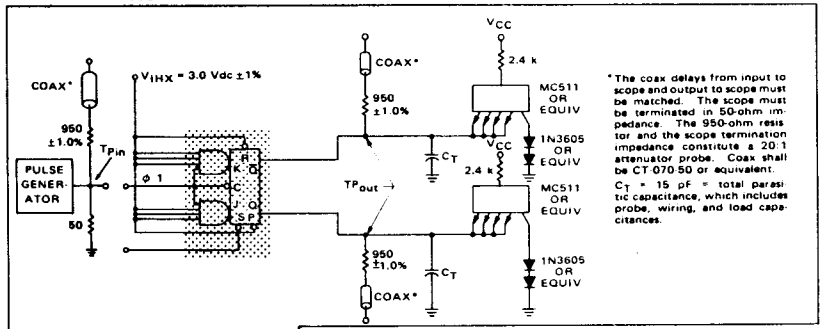


FIGURE 3 – SET-RESET-PRESET TERMINAL CHARACTERISTICS TEST CIRCUIT



*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

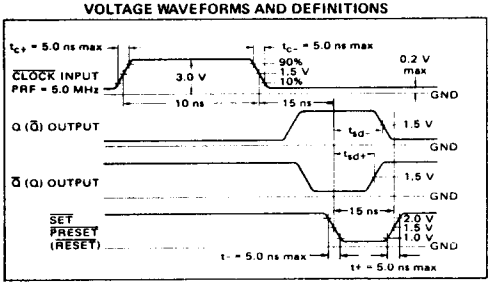
Two pulse generators are required and must be slaved together to provide the waveforms shown.

TEST PARAMETERS

SYMBOL	VALUE	UNIT
t_{sd-}	15	ns max
t_{sd+}	15	ns max

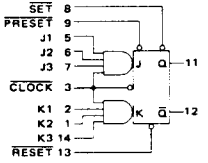
NOTE:
Connections shown for measuring times related to SET terminal only. To measure times at PRESET terminal apply input pulse to Pin 9 in place of Pin 8. To measure times at RESET terminals, apply the input pulse to Pin 13.

VOLTAGE WAVEFORMS AND DEFINITIONS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one J and K input, plus the $\overline{SET}$, $\overline{PRESET}$, and $\overline{RESET}$ inputs. To complete testing, sequence through remaining J and K inputs in the same manner.



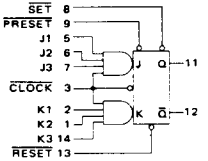
@ Test Temperature		TEST CURRENT / VOLTAGE VALUES: mA I_{OL} Pr*	I_{OL} Std	I_{OH} Pr*	I_{OH} Std	I_{in}	$2I_{in}$	Volts V_{IL}	V_{IH}	V_R	$V_{th\,1}$	$V_{th\,0}$	V_{out}	V_{CC}
MC2125*, MC2175	−55°C	22.0	12.0	-1.5	-0.7	1.0	2.0	0.45	2.8	4.5	2.0	0.9	5.5	5.0
	+25°C	22.0	12.0	-1.2	-0.7	1.0	2.0	0.45	2.8	4.5	1.8	1.1	5.5	5.0
	+125°C	22.0	12.0	-1.2	-1.1	1.0	2.0	0.45	2.8	4.5	1.5	0.9	5.5	5.0
MC2025*, MC2075	0°C	22.5	12.5	-1.8	-1.0	1.0	2.0	0.45	3.0	4.5	1.9	1.0	5.5	5.0
	+25°C	22.5	12.5	-1.8	-1.0	1.0	2.0	0.45	3.0	4.5	1.8	1.1	5.5	5.0
	+75°C	22.5	12.5	-1.8	-1.0	1.0	2.0	0.45	3.0	4.5	1.7	1.0	5.5	5.0

Characteristic	Symbol	Pin Under Test	MC2125, MC2175 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC2025, MC2075 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	$2I_{in}$	V_{IL}	V_{IH}	V_R	$V_{th\,1}$	$V_{th\,0}$	V_{out}	V_{CC}	**	Gnd
Input																												
Forward Current J	I_F	5	-	-1.33	-	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1.66	mAdc	-	-	-	-	-	-	1,2,3,6,7,8,9,14	-	-	-	4	-	5,10,13
K		1	-	-1.33	-	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1.66		-	-	-	-	-	-	2,3,5,6,7,9,13,14	-	-	-		-	1,8,10
Set		8	-	-2.4	-	-2.4	-	-2.4	-	-2.8	-	-2.8	-	-2.8		-	-	-	-	-	-	1,2,3,5,6,7,9,13,14	-	-	-		-	8,10
Preset		9	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓		-	-	-	-	-	-	1,2,3,5,6,7,8,13,14	-	-	-		-	9,10
Reset		13	-		-		-		-		-		-			-	-	-	-	-	-	1,2,3,5,6,7,8,9,14	-	-	-		-	10,13
Clock		3	-	-1.33	-	-1.33	-	-1.33	-	-1.66	-	-1.66	-	-1.66		-	-	-	-	3	-	1,2,5,6,7,8,9,13,14	-	-	-		-	10
Leakage Current J	I_R	5	-	70	-	70	-	70	-	70	-	70	-	70	μAdc	-	-	-	-	-	-	5,9	-	-	-	4	8	3,6,7,10
K		1	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓		-	-	-	-	-	-	1,8,9	-	-	-		13	2,3,10,14
Set		8	-		-		-		-		-		-			-	-	-	-	-	-	8,13	-	-	-		-	3,9,10,12
Preset		9	-		-		-		-		-		-			-	-	-	-	-	-	9,13	-	-	-		-	3,8,10
Reset		13	-		-		-		-		-		-			-	-	-	-	-	-	8,9,13	-	-	-		13	3,10
Clock		3	-	140	-	140	-	140	-	140	-	140	-	140		-	-	-	-	-	-	3	-	-	-	↓	-	1,2,5,6,7,10,14
Inverse Beta J Current	I_L	5	-	70	-	70	-	70	-	70	-	70	-	70	μAdc	-	-	-	-	13	-	5	-	-	-	4	-	10
K		1	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓		-	-	-	-	8	-	1	-	-	-		-	↓
Set		8	-		-		-		-		-		-			-	-	-	-	13	-	8	-	-	-		-	
Preset		9	-		-		-		-		-		-			-	-	-	-	13	-	9	-	-	-		-	
Reset		13	-		-		-		-		-		-			-	-	-	-	8	-	13	-	-	-		-	
Clock		3	-	140	-	140	-	140	-	140	-	140	-	140		-	-	-	-	13	-	3	-	-	-		-	
		3	-	140	-	140	-	140	-	140	-	140	-	140		-	-	-	-	8	-	3	-	-	-	↓	-	↓
Breakdown J Voltage	BV_{in} "0"	5	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	5	-	13	-	-	-	-	-	4	-	10
K		1	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-		-	-	1	-	8	-	-	-	-	-		-	↓
Set		8		-		-		-		-		-		-		-	-	8	-	13	-	-	-	-	-		-	
Preset		9		-		-		-		-		-		-		-	-	9	-	13	-	-	-	-	-		-	
Reset		13		-		-		-		-		-		-		-	-	13	-	8	-	-	-	-	-		-	
Clock		3		-		-		-		-		-		-		-	-	-	3	13	-	-	-	-	-		-	
		3		-		-		-		-		-		-		-	-	-	3	8	-	-	-	-	-	↓	-	↓
J	BV_{in} "1"	5	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc	-	-	5	-	-	-	9	-	-	-	4	8	3,6,7,10
K		1	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-		-	-	1	-	-	-	8,9	-	-	-		13	2,3,10,14
Set		8		-		-		-		-		-		-		-	-	8	-	-	-	13	-	-	-		-	3,9,10
Preset		9		-		-		-		-		-		-		-	-	9	-	-	-	-	-	-	-		-	3,8,10
Reset		13		-		-		-		-		-		-		-	-	13	-	-	-	-	-	-	-		13	3,10
Clock		3		-		-		-		-		-		-		-	-	-	3	-	-	-	-	-	-	↓	-	1,2,5,6,7,10,14

(continued)

ELECTRICAL CHARACTERISTICS (continued)

Test procedures are shown for only one J and K input, plus the $\overline{SET}$, $\overline{PRESET}$, and $\overline{RESET}$ inputs. To complete testing, sequence through remaining J and K inputs in the same manner.



	@ Test Temperature	TEST CURRENT / VOLTAGE VALUES: I_{OL} mA Pr*	I_{OL} mA Std	I_{OH} mA Pr*	I_{OH} mA Std	I_{in} mA	$2I_{in}$ mA	V_{IL} Volts	V_{IH} Volts	V_R Volts	$V_{th\,1}$ Volts	$V_{th\,0}$ Volts	V_{out} Volts	V_{CC} Volts
MC2125*, MC2175	−55°C	22.0	12.0	-1.5	-0.7	1.0	2.0	0.45	2.8	4.5	2.0	0.9	5.5	5.0
	+25°C	22.0	12.0	-1.2	-0.7	1.0	2.0	0.45	2.8	4.5	1.8	1.1	5.5	5.0
	+125°C	22.0	12.0	-1.2	-1.1	1.0	2.0	0.45	2.8	4.5	1.5	0.9	5.5	5.0
MC2025*, MC2075	0°C	22.5	12.5	-1.8	-1.0	1.0	2.0	0.45	3.0	4.5	1.9	1.0	5.5	5.0
	+25°C	22.5	12.5	-1.8	-1.0	1.0	2.0	0.45	3.0	4.5	1.8	1.1	5.5	5.0
	+75°C	22.5	12.5	-1.8	-1.0	1.0	2.0	0.45	3.0	4.5	1.7	1.0	5.5	5.0

Characteristic	Symbol	Pin Under Test	MC2125, MC2175 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC2025, MC2075 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	$2I_{in}$	V_{IL}	V_{IH}	V_R	$V_{th\,1}$	$V_{th\,0}$	V_{out}	V_{CC}	**	Gnd
Output																												
Output Voltage	V_{out} "0"	11	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc	11	-	-	-	-	-	-	8	-	-	4	-	3,10,13
		11	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	↓	11	-	-	-	-	-	-	9	-	-	↓	-	3,10,13
		12	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	↓	12	-	-	-	-	-	-	13	-	-	↓	-	3,8,10
	V_{out} "1"	11	2.5	-	2.4	-	2.5	-	2.5	-	2.4	-	2.5	-	Vdc	-	11	-	-	-	-	-	-	8	-	4	-	3,10,13
		11	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-	11	-	-	-	-	-	-	9	-	↓	-	3,10,13
		12	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-	12	-	-	-	-	-	-	13	-	↓	-	3,8,10
Leakage Current	$I_{O(L)K}$	11	-	1.25	-	1.25	-	1.25	-	1.25	-	1.25	-	1.25	mAdc	-	-	-	-	-	-	-	-	-	11	4	-	1,2,3,5,6,7,8,9,10,14
		12	-	1.25	-	1.25	-	1.25	-	1.25	-	1.25	-	1.25	mAdc	-	-	-	-	-	-	-	-	-	12	4	-	1,2,3,5,6,7,10,13,14
Short Circuit Current*	I_{SC}	11	-30	-90	-30	-90	-30	-90	-30	-90	-30	-90	-30	-90	mAdc	-	-	-	-	-	-	-	-	-	-	4	-	1,2,3,5,6,7,8,9,10,11,14
		12	-30	-90	-30	-90	-30	-90	-30	-90	-30	-90	-30	-90	mAdc	-	-	-	-	-	-	-	-	-	-	4	-	1,2,3,5,6,7,10,12,13,14
Output Voltage	V_{OL}	11	-	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc	11	-	-	-	-	8	-	-	-	-	4	-	3,10,13
		11	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	↓	11	-	-	-	-	9	-	-	-	-	↓	-	3,10,13
		12	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	↓	12	-	-	-	-	13	-	-	-	-	↓	-	3,8,10
	V_{OH}	11	2.8	-	3.0	-	3.0	-	3.0	-	3.0	-	3.0	-	Vdc	-	11	-	-	8	-	-	-	-	-	4	-	3,10,13
		11	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-	11	-	-	9	-	-	-	-	-	↓	-	3,10,13
		12	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-	↓	-	12	-	-	13	-	-	-	-	-	↓	-	3,8,10
Power Requirements																												
Power Supply Drain	I_{PD}	4	-	14	-	14	-	14	-	17	-	17	-	17	mAdc	-	-	-	-	-	-	-	-	-	-	4	-	3,10,13
		4	-	14	-	14	-	14	-	17	-	17	-	17	mAdc	-	-	-	-	-	-	-	-	-	-	4	-	3,8,10

*Prime Fan-Out.

**Momentarily ground pin prior to taking measurement to set flip-flop in desired state. If pin is also in another column, the pin must be returned to that voltage or current for measurement.

Table 3-4 DSP56001A Identification by Signal Name (Continued)

Signal Name	132 pin "FC" PQFP or "FE" CQFP Pin No.	88 pin "RC" PGA Pin No.	Signal Name	132 pin "FC" PQFP or "FE" CQFP Pin No.	88 pin "RC" PGA Pin No.
$\overline{WT}$	45	L13	nc	103	
X/$\overline{Y}$	48	N13	nc	107	
XTAL	126	A6	nc	110	
nc	3		nc	116	
nc	4		nc	117	
nc	7		nc	122	
nc	17		nc	125	
nc	18		nc	132	
nc	21				

Power and ground pins have special considerations for noise immunity. See the section **Design Considerations**.

Table 3-5 DSP56001A Power Supply Pins

132 pin "FC" PQFP or "FE" CQFP Pin No.	88 pin "RC" PGA Pin No.	Power Supply	Circuit Supplied
63	L8	V_{CCN}	Address Bus Buffers
64			
55	L6	GNDN	
56	L9		
73			
74			