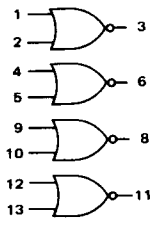
MC1010 thru MC1012
MC1210 thru MC1212

Provide the NOR output function. These devices contain an internal bias reference insuring that the threshold point is always in the center of the transition region over the temperature range.

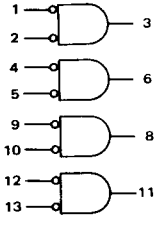
Emitter follower output configurations differ for these three circuits as shown in the circuit schematic.

POSITIVE LOGIC



$3 = \overline{1 + 2}$

NEGATIVE LOGIC

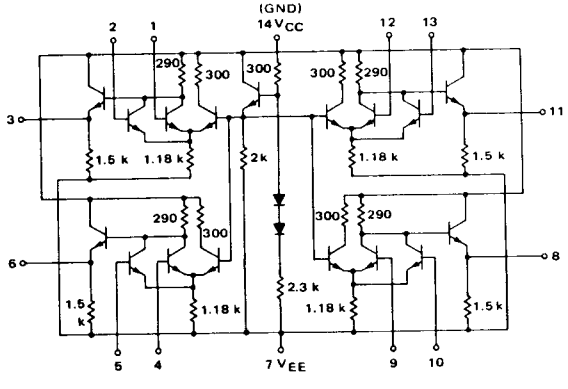


$3 = \overline{1 \cdot 2}$

DC Input Loading Factor = 1
DC Output Loading Factor = 25

Power Dissipation: MC1010/MC1210 – 115 mW typical
MC1011/MC1211 – 95 mW typical
MC1012/MC1212 – 65 mW typical

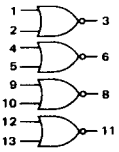
MC1010/MC1210 CIRCUIT SCHEMATIC



MC1011/MC1211
Omit pulldown resistors on pins 3 and 6

MC1012/MC1212
Omit all output pulldown resistors

Resistor values are nominal.



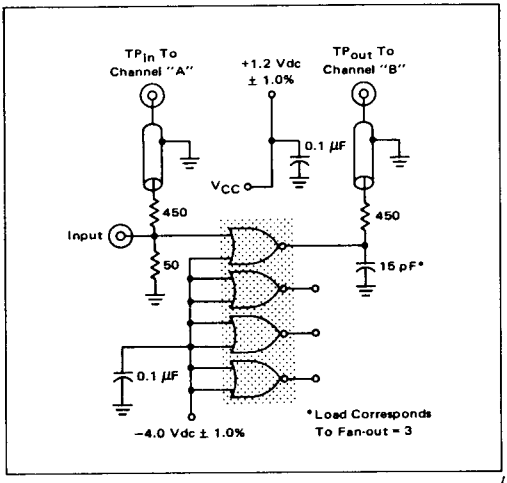
ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Outputs without pull-down resistors are tested with a 1.5 kΩ resistor to V_{EE}.

Characteristic	Symbol	Pin Under Test	MC1210-1212 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC1010-1012 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	I_E	7														
MC1210/MC1010			-	-	-	32	-	-	mAdc	-	-	-	32	-	-	mAdc
MC1211/MC1011			-	-	-	26	-	-		-	-	-	26	-	-	
MC1212/MC1012			-	-	-	18	-	-		-	-	-	18	-	-	
Input Current	I_{in}	1	-	-	-	100	-	-	μAdc	-	-	-	100	-	-	μAdc
		2	-	-	-	100	-	-	μAdc	-	-	-	100	-	-	μAdc
Input Leakage Current	I_R	Inputs*	-	-	-	0.2	-	1.0	μAdc	-	-	-	0.2	-	1.0	μAdc
"NOR" Logical "1" Output Voltage†	V_{OH}†	3	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
		3	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"NOR" Logical "0" Output Voltage	V_{OL}	3	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
		3	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
Switching Times			Typ	Max	Typ	Max	Typ	Max		Typ	Max	Typ	Max	Typ	Max	
Propagation Delay (Fan-Out = 3)	t_{1+3-}	3	4.0	7.5	4.5	7.5	6.0	9.0	ns	4.0	7.5	4.5	7.5	5.5	8.5	ns
	t_{1-3+}		5.0	7.0	5.0	7.0	6.0	9.0		5.0	7.0	5.0	7.0	5.5	8.0	
(Fan-Out = 15)	t_{1+3-}		18	-	18	-	22	-		18	-	18	-	20	-	
	t_{1-3+}		6.0	-	6.0	-	9.0	-		6.0	-	6.0	-	7.0	-	
Rise Time (Fan-Out = 3)	t_{3+}		4.0	7.5	4.0	7.0	5.0	8.0		4.0	7.0	4.0	7.0	4.5	7.5	
Fall Time (Fan-Out = 3)	t_{3-}		6.0	8.5	6.0	8.0	7.0	10		6.0	8.0	6.0	8.0	6.5	9.0	

* Individually test each input using the pin connections shown.
† V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA).

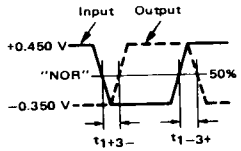
SWITCHING TIME TEST CIRCUIT @ 25°C



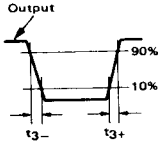
@Test Temperature		TEST VOLTAGE/CURRENT VALUES Vdc ±1.0%				mAdc
		$V_{IL\ min}$ to $V_{IL\ max}$	$V_{IH\ min}$ to $V_{IH\ max}$	$V_{IH\ max}$	V_{EE}	I_L
MC1210-1212	−55°C	-5.2 to -1.405	-1.165 to -0.825	-	-5.2	-2.5
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5
	+125°C	-5.2 to -1.205	-0.875 to -0.530	-	-5.2	-2.5
MC1010-1012	0°C	-5.2 to -1.350	-1.070 to -0.740	-	-5.2	-2.5
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5
	+75°C	-5.2 to -1.260	-0.950 to -0.615	-	-5.2	-2.5

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: $V_{IL\ min}$ to $V_{IL\ max}$	$V_{IH\ min}$ to $V_{IH\ max}$	$V_{IH\ max}$	V_{EE}	I_L	V_{CC} (Gnd)
Power Supply Drain Current MC1210/MC1010 MC1211/MC1011 MC1212/MC1012	I_E	7	- - -	- - -	- - -	1, 2, 4, 5, 7, 9, 10, 12, 13	- - -	14
Input Current	I_{in}	1 2	- -	- -	1 2	2, 4, 5, 7, 9, 10, 12, 13 1, 4, 5, 7, 9, 10, 12, 13	- -	14 14
Input Leakage Current	I_R	Inputs*	-	-	-	1, 2, 4, 5, 7, 9, 10, 12, 13	-	14
"NOR" Logical "1" Output Voltage†	V_{OH}†	3 3	1 2	- -	-	2, 4, 5, 7, 9, 10, 12, 13 1, 4, 5, 7, 9, 10, 12, 13	3 3	14 14
"NOR" Logical "0" Output Voltage	V_{OL}	3 3	- -	1 2	-	2, 4, 5, 7, 9, 10, 12, 13 1, 4, 5, 7, 9, 10, 12, 13	- -	14 14
Switching Times			Pulse In	Pulse Out		V_{EE} = −4.0 Vdc		(+1.2V)
Propagation Delay (Fan-Out = 3)	t_{1+3-} t_{1-3+}	3	1	3	-	2, 4, 5, 7, 9, 10, 12, 13	-	14
(Fan-Out = 15)	t_{1+3-} t_{1-3+}				-		-	
Rise Time (Fan-Out = 3)	t_{3+}				-		-	
Fall Time (Fan-Out = 3)	t_{3-}				-		-	

PROPAGATION DELAY



RISE AND FALL TIMES



Input Pulse t_r and t_f = 5.0 ± 0.5 ns

Switching waveforms shown for pulse in on pin 1 and pulse out on pin 3, however all other input-output combinations will meet the limits specified.

SWITCHING TIME WAVEFORMS

APPLICATIONS INFORMATION

The MC1010-1012/MC1210-1212 quad 2-input NOR gates are very useful in building more complex functions. For example, two R-S flip-flops may be obtained by cross-coupling gates, or a single gated R-S flip-flop may be obtained (see diagram below).

Dual clocked R-S flip-flops are available in MECL II (see flip-flop section). The quad 2-input gate may also be used as a dual exclusive OR or NOR by ORing the outputs as shown below.

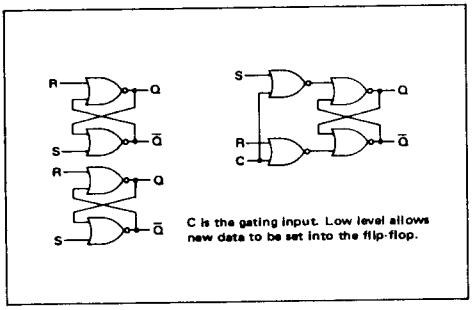


FIGURE 1 - FLIP-FLOPS OBTAINED BY USING MC1010-1012/MC1210-1212 GATES

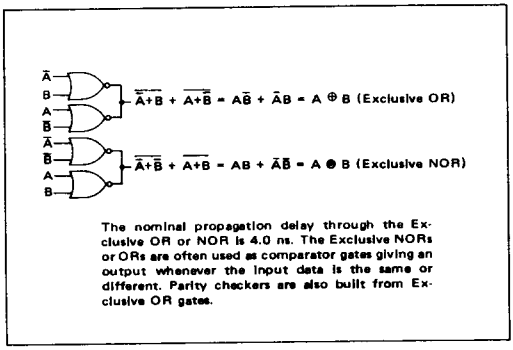


FIGURE 2 - DUAL EXCLUSIVE "OR" or "NOR" GATES