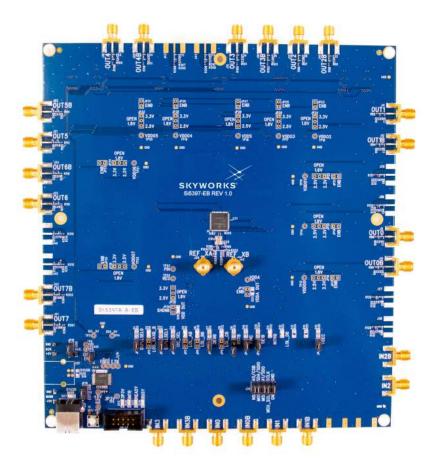


UG353: Si5397 Evaluation Board User's Guide

The Si5397 EVB is used for evaluating the Si5397 Any-Frequency, Any-Output, Jitter-Attenuating Clock Any-Frequency, Any-Output, Jitter-Attenuating Clock Multiplier. There are two different EVBs for the Si5397. There is a Grade A (external XTAL version) and Grade J (internal XTAL version). This user guide is intended for all versions of the Si5397 EVBs. The term Si5397 EVB is inclusive of the two different evaluation boards. The device grade and revision is distinguished by a white 1 inch x 0.187 inch label installed in the lower left hand corner of the board. In the example below, the label "SI5397A-A-EB" indicates the evaluation board has been assembled with an Si5397 device, Grade A, Revision A, installed. (For ordering purposes only, the terms "EB" and "EVB" refer to the board and the kit, respectively. For the purpose of this document, the terms are synonymous in context.)



KEY FEATURES

- Si5397A-A-EB for evaluating external reference versions Si5397A/B/C/D
- Si5397J-A-EB for evaluating internal reference versions Si5397J/K/L/M
- Powered from USB port or external +5 V power supply via screw terminals
- Onboard 48 MHz XTAL allows standalone or holdover mode of operation on the Si5397
- ClockBuilder Pro[®] (CBPro) GUI programmable VDD supply allows device supply voltages of 3.3, 2.5, or 1.8 V
- CBPro GUI programmable VDDO supplies allow each of the eight outputs to have its own supply voltage selectable from 3.3, 2.5, or 1.8 V
- CBPro GUI allows control and measurement of voltage, current, and power of VDD and all eight VDDO supplies
- Status LEDs for power supplies and control/ status signals of the Si5397
- SMA connectors for input clocks, output clocks and optional external timing reference clock to be used on external reference grade only

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UG353: Si5397 Evaluation Board User's Guide • Functional Block Diagram

1. Functional Block Diagram

Below is a functional block diagram of the Si5397 EVB. Keep in mind that the Grade J does not use an external XTAL or reference and do not use the XA/XB pins. This evaluation board can be connected to a PC via the main USB connector for programming, control, and monitoring. See 3. Quick Start or 10.3 Overview of ClockBuilder Pro Applications for more information.

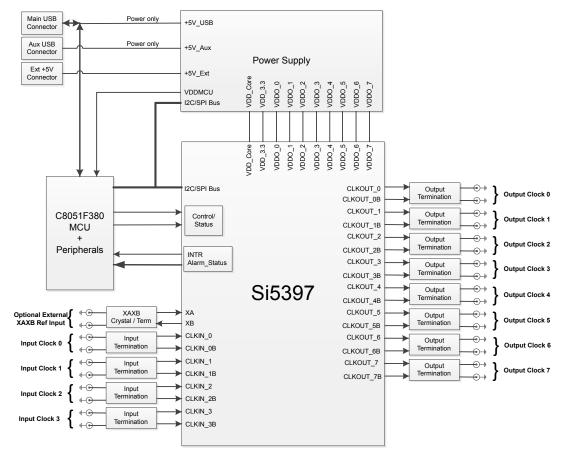


Figure 1.1. Si5397 EVB Functional Block Diagram

UG353: Si5397 Evaluation Board User's Guide • Si5397-EVB Support Documentation and ClockBuilder Pro Software

2. Si5397-EVB Support Documentation and ClockBuilder Pro Software

All Si5397 EVB schematics, BOMs, User's Guides, and software can be found online:

https://www.skyworksinc.com/-/media/Skyworks/SL/documents/public/data-sheets/si5397-96-a-datasheet.pdf

UG353: Si5397 Evaluation Board User's Guide • Quick Start

3. Quick Start

- 1. Install the ClockBuilder Pro desktop software from https://www.skyworksinc.com/en/application-pages/clockbuilder-pro-software.
- 2. Connect a USB cable from the Si5397 EVB to the PC where the software was installed.
- 3. Confirm jumpers are installed as shown in Table 4.1 Si5397 EVB Jumper Defaults¹ on page 6.
- 4. Launch the ClockBuilder Pro Software.
- 5. You can use ClockBuilder Pro to create, download, and run a frequency plan on the Si5397-EVB.
- 6. Find the Si5397 data sheet here: https://www.skyworksinc.com/-/media/Skyworks/SL/documents/public/data-sheets/si5397-96-adatasheet.pdf

4. Jumper Defaults

Location	Туре	l= Installed 0 = Open	Location	Туре	I = Installed 0 = Open
JP1	2-pin	I	JP23	2-pin	0
JP2	2-pin	0	JP24	2-pin	0
JP3	2-pin	I	JP25	2-pin	0
JP4	2-pin	I	JP26	2-pin	0
JP5	2-pin	0	JP27	2-pin	0
JP6	2-pin	0	JP28	2-pin	0
JP7	2-pin	I	JP29	2-pin	0
JP8	2-pin	0	JP30	2-pin	0
JP9	2-pin	0	JP31	2-pin	0
JP10	2-pin	I	JP32	2-pin	0
JP13	2-pin	0	JP33	2-pin	0
JP14	2-pin	I	JP34	2-pin	0
JP15	3-pin	all open	JP35	2-pin	0
JP16	3-pin	1 to 2	JP36	2-pin	0
JP17	2-pin	0	JP38	3-pin	All Open
JP18	2-pin	0	JP39	2-pin	0
JP19	2-pin	0	JP40	2-pin	I
JP20	2-pin	0	JP41	2-pin	I
JP21	2-pin	0	J36	5 x 2 Hdr	All 5 installed
JP22	2-pin	0			

Table 4.1. Si5397 EVB Jumper Defaults¹

1. Refer to the Si5397 EVB schematics for the functionality associated with each jumper.

5. Status LEDs

Location	Silkscreen	Color	Status Function Indication
D27	5VUSBMAIN	Blue	Main USB +5 V present
D22	3P3V	Blue	DUT +3.3 V is present
D26	VDD DUT	Blue	DUT VDD voltage present
D25	INTR	Red	MCU INTR (Interrupt) active
D21	READY	Green	MCU Ready
D24	BUSY	Green	MCU Busy
D2	LOS_XAXB_B	Blue	Loss of Signal at XAXB input
D5	LOL_AB	Blue	Lossof Lock - DSPLL A
D6	LOL_BB	Blue	Lossof Lock - DSPLL B
D8	LOL_CB	Blue	Lossof Lock - DSPLL C
D11	INTRB	Blue	Si5397 Interrupt Active
D12	LOL_DB	Blue	Loss of Lock _ DSPLL D

D27, D22, and D26 are illuminated when USB +5 V, Si5397 +3.3 V, and Si5397 Vcore supply voltages, respectively, are present. D25, D21, and D24 are status LEDs showing onboard MCU activity. D2 indicates loss of signal at XAXB input (either crystal osc or external reference). D5, D6, D8, D12 indicate loss of lock for one of four internal DSPLLs (A–D). D11 indicates the Si5397 interrupt output is active (as configured by Si5397 register programming). LED locations are highlighted below with LED function name indicated on board silkscreen.

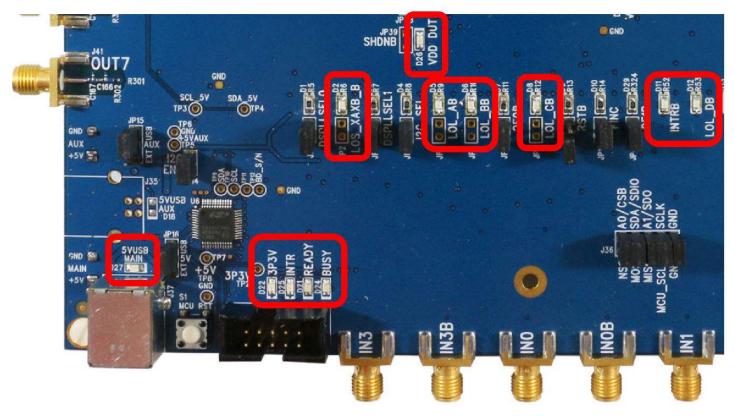


Figure 5.1. Status LEDs

UG353: Si5397 Evaluation Board User's Guide • External Reference Input (XA/XB)

6. External Reference Input (XA/XB)

An external timing reference (48 MHz XTAL) is used in combination with the internal oscillator to produce an ultra-low jitter reference clock for the DSPLL and for providing a stable reference for the free-run and holdover modes. The Si5397A-A-EVB can accommodate an external reference clock instead of a crystal. To evaluate the device with an external REFCLK, C111 and C113 must be populated and XTAL Y1 removed (see figure below). The REFCLK can then be applied to SMA connectors J39 and J40. In the case of the Si5397J-A-EVB (the internal reference grade), there will be no external xtal supplied on the board and no input from Ref_XA and Ref_XB. In this case, it is advised that R197 and R202 be removed.

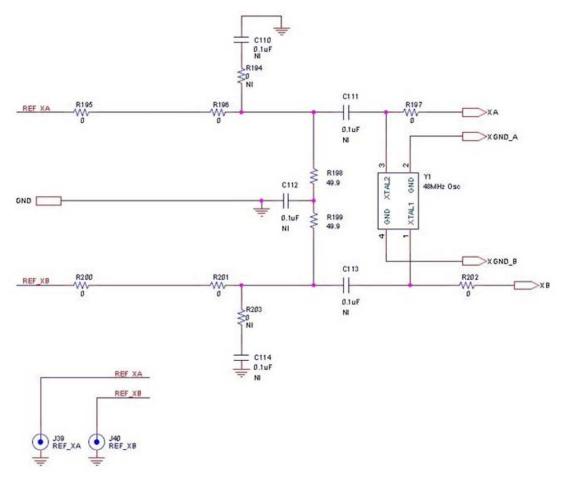


Figure 6.1. External Reference Input Circuit

UG353: Si5397 Evaluation Board User's Guide • Clock Input Circuits (INx/INxB)

7. Clock Input Circuits (INx/INxB)

The Si5397 EVB has eight SMA connectors (IN0, IN0B–IN3, IN3B) for receiving external clock signals. All input clocks are terminated as shown below. Note that input clocks are ac-coupled and 50 Ω terminated. This represents four differential input clock pairs. Single-ended clocks can be used by appropriately driving one side of the differential pair with a single-ended clock. For details on how to configure inputs as single-ended, please refer to the Si5397 data sheet.

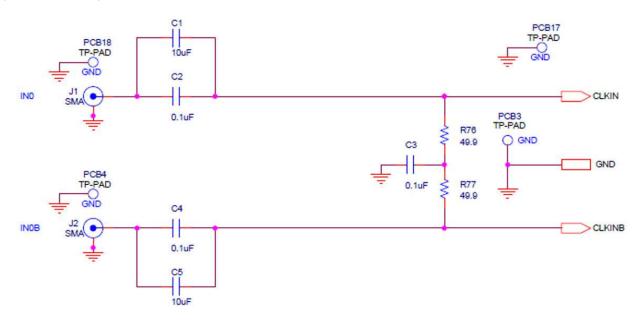


Figure 7.1. Input Clock Termination Circuit

UG353: Si5397 Evaluation Board User's Guide • Clock Output Circuits (OUTx/OUTxB)

8. Clock Output Circuits (OUTx/OUTxB)

Each of the sixteen output drivers (eight differential pairs, OUT0/OUT0B—OUT7/OUT7B) is ac-coupled to its respective SMA connector. The output clock termination circuit is shown below. The output signal will have no dc bias. If dc coupling is required, the ac coupling capacitors can be replaced with a resistor of appropriate value. The Si5397 EVB provides pads for optional output termination resistors and/or low-frequency capacitors. Note that components with a schematic "NI" designation are not normally populated on the Si5397 EVB and provide locations on the PCB for optional dc/ac terminations by the end user.

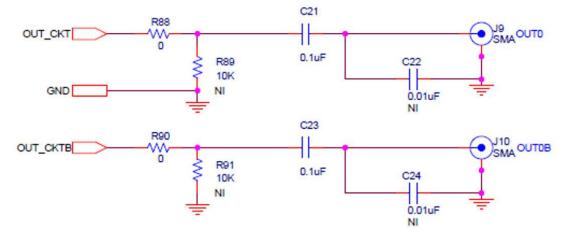


Figure 8.1. Output Clock Termination Circuit

UG353: Si5397 Evaluation Board User's Guide • Installing ClockBuilder Pro Desktop Software

9. Installing ClockBuilder Pro Desktop Software

To install the CBPro software on any **Windows 7** (or above) PC, go to https://www.skyworksinc.com/en/application-pages/clockbuilderpro-software and download the ClockBuilder Pro software.

Installation instructions and User's Guide for ClockBuilder Pro can be found at the download link shown above.

UG353: Si5397 Evaluation Board User's Guide • Using the Si5397 EVB

10. Using the Si5397 EVB

10.1 Connecting the EVB to Your Host PC

Once ClockBuilderPro software is installed, connect to the EVB with a USB cable as shown in the figure below:

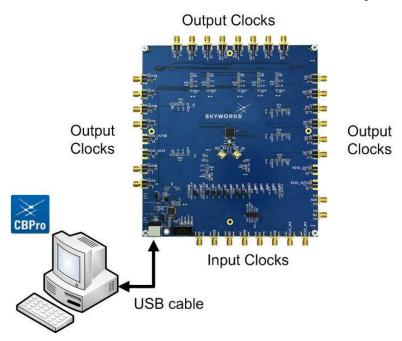


Figure 10.1. EVB Connection Diagram

10.2 Additional Power Supplies

The Si5397 EVB comes preconfigured with jumpers installed at JP15 and JP16 (pins1–2 in both cases) in order to select "USB". These jumpers, together with the components installed, configure the evaluation board to obtain all +5 V power solely through the main USB connector at J37. This setup is the default configuration and should normally be sufficient.

The following figure shows the correct installation of the jumper shunts at JP15 and JP16 for default or standard operation.

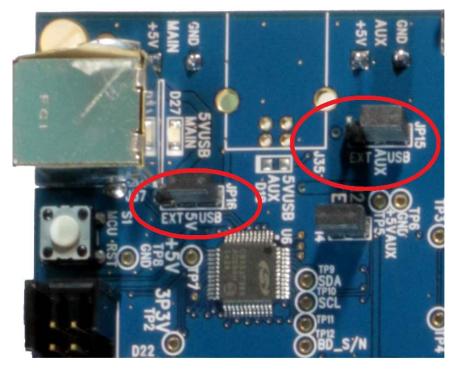


Figure 10.2. JP15–JP16 Standard Jumper Shunt Installation

The general guidelines for single USB power supply operation are as follows:

- Use either a USB 3.0 or USB 2.0 port. These ports are specified to supply 900 mA and 500 mA, respectively, at +5 V.
- If you are working with a USB 2.0 port and you are current limited, turn off enough DUT output voltage regulators to drop the total DUT current ≤470 mA. (Note: USB 2.0 ports may supply > 500 mA. Provided the nominal +5 V drops gracefully by less than 10%, the EVB will still work.)
- If you are working with a USB 2.0 and you are current limited and need all output clock drivers enabled, reconfigure the EVB to drive the DUT output voltage regulators from an external +5 V power supply as follows:
 - Connect an external +5 V power supply to terminal block J33 on the back side of the PCB.
 - Move the jumper at JP15 from pins 1-2 USB to pins 2-3 EXT.

10.3 Overview of ClockBuilder Pro Applications

Note: The following instructions and screen captures may vary slightly depending on your version of ClockBuilder Pro. The ClockBuilder Pro installer will install **two** main applications:

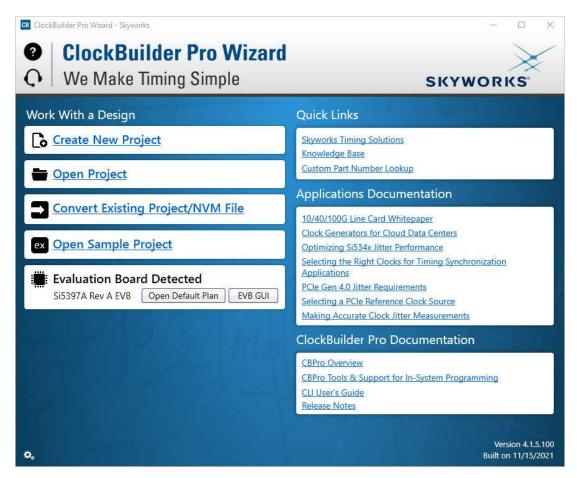


Figure 10.3. Application #1: ClockBuilder ProWizard

Use the CBPro wizard to:

- · Create a new design
- · Review or edit an existing design
- · Export: create in-system programming

Ĥ								
fo	DUT SPI	DUT Settings Editor	DUT Register Editor	Regulators	All Voltages	GPIO	Status Registers	 Control Registers
			Voltage	Curren	t Powe	r		Soft Reset and Calibration
	VDD	1.80V	1.792 V	158 r	nA 283	mW [Read	SOFT_RST_ALL
	VDDA	3.30V	on 3.300 V	123 r	nA 406	mW [Read	SOFT_RST_PLLA
	VDDS	5 3.30V	3.284 V	7 r	nA 23	mW [Read	SOFT_RST_PLLB
	VDDO		Off 0.009 V	0 r		mW [Read	SOFT_RST_PLLC
	VDDOI		Off 0.003 V	0 r		mW [Read	SOFT_RST_PLLD
	VDDO2		Off 0.001 V	0 r		mW [Read	Hard Reset, Sync, & Power Dov
	VDDO2		0.001 0.001 V	0 r		mW [Read	HARD_RST
	VDD03		n 1.796 V	0 r		mw [Read	SYNC
	VDDO		n 1.794 V	0 r		mw [Read	PDN: 0
	VDDO		Off 0.004 V	0 r		mW [Read	Frequency Adjust
	VDD07		Off 0 V	0 r		mW [Read	FINC
		- Select Voltage	Total	288 r	mA 0.712	w [Read All	FDEC
	Output upplies –		wer Off Co	mpare Desig	n Estimates to	o Measu	rements	
9		_						
Itere	d 🔽 4	Auto Scroll: On	Insert Marker	Clear	Copy to Clipb	oard	Pause	
mes	tamp Sc	ource Message						
): <mark>1</mark> 5:	18.502 EV		leasure_Regulator(reg		D_7) => Volt	age_Reg	: 0.000V, Voltage_Pin:	

Figure 10.4. Application #2: EVBGUI

Use the EVB GUI to:

- Download configuration to EVB's DUT (Si5397)
- Control the EVB's regulators
- · Monitor voltage, current, and power on the EVB

10.4 Common ClockBuilderPro Workflow Scenarios

There are three common workflow scenarios when using CBPro and the Si5397 EVB. These workflow scenarios are:

- · Workflow Scenario 1: Testing a Skyworks-Created Default Configuration
- Workflow Scenario 2: Modifying the Default Skyworks-Created Device Configuration
- · Workflow Scenario 3: Testing a User-Created Device Configuration

Each workflow scenario is described in more detail in the following sections.

10.5 Workflow Scenario 1: Testing a Skyworks Default Configuration

The flow for using the EVB GUI to initialize and control a device on the EVB is as follows:

Once the PC and EVB are connected, launch ClockBuilderPro by clicking this icon on your PC's desktop:



Figure 10.5. ClockBuilderPro Desktop Icon

If an EVB is detected, click on the "Open Default Plan" button on the Wizard's main menu. CBPro automatically detects the EVB and device type.

CB Clock	Builder Pro Wizard - Skyworks
8 Q	ClockBuilder Pro Wizard We Make Timing Simple
Worl	With a Design
Co	Create New Project
	<u>Open Project</u>
3	Convert Existing Project/NVM File
ex	Open Sample Project
	Evaluation Board Detected Si5397A Rev A EVB Open Default Plan EVB GUI

Figure 10.6. Open Default Plan

UG353: Si5397 Evaluation Board User's Guide • Using the Si5397 EVB

Once you open the default plan (based on your EVB model number), a popup will appear:

CB Clo	ockBuilder Pro v4.1.5.100	—		×
A	Write Design to EVB?			
	The EVB may be out-of-sync with your design. Wou your design to the EVB?	ld you li	ke to wr	ite
	Yes No			

Figure 10.7. Write Design to EVB Dialog

Select "Yes" to write the default plan to the Si5397 device mounted on your EVB. This ensures the device is completely reconfigured per the Skyworks default plan for the DUT type mounted on the EVB.

Writing Si5397 Desig	n to EVB	
Address 0x0270		

Figure 10.8. Writing Design Status

After CBPro writes the default plan to the EVB, click on "Open EVB GUI" as shown below:

CB Si5397 EVB Default Configuration - ClockBuilder Pro	X
ClockBuilder Pro v4.1.5.100 🍫	SKYWORKS
Design Dashboard 🔻	Configuring Si5397A Rev A
EVB sample plan for Si5397 has been loaded. You can make edits to Image: Configuration with Wizard Design ID & Notes · Host Interface · Reference · Free Run · Inputs · Input Select · Outputs · DCO · Hitless Switching Assistant · DSPLL · LOS · OOF · LOL · INTR	the EVB's configuration using the interactive Wizard. Evaluation Board Detected Si5397A Rev A EVB Write Design to EVB Open EVB GUI

Figure 10.9. Open EVB GUI

The EVB GUI will appear. Note that all power supplies will be set to the values defined in the device's default CBPro project file created by Skyworks, as shown in the following figure:

fo	DUT SPI	DUT Settings Editor	DUT Register Editor	Regulators	All Voltages	GPIO	Status Registers	
			Voltage	Current	t Power	0		
	VDD	0 1.80V 📳 🚺	Dn 1.790 V	314 n	nA 562 r	mW [Read	
	VDDA	3.30V	0n 3.296 V	128 n	nA 422 r	mW [Read	
	VDDS	5 3.30V 🕎 🔽	0n 3.279 V	7 n	nA 23 r	nW [Read	
	VDDO	2.50V 📳 🚺	2.504 V	16 n	nA 40 r	nW [Read	
	VDDO1	2.50V 🔽 🚺	2.497 V	18 n	nA 45 r	mW [Read	
	VDDO2	2 2.50V 🔽 🔽	2.488 V	16 n	nA 40 r	nW [Read	
	VDDO	3 2.50V 🕎 🔽	2.491 V	18 n	nA 45 r	mW [Read	
	VDDO4	4 2.50V 📳 🔽	2.487 V	16 n	nA 40 r	mW [Read	
	VDDOS	5 2.50V 🔽 🔽	2.504 V	18 n	nA 45 r	mW [Read	
	VDDO	5 2.50V 🔽 🔽	2.491 V	15 n	nA 37 r	mW [Read	
	VDD07	7 2.50V 🕎 🚺	2.510 V	15 n	nA 38 r	mW [Read	
		- Select Voltage	Total	581 n	nA 1.337	w	Read All	

Figure 10.10. EVB GUI Window

10.5.1 Verify Free-Run Mode Operation

Assuming no external clocks have been connected to the INPUT CLOCK differential SMA connectors (labeled "INx/INxB") located around the perimeter of the EVB, the DUT should now be operating in free-run mode, as the DUT will be locked to the crystal in this case.

You can run a quick check to determine if the device is powered up and generating output clocks (and consuming power) by clicking on the Read All button highlighted above and then reviewing the voltage, current, and power readings for each VDDx supply.

Note: Shutting the VDD and VDDA supplies "Off" then "On" will power-down and reset the DUT. Every time you do this, to reload the Skyworks-created default plan into the DUT's register space, you must go back to the Wizard's main menu and select "Write Design to EVB" as shown below.

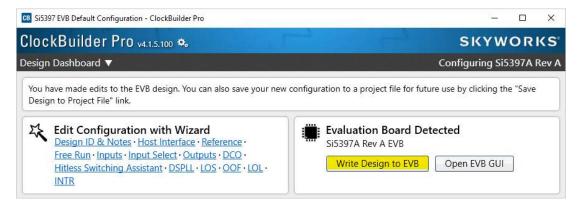


Figure 10.11. Write Design to EVB

Failure to perform this step will cause the device to read in a preprogrammed plan from its non-volatile memory (NVM). However, the plan loaded from the NVM may not be the latest plan recommended by Skyworks for evaluation.

At this point, you should verify the presence and frequencies of the output clocks (running to free-run mode from the crystal) using appropriate external instrumentation connected to the output clock SMA connectors. To verify the output clocks are toggling at the correct frequency and signal format, click on View Design Report as highlighted below.

SKYWORK
Configuring Cit2074 D
Configuring Si5397A Re
ration to a project file for future use by clicking the "Save
Evaluation Board Detected Si5397A Rev A EVB Write Design to EVB Open EVB GUI
Export You can export your configuration to a format suitable for in-system programming.
Documentation Si5397/96 Reference Manual Si5397/96 Data Sheet Si5397 EVB User's Guide
Ask for Help Have a question about your design? Click <u>here</u> to get assistance

Figure 10.12. View Design Report

Your configuration's design report will appear in a new window, as shown below. Compare the observed output clocks to the frequencies and formats noted in your default project's Design Report.

B Si5397 De	isign Report	_		\times
esign Rep	ort			
Design				
Host Int				
	ower Supply: VDD (Core)			
	ode: 4-Wire			
I2C A pins)	ddress Range: 108d to 111d / 0x6C to 0x6F (select	ed via	A0/A1	
External	Reference:			
48 MH:	z (XTAL - Crystal)			
Inputs:				
IN0:	25 MHz			
	Standard Differential and Single-ended			
	DSPLL A,B,C,D			
IN1:	25 MHz			
	Standard Differential and Single-ended			
	DSPLL A,B,C,D			
1N2:	10 MHz Standard Differential and Single-ended			
	DSPLL A,B,C,D			
TN3.	10 MHz			
100.	Standard Differential and Single-ended			
	DSPLL A,B,C,D			
Outputs:				
OUT0:	161.1328125 MHz			
	Enabled, LVDS 2.5 V			
	DSPLL A			
OUT1:	644.53125 MHz			
	Enabled, LVDS 2.5 V			
0.170	DSPLL A			
0012:	168.041015625 MHz Enabled, LVDS 2.5 V			
	DSPLL B			
OUT3:	672.1640625 MHz			-
Complete C	lipboard Save Report Ask for Help		Clos	~

Figure 10.13. Design Report Window

10.5.2 Verify Locked Mode Operation

Assuming you connect the correct input clocks to the EVB (as noted in the Design Report shown above), the DUT on your EVB will be running in "locked" mode.

10.6 Workflow Scenario 2: Modifying the Default Skyworks-Created Device Configuration

To modify the "default" configuration using the CBPro Wizard, click on the links below under "Edit Configuration with Wizard".

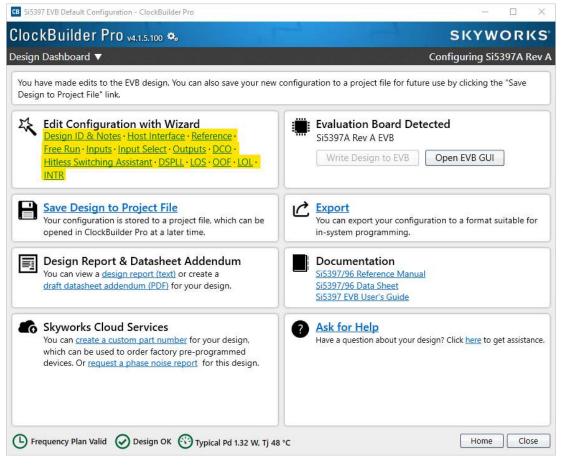


Figure 10.14. Edit Configuration with Wizard

You will now be taken to the Wizard's step-by-step menus to allow you to change any of the default plan's operating configurations.

lockBuild	ler Pro v4.1.5.100 🍫	SKYWORK
ep 1 of 14 - D	esign ID & Notes 🔻	Configuring Si5397A Re
Design ID The device has 8 i	registers, DESIGN_ID0 through DESIGN_ID7, that can be used to store a design/configuratio	n/revision identifier.
Design ID:	5397EVB (optional; max 8 characters) The string you enter here is stored as ASCII bytes in registers DESIGN_ID0 through DESI	GN_ID7.
Padding Mode:	NULL Padded If you do not enter the full 8 characters, the remaining bytes of DESIGN_IDx will be character).	padded with 0x00 bytes (aka NULL
	Space Padded If you do not enter the full 8 characters, the remaining bytes of DESIGN_IDx will be character).	padded with 0x20 bytes (space
inter anything yo	u want here. The text is stored in your project file and included in design reports and custor vord wrapped in reports, you can use newlines to start a new paragraph.	n part number datasheet addendums
nter anything yo		m part number datasheet addendum
nter anything yo		m part number datasheet addendum:
nter anything yo		m part number datasheet addendums
		m part number datasheet addendur

Figure 10.15. Design Wizard

Note that you can click on the icon on the lower left hand corner of the menu to confirm if your frequency plan is valid. After making your desired changes, you can click on Write to EVB to update the DUT to reconfigure your device real-time. The Design Write status window will appear each time you make a change.

Writing Si5397 Design to EVB				
	Design to EVB	Design to EVB	Design to EVB	

Figure 10.16. Writing Design Status

10.7 Workflow Scenario 3: Testing a User-Created Device Configuration

To test a previously created user configuration, open the CBPro Wizard by clicking on the icon on your desktop and then selecting Open Design Project File.

CB ClockBuilder Pro Wizard - Skyworks	— 🗆 X
 ClockBuilder Pro Wizard We Make Timing Simple 	SKYWORKS
Work With a Design	Quick Links
Create New Project	Skyworks Timing Solutions Knowledge Base
🖶 <mark>Open Project</mark>	Custom Part Number Lookup
Convert Existing Project/NVM File	Applications Documentation 10/40/100G Line Card Whitepaper
ex Open Sample Project	Clock Generators for Cloud Data Centers Optimizing Si534x Jitter Performance
Si5397A Rev A EVB Open Default Plan EVB GUI	Selecting the Right Clocks for Timing Synchronization Applications PCIe Gen 4.0 Jitter Requirements Selecting a PCIe Reference Clock Source Making Accurate Clock Jitter Measurements
ALTERN TOPS - DAY	ClockBuilder Pro Documentation
	CBPro Overview CBPro Tools & Support for In-System Programming CLI User's Guide Release Notes
Q ₀	Version 4.1.5.100 Built on 11/15/2021

Figure 10.17. Open Design Project File

Locate your CBPro design file (*.slabtimeproj or *.sitproj file).design file in the Windows file browser.

CB Open CBPro Project File				×
\leftarrow \rightarrow \checkmark \uparrow \square \rightarrow This i	PC > Documents > CBPro	ٽ ~	Search CBPro	م
Organize 👻 New folder			-== -==	• 🔳 🕐
A Quick access	Name	Date modified	Туре	Size
	Si5397-RevA-5397EVB-Project	12/16/2021 10:35 AM	Skyworks Timing	14 KB
 OneDrive - Persor This PC 3D Objects Desktop Documents 				
File nam	ne: Si5397-RevA-5397EVB-Project	~	Skyworks Timing P Open	roject V Cancel

Figure 10.18. Browse to Project File

Select "Yes" when the WRITE DESIGN to EVB popup appears:

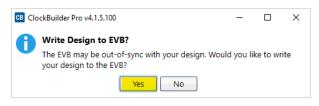


Figure 10.19. Write Design to EVB Dialog

The progress bar will be launched. Once the new design project file has been written to the device, verify the presence and frequencies of your output clocks and other operating configurations using external instrumentation.

10.8 Exporting the Register Map File for Device Programming by a Host Processor

You can also export your configuration to a file format suitable for in-system programming by selecting Export as shown below:

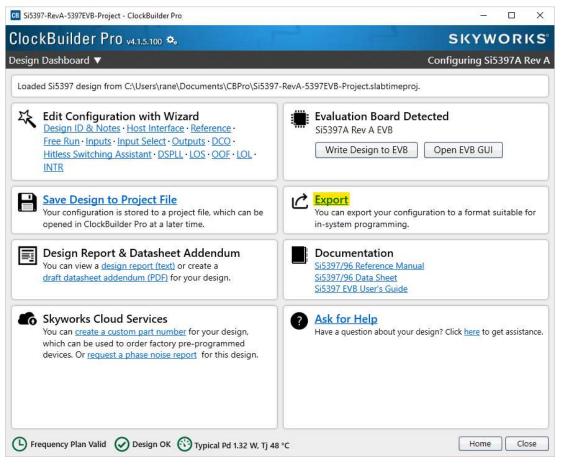


Figure 10.20. Export Register Map File

You can now write your device's complete configuration to file formats suitable for in-system programming:

ntroduction	Register File	Settings File	Multi-Project Register/Set	tings Regmap			_
About Regi	ster Export						_
This export configuratio		e registers that	t need to be written to the	Si5397 to achieve	your design	/	
	l line version o rompt to learr		ailable. Type <mark>CBProProjec</mark>	tRegistersExport -	-help from a	1	
Options							
Export Type	:						
Each and d	ata fields.	S	le lata pair in hexadecimal fo	rmat. A comma sej	parates the a	ddress	
The r	le Header File egister write se directly in firm		ressed in C code via an ar	ray of address,data	pairs. This c	an be	
If check	by the # chara	tional header v	will be included at the top der will contain some basi				
Include Certain This ens the dow	pre- and post- control registe ures the device	rs must be wri e is stable duri	egister writes tten before and after writi ng configuration downloa urn inclusion of this seque	d and resumes nor	mal operatio	on after	J

Figure 10.21. Export Settings

UG353: Si5397 Evaluation Board User's Guide • Writing a New Frequency Plan or Device Configuration to Non-Volatile Memory (OTP)

11. Writing a New Frequency Plan or Device Configuration to Non-Volatile Memory (OTP)

Note: Writing to the device non-volatile memory (OTP is **NOT** the same as writing a configuration into the Si5397 using Clock-BuilderPRo on the Si5397 EVB. Writing a configuration into the EVB from ClockBuilderPro is done using Si5397 RAM space and can be done a virtually unlimited numbers of times. Writing to OTP is limited as described below.

Refer to the Si5397/96 Reference Manual and device data sheets for information on how to write a configuration to the EVB DUT's non-volatile memory (OTP). The OTP can be programmed a maximum of **two** times only. Care must be taken to ensure the desired configuration is valid when choosing to write to OTP.

UG353: Si5397 Evaluation Board User's Guide • Serial Device Communications

12. Serial Device Communications

12.1 Onboard SPI Support

The MCU onboard the Si5397 EVB communicates with the Si5397 device through a 4-wire SPI (Serial Peripheral Interface) link. The MCU is the SPI master and the Si5397 device is the SPI slave. The Si5397 device can also support a 2-wire I²C serial interface, although the Si5397 EVB does NOT support the I²C mode of operation. SPI mode was chosen for the EVB because of the relatively higher speed transfers supported by SPI vs. I²C.

12.2 External I²C Support

I²C can be supported if driven from an external I²C controller. The serial interface signals between the MCU and Si5397 pass through shunts loaded on header J36. These jumper shunts must be installed in J36 for normal EVB operation using SPI with CBPro. If testing of I²C operation via external controller is desired, the shunts in J36 can be removed thereby isolating the onboard MCU from the Si5397 device. The shunt at J4 (I2C_SEL) must also be removed to select I²C as Si5397 interface type. An external I²C controller connected to the Si5397 side of J36 can then communicate to the Si5397 device. For more information on I²C signal protocol, refer to the Si5397 data sheet.

The figure below illustrates the J36 header schematic. J36 even numbered pins (2, 4, 6, etc.) connect to the Si5397 device, and the odd numbered pins (1, 3, 5, etc.) connect to the MCU. Once the jumper shunts have been removed from J36 and J4, I²C operation should use J36 pin 4 (DUT_SDA_SDIO) as the I2CSDA and J36 pin 8 (DUT_SCLK) as the I2CSCLK. Note that the external I²C controller will need to supply its own I²C signal pull-upresistors.

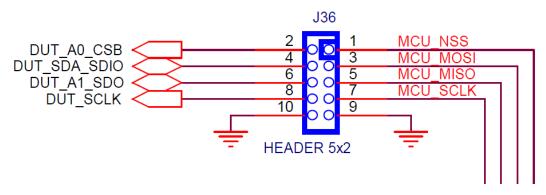


Figure 12.1. Serial Communications Header J36

UG353: Si5397 Evaluation Board User's Guide • Si5397 EVB Schematic, Layout, and Bill of Materials (BOM)

13. Si5397 EVB Schematic, Layout, and Bill of Materials (BOM)

The Si5397 EVB Schematic, Layout, and Bill of Materials (BOM) can be found online at: https://www.skyworksinc.com/-/media/Sky-works/SL/documents/public/data-sheets/si5397-96-a-datasheet.pdf

Note: Please be aware that the Si5397 EVB schematic is in OrCad Capture *hierarchical format* and not in a typical "flat" schematic format.

This document supports the evaluation board silkscreened Si5397 EVB for the following configurations as described in the table below. The data sheet documents the different Si5397 grades.

Config #	Eval Board Label	Si5397		Notes
		Grade	Revision	
1	Si5397A-A-EB	A	A	Crystal and related components installed.
2	Si5397J-A-EB	J	J	Crystal and related components not installed. Only the DUT and label differ versus Si5397J-A-EB.

Table 13.1. Evaluation Board Configurations

SKYWORKS

ClockBuilder Pro

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