

- Hamming code generation
- Extended 100E VEE range of -4.2V to -5.5V
- 8-bit wide
- Expandable for more width
- Provides parity register
- Fully compatible with industry standard 10KH, 100K ECL levels
- Internal 75KΩ input pulldown resistors
- Fully compatible with Motorola MC10E/100E193
- Available in 28-pin PLCC package

The SY10/100E193 are error detection and correction (EDAC) circuits designed for use in new, high-performance ECL systems. The E193 generates hamming parity codes on an 8-bit word as shown in the block diagram. The P5 output gives the parity of the whole word. PGEN provides word parity after Odd/Even parity control and gating with the BPAR input. PGEN also feeds into a 1-bit shiftable register for use as part of a scan ring.

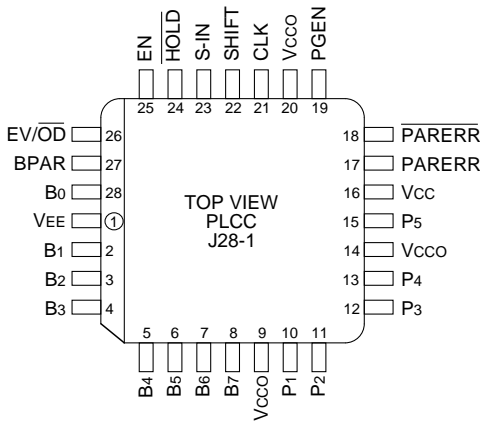
The combinatorial part of the device generates the same code pattern as the Motorola MC10193.

Used in conjunction with 12-bit parity generators, such as the E160, a SECDED (single error correction, double error detection) error system can be designed for a multiple of an 8-bit word.

PIN NAMES

Pin	Function
B0-B7	Check Bit Inputs
BPAR	Check Bit Parity Input
EV/OD	Even/Odd Parity Select
EN	Parity Enable
HOLD	Syndrome Hold Input
S-IN	Syndrome Bit Input
SHIFT	Syndrome Bit Shift
CLK	Clock Input
P1-P5	Parity Output
PGEN	Parity Generate Output
PARERR/PARERR	Parity Error Output
Vcco	Vcc to Output

PACKAGE/ORDERING INFORMATION



28-Pin PLCC (J28-1)

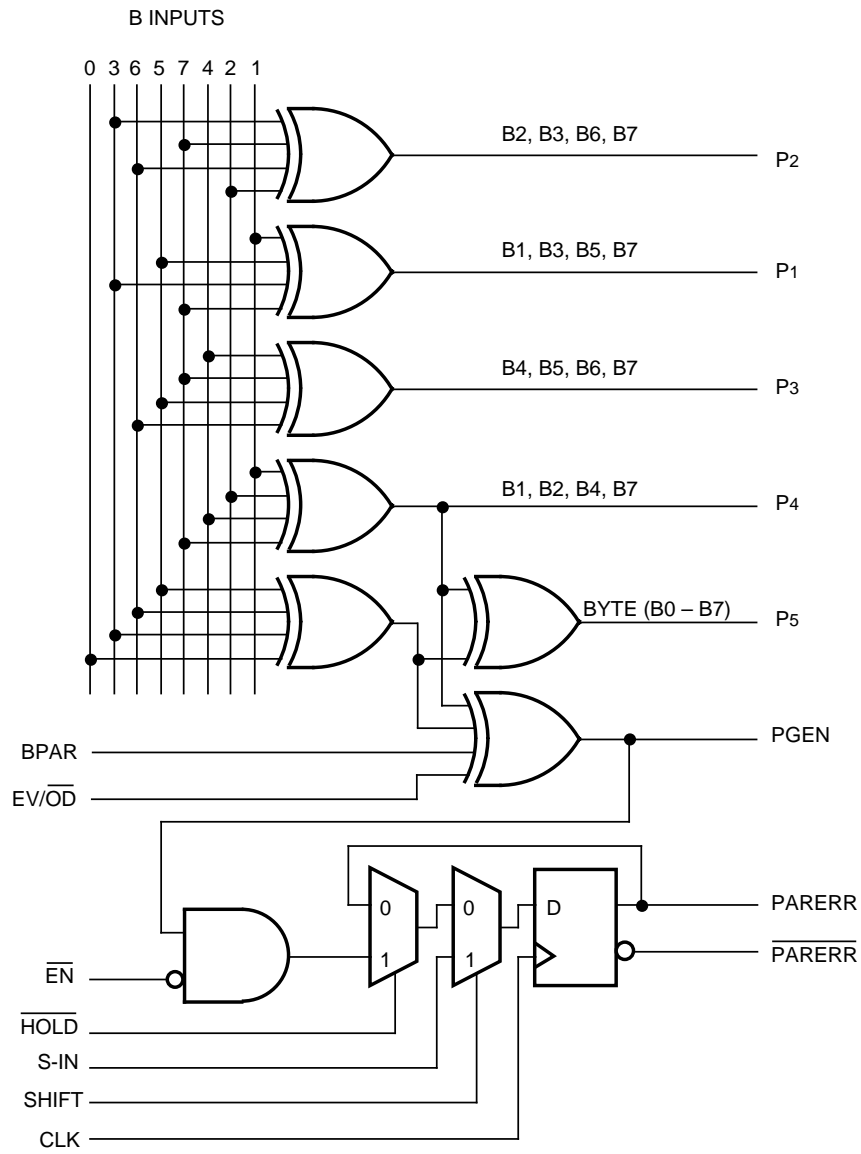
Ordering Information⁽¹⁾

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY10E193JC	J28-1	Commercial	SY10E193JC	Sn-Pb
SY10E193JCTR ⁽²⁾	J28-1	Commercial	SY10E193JC	Sn-Pb
SY100E193JC	J28-1	Commercial	SY100E193JC	Sn-Pb
SY100E193JCTR ⁽²⁾	J28-1	Commercial	SY100E193JC	Sn-Pb
SY10E193JZ ⁽³⁾	J28-1	Commercial	SY10E193JZ with Pb-Free bar-line indicator	Matte-Sn
SY10E193JZTR ^(2, 3)	J28-1	Commercial	SY10E193JZ with Pb-Free bar-line indicator	Matte-Sn
SY100E193JZ ⁽³⁾	J28-1	Commercial	SY100E193JZ with Pb-Free bar-line indicator	Matte-Sn
SY100E193JZTR ^(2, 3)	J28-1	Commercial	SY100E193JZ with Pb-Free bar-line indicator	Matte-Sn

Notes:

1. Contact factory for die availability. Dice are guaranteed at $T_A = 25^\circ\text{C}$, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

BLOCK DIAGRAM

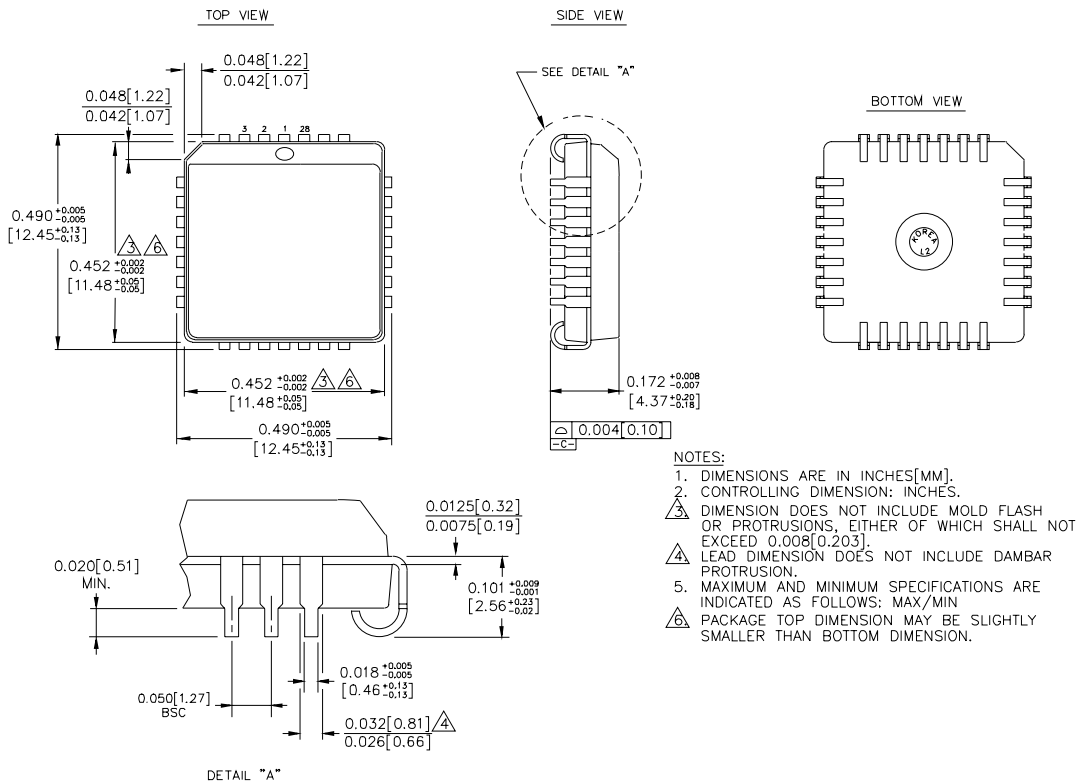


VEE = VEE (Min.) to VEE (Max.); VCC = VCCO = GND

Symbol	Parameter	TA = 0°C			TA = +25°C			TA = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I _{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	μA	—
I _{EE}	Power Supply Current	—	—	—	—	—	—	—	—	—	mA	—
	10E	—	112	134	—	112	134	—	112	134		
	100E	—	112	134	—	112	134	—	129	155		

VEE = VEE (Min.) to VEE (Max.); VCC = VCCO = GND

Symbol	Parameter	TA = 0°C			TA = +25°C			TA = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t _{PD}	Propagation Delay to Output B to P1, P2, P3, P4	350	700	1000	350	700	1000	350	700	1000	ps	—
	B to P5	400	775	1150	400	775	1150	400	775	1150		
	EV/ $\overline{\text{OD}}$, BPAR to PGEN	350	650	850	350	650	850	350	650	850		
	B to PGEN	600	1000	1450	600	1000	1450	600	1000	1450		
	CLK to PARERR	300	550	850	300	550	850	300	550	850		
t _s	Set-up Time SHIFT	400	150	—	400	150	—	400	150	—	ps	—
	S-IN	300	50	—	300	50	—	300	50	—		
	$\overline{\text{HOLD}}$	750	350	—	750	350	—	750	350	—		
	$\overline{\text{EN}}$	500	250	—	500	250	—	500	250	—		
	EV/ $\overline{\text{OD}}$	1300	850	—	1300	850	—	1300	850	—		
	BPAR	1300	850	—	1300	850	—	1300	850	—		
	B	1700	1100	—	1700	1100	—	1700	1100	—		
t _H	Hold Time SHIFT	200	-150	—	200	-150	—	200	-150	—	ps	—
	S-IN	300	-50	—	300	-50	—	300	-50	—		
	$\overline{\text{HOLD}}$	100	-350	—	100	-350	—	100	-350	—		
	$\overline{\text{EN}}$	100	-250	—	100	-250	—	100	-250	—		
	EV/ $\overline{\text{OD}}$	-200	-850	—	-200	-850	—	-200	-850	—		
	BPAR	-200	-850	—	-200	-850	—	-200	-850	—		
	B	-300	-1100	—	-300	-1100	—	-300	-1100	—		
t _r t _f	Rise/Fall Time 20% to 80%	300	700	1100	300	700	1100	300	700	1100	ps	—



Rev. 03

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