ISL6729

Low-Cost, Single-Ended, Current-Mode PWM for Microcontroller Based Power Converters

FN9152
Rev 3.00
December 21, 2016

The ISL6729 pulse width modulating (PWM) current mode controller is designed for power conversion applications that are based on a microcontroller, or other device, which can generate a digital clock signal at the desired switching frequency. Similar to the ISL684x family of products, the ISL6729 provides the basic current mode PWM control features, but eliminates the error amplifier, the oscillator, and the reference. An external clock signal applied to the oscillator input provides the time base and sets the maximum duty cycle. The reduced feature set is ideal for those applications where a microcontroller is available to provide the monitor and control functions. The analog PWM provides the cycle-by-cycle peak-current mode control, leaving the monitor and control overhead to the microcontroller.

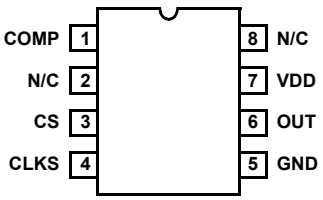
PART NUMBER	RISING UVLO	MAX. DUTY CYCLE
ISL6729	4.75V	100%

Related Literature

- For a full list of related documents, visit our website
  - ISL6729 product page

Pin Configuration

ISL6729 (8 LD SOIC, MSOP)
TOP VIEW



Features

- 5V operation
- 1A MOSFET gate driver
- 400µA startup current
- 30ns propagation delay current sense to output
- Fast transient response with peak-current mode control
- Switching frequency to 2MHz
- 20ns rise and fall times with 1nF output load
- Maximum duty cycle determined by clock input duty cycle
- Tight tolerance current limit threshold
- Pb-free (RoHS compliant)

Applications

- Telecom and datacom power
- Wireless base station power
- File server power
- Industrial power systems
- PC power supplies
- Isolated buck and flyback regulators
- Boost regulators

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE (RoHS COMPLIANT)	PKG. DWG. #
ISL6729IBZ	6729IBZ	-40 to +105	8 Ld SOIC	M8.15
ISL6729IUZ **(No longer available or supported)**	6729Z	-40 to +105	8 Ld MSOP	M8.118

NOTES:

1. Add -T suffix for 2.5k unit tape and reel option. Refer to TB347 for details on reel specifications.
2. Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see product information page for ISL6729. For more information on MSL, see tech brief TB363.

Functional Block Diagram

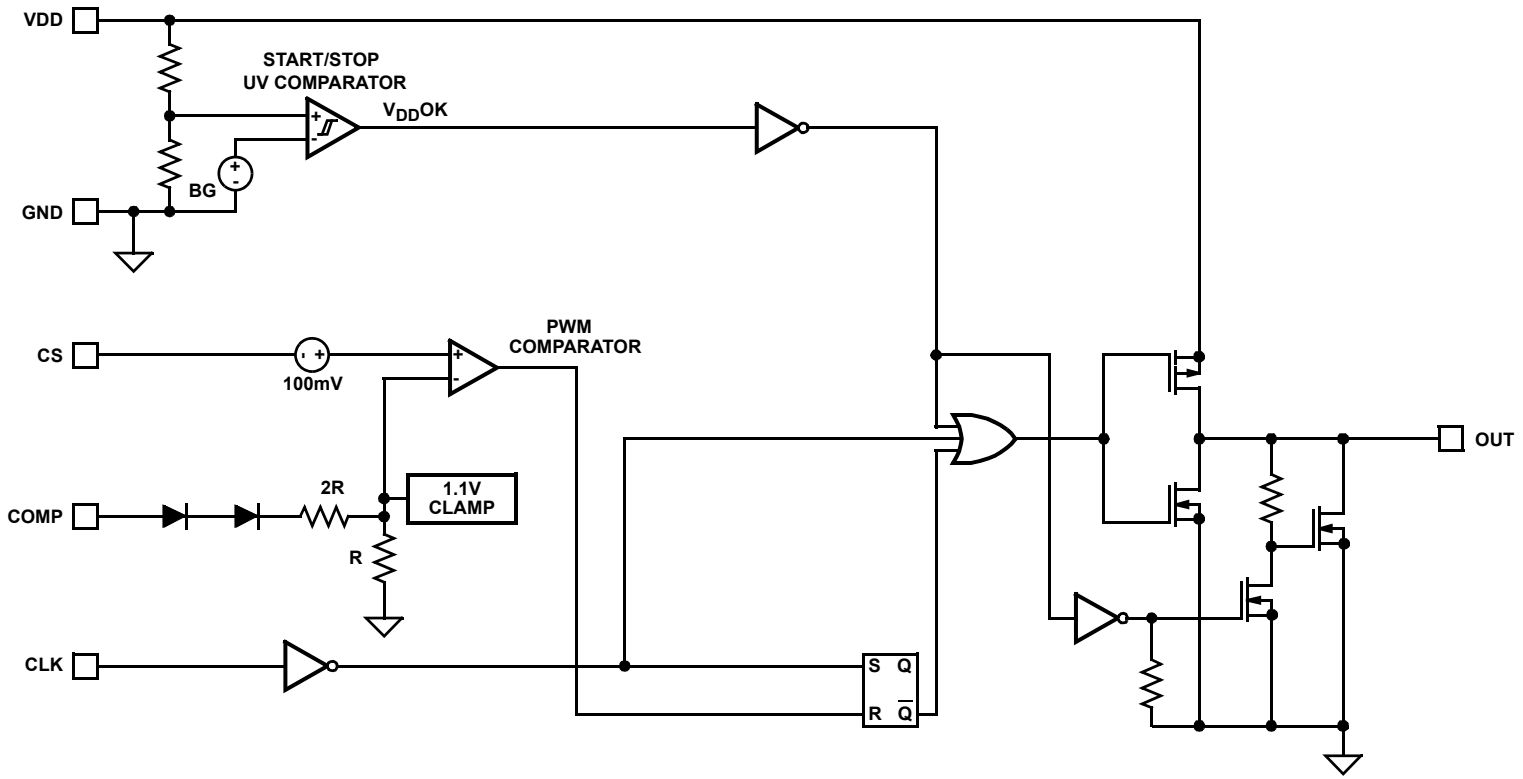


FIGURE 1. FUNCTIONAL BLOCK DIAGRAM

Typical Application - Interleaved Multiphase Isolated Converter

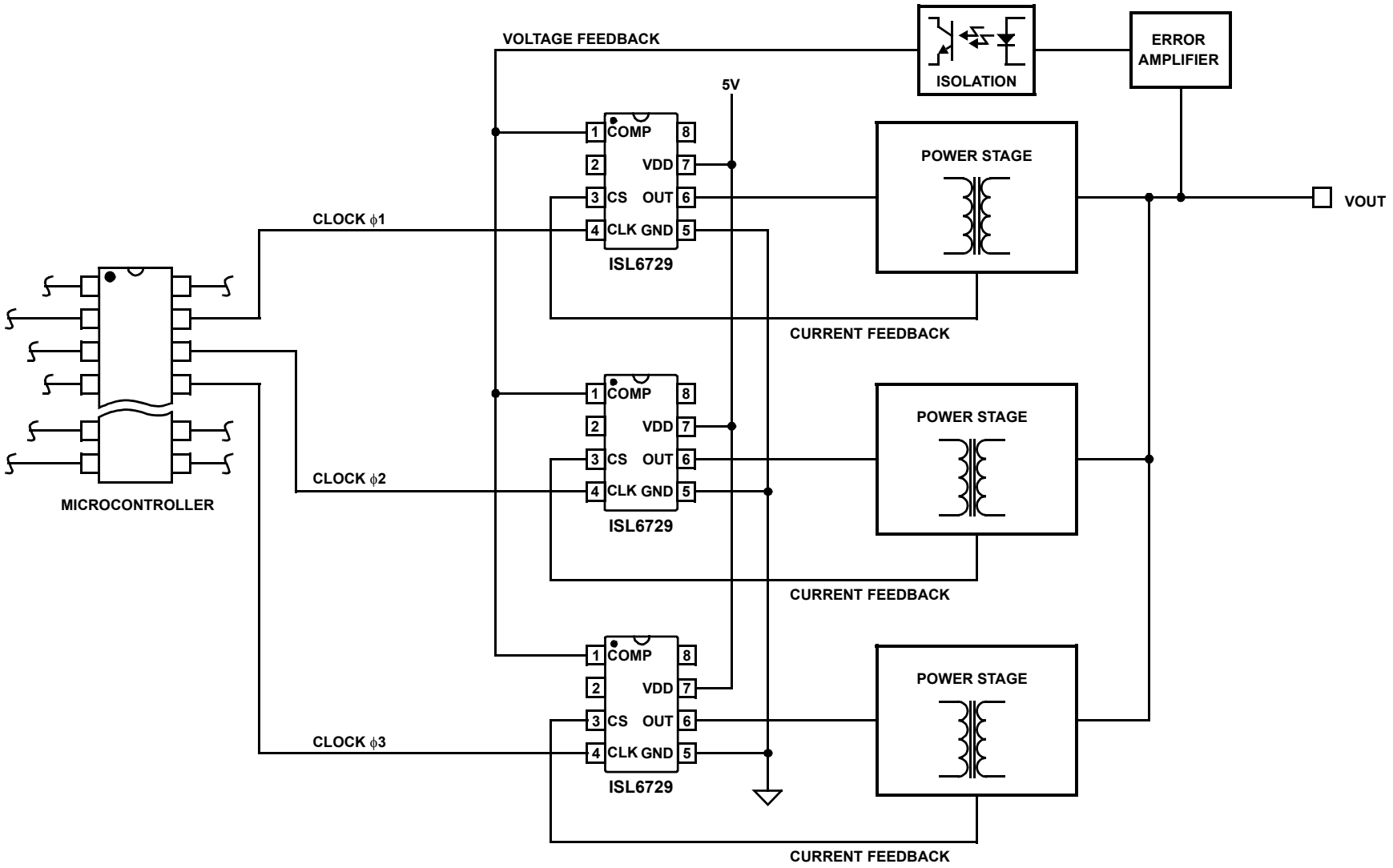


FIGURE 2. TYPICAL APPLICATION - INTERLEAVED MULTIPHASE ISOLATED CONVERTER

Absolute Maximum Ratings

Supply Voltage, VDD . . . . . (GND - 0.3V) to +6.5V
OUT . . . . . (GND - 0.3V) to V_{DD} + 0.3V
Signal Pins . . . . . (GND - 0.3V) to 6.5V
Peak GATE Current 1A
ESD Classification
Human Body Model (Per MIL-STD-883 Method 3015.7) 2kV
Charged Device Model (Per EOS/ESD DS5.3, 4/14/93) 1kV

Thermal Information

Thermal Resistance (Typical, Note 4)	θ_{JA} (°C/W)
SOIC Package	100
MSOP Package	130

Maximum Junction Temperature . . . . . -55°C to +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

Operating Conditions

Temperature Range
ISL6729Ix . . . . . -40°C to +105°C
Supply Voltage Range (Typical)
ISL6729 . . . . . 4.75V to 5.25V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

4. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
5. All voltages are with respect to GND.

Electrical Specifications

Recommended operating conditions unless otherwise noted. Refer to Figure 1 on page 2 and Figure 2 on page 3. V_{DD} = 5V, CLK = 50kHz, T_A = -40 to +105°C (Note 6), Typical values are at T_A = +25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
UNDERVOLTAGE LOCKOUT					
START Threshold		4.15	4.50	4.75	V
STOP Threshold		4.00	4.30	4.60	V
Hysteresis		-	0.2	-	V
Start-Up Current, I_{DD}	V_{DD} < START threshold	-	0.4	12	mA
Operating Current, I_{DD}	(Note 7)	-	3.3	5.5	mA
Operating Supply Current, I_D	Includes 1nF GATE loading	-	4.1	6.0	mA
CURRENT SENSE					
Input Bias Current	V_{CS} = 1V	-1.0	-	1.0	µA
CS Offset Voltage	V_{CS} = 0V (Note 8)	95	100	105	mV
COMP to PWM Comparator Offset Voltage	V_{CS} = 0V (Note 8)	0.80	1.15	1.30	V
CS Input Signal, Maximum		0.91	0.97	1.03	V
Gain, $A_{CS} = \Delta V_{COMP}/\Delta V_{CS}$	0 < V_{CS} < 910mV, V_{FB} = 0V. (Note 8)	2.5	3.0	3.5	V/V
CS to OUT Delay	(Note 8)	-	25	40	ns
CLOCK					
Input High Voltage Level, V_{IH}		-	2.8	-	V
Input Low Voltage Level, V_{IL}		-	2.7	-	V
Maximum Clock Rate	(Note 8)	2	-	-	MHz
OUTPUT					
Gate V_{OH}	V_{DD} - OUT, I_{OUT} = -200mA	-	1.0	2.0	V
Gate V_{OL}	OUT - GND, I_{OUT} = 200mA	-	1.0	2.0	V
Peak Output Current	C_{OUT} = 1nF (Note 8)	1.0	-	-	A
Rise Time	C_{OUT} = 1nF (Note 8)	-	20	40	ns
Fall Time	C_{OUT} = 1nF (Note 8)	-	20	40	ns

Electrical Specifications Recommended operating conditions unless otherwise noted. Refer to Figure 1 on page 2 and Figure 2 on page 3. V_{DD} = 5V, CLK = 50kHz, T_A = -40 to +105°C (Note 6), Typical values are at T_A = +25°C **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PWM					
Maximum Duty Cycle		-	99	-	%
Minimum Duty Cycle		-	-	0	%

NOTES:

6. Specifications at -40°C are established by design, not production tested.
7. This is the V_{DD} current consumed when the device is active but not switching. Does not include gate drive current.
8. Established by design, not 100% tested in production.

Pin Descriptions

CLK - This is the oscillator timing control pin. The operational frequency and maximum duty cycle are set by applying a 5V amplitude clock signal to CLK. The logic high duration defines the maximum ON time for the output. A maximum clock rate up to 2.0MHz is possible.

COMP - COMP is the input to the PWM comparator and is typically controlled through an external error amplifier.

CS - This is the current sense input to the PWM comparator. The range of the input signal is nominally 0 to 1.0V and has an internal offset of 100mV.

GND - GND is the power and small signal reference ground for all functions.

OUT - This is the drive output to the power switching device. It is a high current output capable of driving the gate of a power MOSFET with peak currents of 1.0A. This GATE output is actively held low when V_{DD} is below the UVLO threshold.

VDD - VDD is the 5V power connection for the IC. The IC will operate from 4.75V to 5.25V. However, the accuracy of the voltage clamp on the COMP signal, which determines the overcurrent threshold, is dependent on the accuracy of VDD. A tight tolerance on VDD will result in a tight overcurrent threshold.

The total supply current will depend on the load applied to OUT. Total I_{DD} current is the sum of the operating current and the average output current. Knowing the operating frequency, f, and the MOSFET gate charge, Qg, the average output current can be calculated from:

$$I_{OUT} = Qg \times f \quad \text{(EQ. 1)}$$

To optimize noise immunity, bypass VDD to GND with a ceramic capacitor as close to the VDD and GND pins as possible.

Ground Plane Requirements

Careful layout is essential for satisfactory operation of the device. A good ground plane must be employed. A unique section of the ground plane must be designated for high di/dt currents associated with the output stage. VDD should be bypassed directly to GND with good high frequency capacitors.

Applications Information

Microcontrollers are becoming more popular for monitoring and supervisory functions in power converters due to their flexibility, capability, and declining prices. Many applications would like to take advantage of this flexibility and use them to perform the control loop function as well. There are many examples of voltage mode control using digital signal processing techniques. However, microcontrollers available today do not have the execution speed required for peak current mode control at the operational frequencies of modern switch-mode power supplies. As such, they are unable to detect the peak current and terminate the switching cycle within the few nanosecond window required. The ISL6729 provides the analog circuitry required to perform peak current control, but delegates the oscillator function to the microcontroller. This arrangement allows the microcontroller to control soft-start, maximum duty cycle, and operational frequency of the power converter, as well as performing the traditional overhead functions such as fault monitoring and system interface.

Application of the ISL6729 is similar to the ISL684x family of PWM converters except that the input bias voltage has been changed to 5V and the oscillator, reference, and error amplifier functions have been removed. An external digital clock signal, such as the PWM output of a microcontroller, must be supplied to control the frequency and maximum duty cycle. The frequency of the applied clock signal and the frequency of operation of the PWM are identical. The duty cycle of the clock is the maximum duty cycle of the PWM. Soft-start may be accomplished by incrementing the duty cycle of the applied clock signal from zero to the maximum desired value in a time frame appropriate for the application.

Figure 2 on page 3 illustrates how the ISL6729 may be used for an interleaved power converter. In this example, three clock signals of equal duty cycle, but phased 120° apart, are applied to separate power stages. Each phase shares a common voltage feedback signal, but uses separate current feedback signals from each power stage for regulation. Excellent current sharing behavior is assured since each phase must produce the same peak current. Accuracy is determined by the variation of the output inductor value and the feedback components.

Multiple output power supplies can be created in a similar fashion. Only one clock signal is required if in-phase operation is desired. Each stage may be independently controlled using separate voltage and current feedback loops.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

DATE	REVISION	CHANGE
December 21, 2016	FN9152.3	Updated entire datasheet with new formatting. Updated Notes 1 and 2. Added Note 3. Updated Ordering Information table. Added Related Literature, Revision History, and About Intersil sections. Updated POD M8.15 to the latest revision. Changes are as follows: -Updated to new POD format by removing table and moving dimensions onto drawing and adding land pattern. - Changed in Typical Recommended Land Pattern the following: 2.41(0.095) to 2.20(0.087) 0.76 (0.030) to 0.60(0.023) 0.200 to 5.20(0.205) -Changed Note 1 “1982” to “1994”. Updated POD M8.118 to the latest revision. Changes are as follows: -Updated to new Intersil format by adding land pattern and moving dimensions from table onto drawing. -Corrected lead width dimension in side view 1 from “0.25 - 0.036” to “0.25 - 0.36”.

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing, and high-end consumer markets.

For the most updated datasheet, application notes, related documentation, and related parts, see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support.

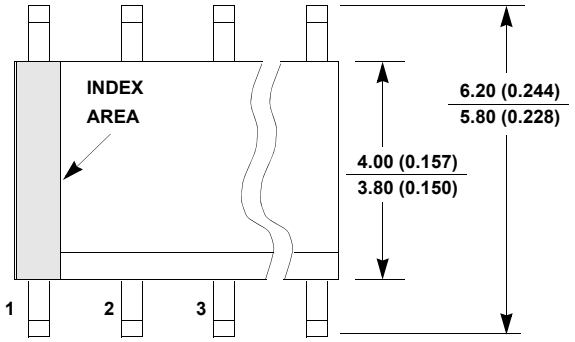
Package Outline Drawing

For the most recent package outline drawing, see M8.15.

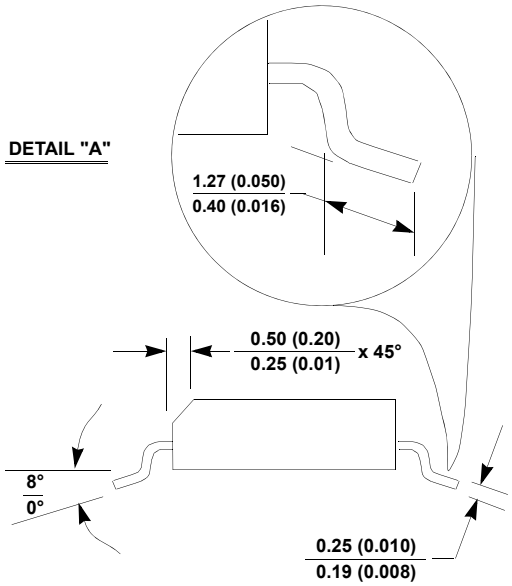
M8.15

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

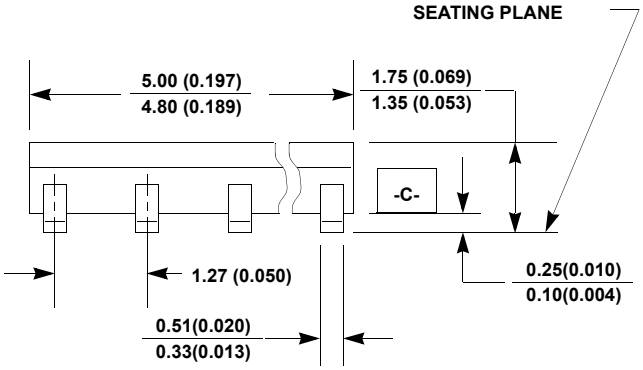
Rev 4, 1/12



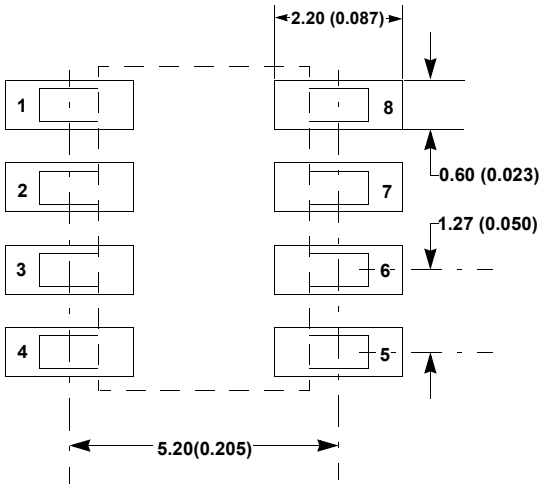
TOP VIEW



SIDE VIEW "B"



SIDE VIEW "A"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensioning and tolerancing per ANSI Y14.5M-1994.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.

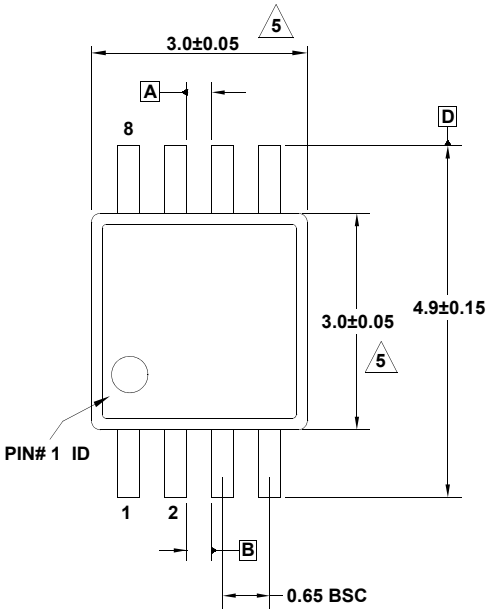
Package Outline Drawing

For the most recent package outline drawing, see M8.118.

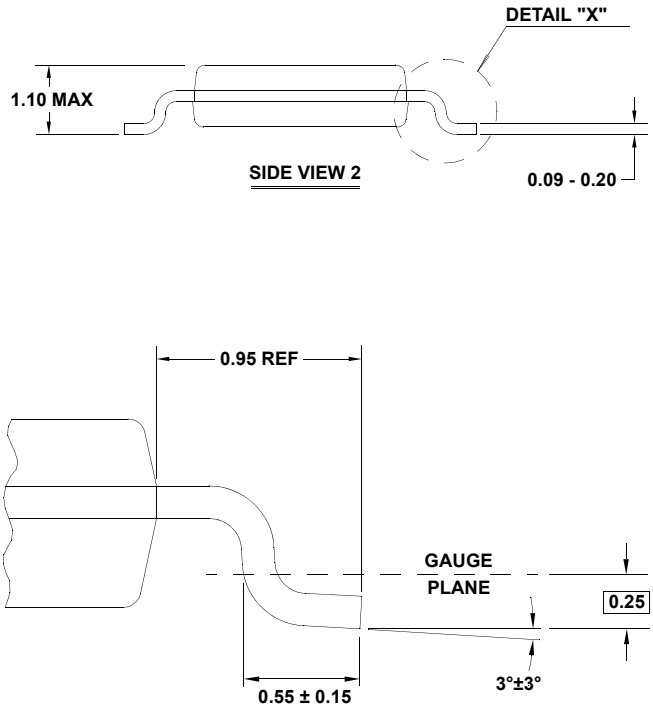
M8.118

8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

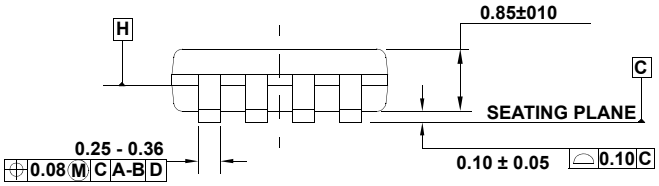
Rev 4, 7/11



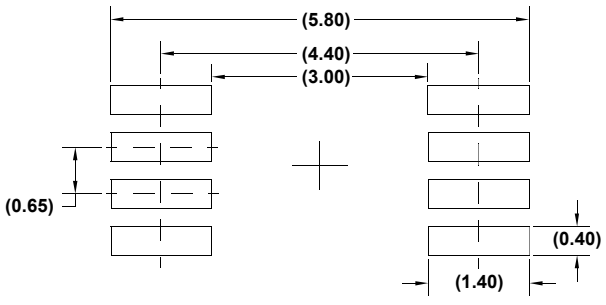
TOP VIEW



DETAIL "X"



SIDE VIEW 1



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-AA and AMSEY14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.15mm max per side are not included.
5. Dimensions are measured at Datum Plane "H".
6. Dimensions in ( ) are for reference only.