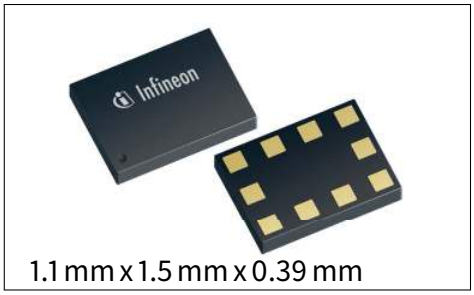
BGSA147ML10

Ultra Low Resistance Antenna Tuning SP4T

Features

- Designed for high-linearity antenna tuning switching and RF tuning applications
- Ultra low R_{ON} resistance of 0.8 Ω at each RF port in ON state
- Individually controlled reflective open or short to ground OFF ports to eliminate unwanted antenna resonances
- Low C_{OFF} capacitance of 155 fF at each port in OFF state
- High RF operating voltage handling above 45 V in OFF state
- MIPI RFFE 2.1 compliant control interface
- External USID_sel pin enabling 3 default USID addresses
- No RF parameter change within supply voltage range
- No blocking capacitors required if no DC applied on the RF lines
- No power supply decoupling required
- Small form factor 1.1 mm x 1.5 mm x 0.39 mm (MSL1, 260°C per JEDEC J-STD-020)
- RoHS and WEEE compliant package



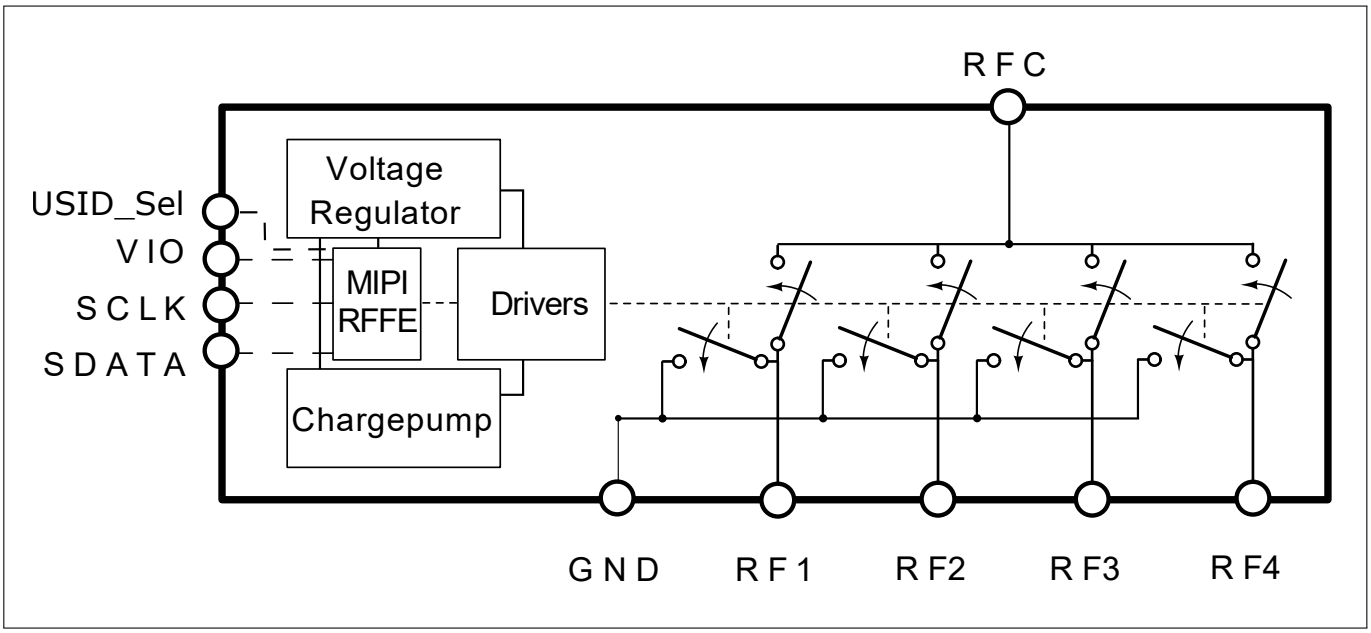
Potential Applications

- Impedance Tuning
- Antenna Tuning
- Inductance Tuning
- Tunable Filters

Product Validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Block diagram



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1 Features

- Designed for high-linearity antenna tuning switching and RF tuning applications
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RoHS Halogen-Free Lead-Free Green

Description

The BGSA147ML10 is a Single-Pole Four Throws (SP4T) Antenna Tuning switch optimized for RF applications up to 7.125 GHz. Its MIPI RFFE digital control interface allows easy implementation and best flexibility when operated in cellular mobile RF Front-End designs.

The BGSA147ML10 is made of 4 ultra-low On resistance / low Off capacitance series switches and 4 shunt to ground switches enabling on-demand open-reflective or short-reflective OFF ports behaviour. This last feature is of great value to reduce antenna engineer development time in case of unwanted antenna resonance or to improve antenna efficiency with less component tuning effort.

Unlike GaAs RF switches, highly linear RF performance is reached at all signal levels within the operating conditions. High RF voltage ruggedness and individually programmable shunt to ground switches on each RF throw make BGSA147ML10 particularly efficient for switching inductors and capacitors in RF matching and Antenna Tuning circuits.

Type	Marking	Package	Ordering Information
BGSA147ML10	A7	TSLP-10-3	BGSA 147ML10 E6327

2 Maximum Ratings

Table 1: Maximum Ratings Table at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Frequency Range	f	0.4	–	7.125	GHz	[1]
RFFE Supply voltage [2]	V_{IO}	-0.3	–	2.2	V	Only for infrequent and short duration time periods
Storage temperature range	T_{STG}	-55	–	150	°C	–
RF peak voltage	V_{RF_max}	–	–	50	V	Short term peaks (1μs in 0.1% duty cycle), exceeding typical linearity, Ron and Coff parameters, in Isolation mode, test condition schematic in Fig. 1
ESD robustness, CDM [3]	$V_{ESD_{CDM}}$	-1	–	+1	kV	
ESD robustness, HBM [4]	$V_{ESD_{HBM}}$	-2	–	+2	kV	
Junction temperature	T_j	–	–	125	°C	–
Thermal resistance junction - soldering point	R_{thJS}	–	–	80	K/W	–
Maximum DC-voltage on RF-Ports and RF-Ground	V_{RFDC}	0	–	0	V	No DC voltages allowed on RF-Ports
RFFE Control Voltage Levels	V_{SCLK}, V_{SDATA}, V_{USID_SEL}	-0.7	–	V_{IO}+0.7 (max. 2.2)	V	–

[1] Switch has a low-pass response. For higher frequencies, losses have to be considered for their impact on thermal heating. The DC voltage at RF ports V_{RFDC} has to be 0V.
[2] Note: Consider any ripple voltages on top of V_{IO}. A high RF ripple at the V_{IO} can exceed the maximum ratings by $V_{IO} = V_{DC} + V_{Ripple}$.
[3] Field-Induced Charged-Device Model ANSI/ESDA/JEDEC JS-002. Simulates charging/discharging events that occur in production equipment and processes. Potential for CDM ESD events occurs whenever there is metal-to-metal contact in manufacturing.
[4] Human Body Model ANSI/ESDA/JEDEC JS-001 (R=1,5 kΩ, C=100 pF).

Warning: Stresses above the max. values listed here may cause permanent damage to the device. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit. Exposure to conditions at or below absolute maximum rating but above the specified maximum operation conditions may affect device reliability and life time. Functionality of the device might not be given under these conditions.

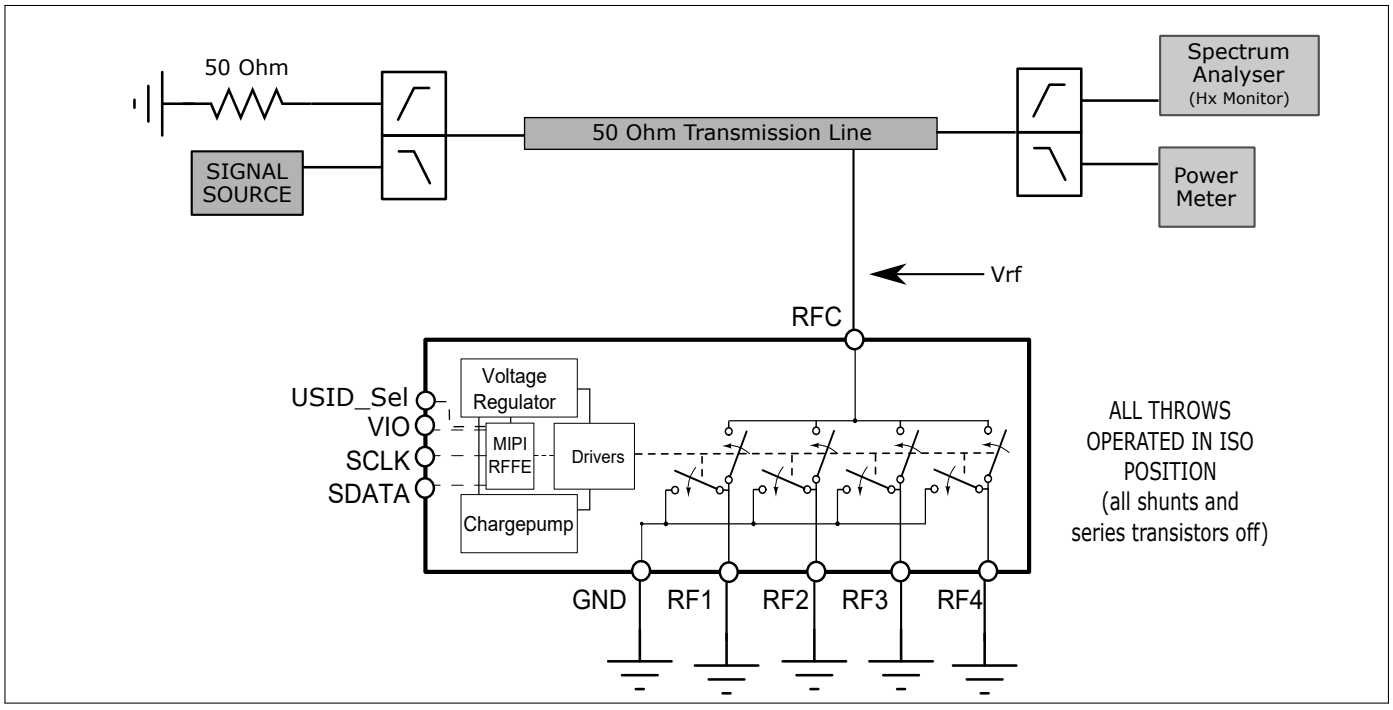

Figure 1: RF operating voltage measurement configuration - OFF mode

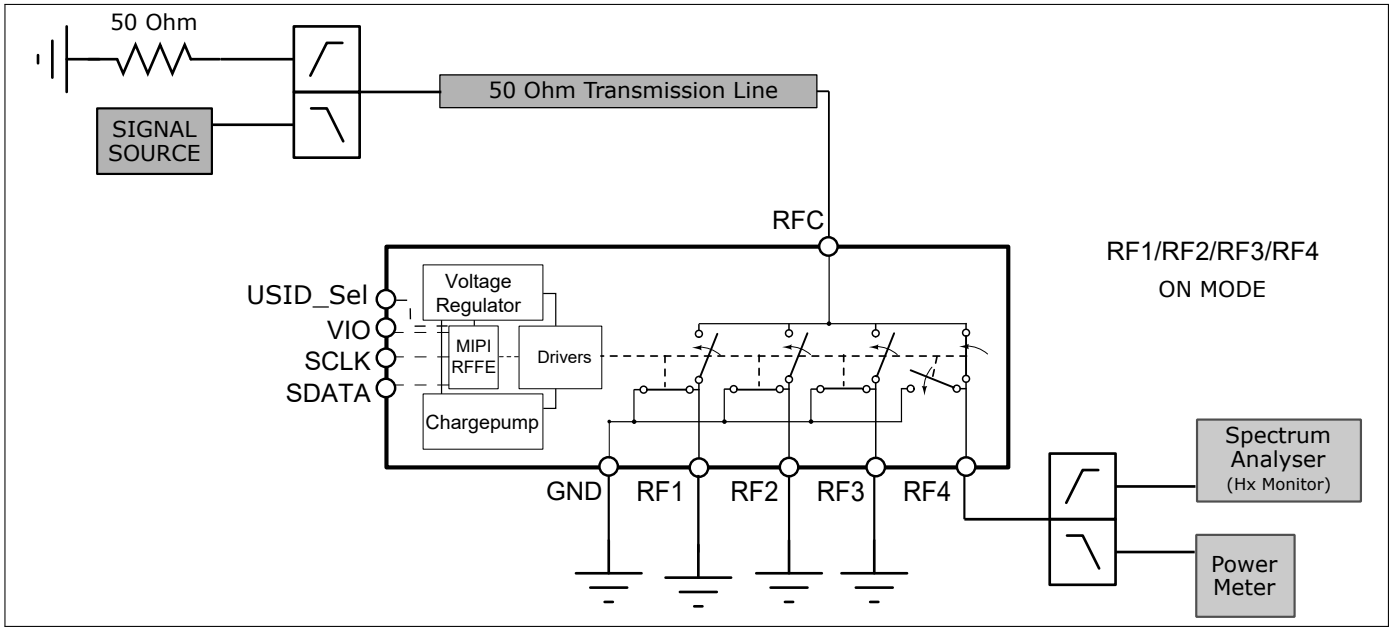

Figure 2: RF operating and Harmonics generation measurement configuration - RFx ON mode (RF4 as example)

3 DC Characteristics

Table 2: DC Characteristics at T_A = −40 °C to 85 °C

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
RFFE supply voltage	V_{IO}	1.65	1.8	1.95	V	–
RFFE input high voltage[1]	V_{IH}	0.7*V_{IO}	–	V_{IO}	V	–
RFFE input low voltage[1]	V_{IL}	0	–	0.3*V_{IO}	V	–
RFFE output high voltage[1]	V_{OH}	0.8*V_{IO}	–	V_{IO}	V	–
RFFE output low voltage[1]	V_{OL}	0	–	0.2*V_{IO}	V	–
RFFE control input capacitance	C_{Ctrl}	–	–	2	pF	–
RFFE supply current	I_{VIO}	–	2	–	µA	VIO Shutdown Mode
		–	22	35	µA	Idle State, no RF Power

[1]SCLK and SDATA

4 RF Small Signal Characteristics

Table 3: Parametric specifications

Parameter	Symbol	Values			Unit	STATE / Notes
		Min.	Typ.	Max.		
Series switch ON DC resistance	R_{ON_Series}	–	0.8	0.85	Ω	T_A = 25 °C, Z_0 = 50 Ω
Series switch OFF DC resistance	R_{OFF_Series}	250	–	–	kΩ	
Shunt to GND switch ON DC resistance	R_{ON_Shunt}		5.8	7	Ω	
Shunt to GND switch OFF DC resistance	R_{OFF_Shunt}	250	–	–	kΩ	
RFx to RFc OFF capacitance, 1 GHz	C_{OFF} [1]	–	155	170	fF	

[1] OFF capacitance calculated from Y21 parameters, shunt OFF.

Table 4: RF electrical parameters, OFF port shunts switches open

Parameter	Symbol	Values			Unit	STATE / Notes
		Min.	Typ.	Max.		
Insertion Loss: RFx to RFC[1,2,3,4]						
600 - 960 MHz	IL_{SP4T}		0.1	0.3	dB	V_{IO} = 1.65 – 1.95 V, Z_0 = 50 Ω at all RF-ports, T_A = –40 °C... + 85 °C
1400 - 1700 MHz			0.25	0.5	dB	
1710 - 2169 MHz			0.35	0.6	dB	
2170 - 2690 MHz			0.5	0.9	dB	
3300 - 4200 MHz			1.2	1.8	dB	
4400 - 5000 MHz			1.7	2.3	dB	
5150 - 5925 MHz			2.1	2.9	dB	
5925 - 7125 MHz			2.5	3.9	dB	
Return Loss: RF1, RF2, RF3, RF4 or RFC [1,2,3]						
600 - 960 MHz	RL_{SP4T}	17	21		dB	V_{IO} = 1.65 – 1.95 V, Z_0 = 50 Ω at all RF-ports, T_A = –40 °C... + 85 °C
1400 - 1700 MHz		13	16		dB	
1710 - 2169 MHz		11	14		dB	
2170 - 2690 MHz		9	13		dB	
3300 - 4200 MHz		6	9		dB	
4400 - 5000 MHz		5	8		dB	
5150 - 5925 MHz		4	7		dB	
5925 - 7125 MHz		4	6		dB	
Isolation: RFx to RFC[1,2,3,4]						
600 - 960 MHz	ISO_{OFF}	19	23		dB	V_{IO} = 1.65 – 1.95 V, Z_0 = 50 Ω at all RF-ports, T_A = –40 °C... + 85 °C
1400 - 1700 MHz		15	17		dB	
1710 - 2169 MHz		13	16		dB	
2170 - 2690 MHz		12	14		dB	
3300 - 4200 MHz		10	12		dB	
4400 - 5000 MHz		9	11		dB	
5150 - 5925 MHz		9	11		dB	
5925 - 7125 MHz		9	11		dB	

[1] Valid for all RF power levels, no compression behavior
[2] On application board without any matching components
[3] Shunts in OFF Mode
[4] x = 1, 2, 3, 4

Table 5: RF electrical parameters, OFF port shunts switches closed

Parameter	Symbol	Values			Unit	STATE / Notes
		Min.	Typ.	Max.		
Insertion Loss: RFx to RFC[1,2,3,4]						
600 - 960 MHz	IL_{SP4T}		0.1	0.2	dB	V_{IO} = 1.65 – 1.95 V, Z_0 = 50 Ω at all RF-ports, T_A = –40 °C... + 85 °C
1400 - 1700 MHz			0.2	0.35	dB	
1710 - 2169 MHz			0.3	0.5	dB	
2170 - 2690 MHz			0.4	0.8	dB	
3300 - 4200 MHz			1.1	1.9	dB	
4400 - 5000 MHz			1.8	2.7	dB	
5150 - 5925 MHz			2.5	3.7	dB	
5925 - 7125 MHz			3.3	5.3	dB	
Return Loss: RF1, RF2, RF3, RF4 or RFC[1,2,3]						
600 - 960 MHz	RL_{SP4T}	17	21		dB	V_{IO} = 1.65 – 1.95 V, Z_0 = 50 Ω at all RF-ports, T_A = –40 °C... + 85 °C
1400 - 1700 MHz		12	16		dB	
1710 - 2169 MHz		11	14		dB	
2170 - 2690 MHz		9	12		dB	
3300 - 4200 MHz		5	8		dB	
4400 - 5000 MHz		4	6		dB	
5150 - 5925 MHz		3	5		dB	
5925 - 7125 MHz		3	5		dB	
Isolation: RFx to RFC[1,2,3,4]						
600 - 960 MHz	ISO_{OFF}	32	39		dB	V_{IO} = 1.65 – 1.95 V, Z_0 = 50 Ω at all RF-ports, T_A = –40 °C... + 85 °C
1400 - 1700 MHz		23	30		dB	
1710 - 2169 MHz		20	27		dB	
2170 - 2690 MHz		17	24		dB	
3300 - 4200 MHz		12	18		dB	
4400 - 5000 MHz		10	16		dB	
5150 - 5925 MHz		9	14		dB	
5925 - 7125 MHz		8	13		dB	

[1] Valid for all RF power levels, no compression behavior
[2] On application board without any matching components
[3] Shunts in ON Mode
[4] x = 1, 2, 3, 4

5 RF large signal parameter

Table 6: RF large signal specifications at T_A = 25 °C

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
RF Operating Voltage	V_{RF_opr}	–	–	45	V	In Isolation mode, 900 MHz test condition schematic in Fig. 1
Harmonic Generation up to 15 GHz, all RF Ports						
Second Order Harmonics	P_{H2}	–	-85	-80	dBm	26 dBm, 50 Ω, f_0 = 663 MHz
Third Order Harmonics	P_{H3}	–	-92	-88	dBm	26 dBm, 50 Ω, f_0 = 663 MHz
Second Order Harmonics	P_{H2}	–	-67	-60	dBm	35 dBm, 50 Ω, f_0 = 920 MHz
Third Order Harmonics	P_{H3}	–	-69	-66	dBm	35 dBm, 50 Ω, f_0 = 920 MHz
Second Order Harmonics	P_{H2}	–	-65	-61	dBm	33 dBm, 50 Ω, f_0 = 1910 MHz
Third Order Harmonics	P_{H3}	–	-70	-66	dBm	33 dBm, 50 Ω, f_0 = 1910 MHz
Second Order Harmonics	P_{H2}	–	-68	-64	dBm	29 dBm, 50 Ω, f_0 = 2690 MHz
Third Order Harmonics	P_{H3}	–	-74	-68	dBm	29 dBm, 50 Ω, f_0 = 2690 MHz
Second Order Harmonics	P_{H2}	–	-65	-58	dBm	29 dBm, 50 Ω, f_0 = 3600 MHz
Third Order Harmonics	P_{H3}	–	-76	-69	dBm	29 dBm, 50 Ω, f_0 = 3600 MHz
Second Order Harmonics	P_{H2}	–	-67	-64	dBm	29 dBm, 50 Ω, f_0 = 4400 MHz
Third Order Harmonics	P_{H3}	–	-77	-73	dBm	29 dBm, 50 Ω, f_0 = 4400 MHz
Second Order Harmonics	P_{H2}	–	-68	-64	dBm	29 dBm, 50 Ω, f_0 = 5000 MHz
Third Order Harmonics	P_{H3}	–	-77	-70	dBm	29 dBm, 50 Ω, f_0 = 5000 MHz
Intermodulation Distortion IMD2						
IIP2, low	$IIP2, l$	110	121	–	dBm	IIP2 conditions Tab. 7
IIP2, high	$IIP2, h$	115	125	–	dBm	
Intermodulation Distortion IMD3						
IIP3	$IIP3$	72	78	–	dBm	IIP3 conditions Tab. 8

Table 7: IIP2 conditions table

Band	In-Band Frequency [MHz]	Blocker Frequency 1 [MHz]	Blocker Power 1 [dBm]	Blocker Frequency 2 [MHz]	Blocker Power 2 [dBm]
Band 1 Low	2140	1950	23	190	-15
Band 1 High	2140	1950	23	4090	-15
Band 5 Low	881.5	836.5	23	45	-15
Band 5 High	881.5	836.5	23	1718	-15

Table 8: IIP3 conditions table

Band	In-Band Frequency [MHz]	Blocker Frequency 1 [MHz]	Blocker Power 1 [dBm]	Blocker Frequency 2 [MHz]	Blocker Power 2 [dBm]
Band 1	2140	1950	23	1760	-15
Band 5	881.5	836.5	23	791.5	-15

6 MIPI RFFE Specification

The MIPI RFFE interface is implemented according to the following specifications and documents:

- MIPI Alliance Specification for RF Front-End Control Interface version 2.1 - 18 December 2017
- MIPI Alliance Errata 01 for MIPI RFFE Specification Version v2.1 - 24 February 2019
- Qualcomm RFFE Vendor specification 80-N7876-1 Rev. Y (December 3, 2018)

Table 9: MIPI Features

Feature	Supported	Comment
MIPI RFFE 2.1 standard	Yes	Backward compatible to MIPI 2.0 standard
Register 0 write command sequence	Yes	
Register read and write command sequence	Yes	
Extended register read and write command sequence	Yes	
Support for standard frequency range operations for SCLK	Yes	Up to 26 MHz
Support for extended frequency range operations for SCLK	Yes	Up to 52 MHz
Longer Reach RFFE Bus Length Feature	Yes	
Programmable driver strength	Yes	Up to 80 pF
Programmable Group SID	Yes	
Programmable USID	Yes	
Trigger functionality	Yes	
Extended Triggers and Trigger Masks	Yes	
Broadcast / GSID write to PM TRIG register	Yes	
Reset	Yes	Via VIO, PM TRIG or software register
Status / error sum register	Yes	
Extended product ID register	Yes	
Revision ID register	Yes	
Group SID register	Yes	
USID select pin	Yes	USID selection See Tab. 10

Table 10: Default MIPI USID Selection

Address	Symbol	External Conditon at USID Port
USID=0110	Addr6	to VIO
USID=0111	Addr7	Ground
USID=1001	Addr9	Floating[1)]

[1)] Total capacitance on the USID_SEL pin must be <5 pF.

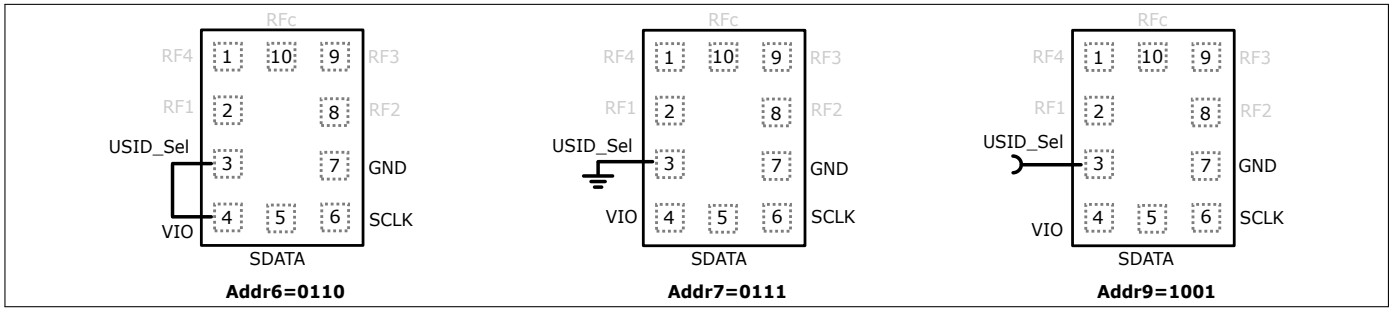

Figure 3: BGSA147ML10 USID_Sel Pin Configuration

Table 11: Startup Behavior

Feature	State	Comment
Power status	Low power	Lower power mode after start-up Default power mode is HIGH
Trigger function	Enabled	Enabled after start-up. Programmable via behavior control register

Table 12: Switching Time Behavior

Parameter	Symbol	Values			Unit	STATE / Notes
		Min.	Typ.	Max.		
Power Up Settling Time	t_{PUP}	–	9	15	µs	Time from Power Up plus Switch command 50% last SCLK falling edge to 90% RF-Signal, see Fig. 4
Switching Time	t_{ST}	–	8	11	µs	Time switching between RF states 50% last SCLK falling edge to 90% RF-Signal, see Fig. 4

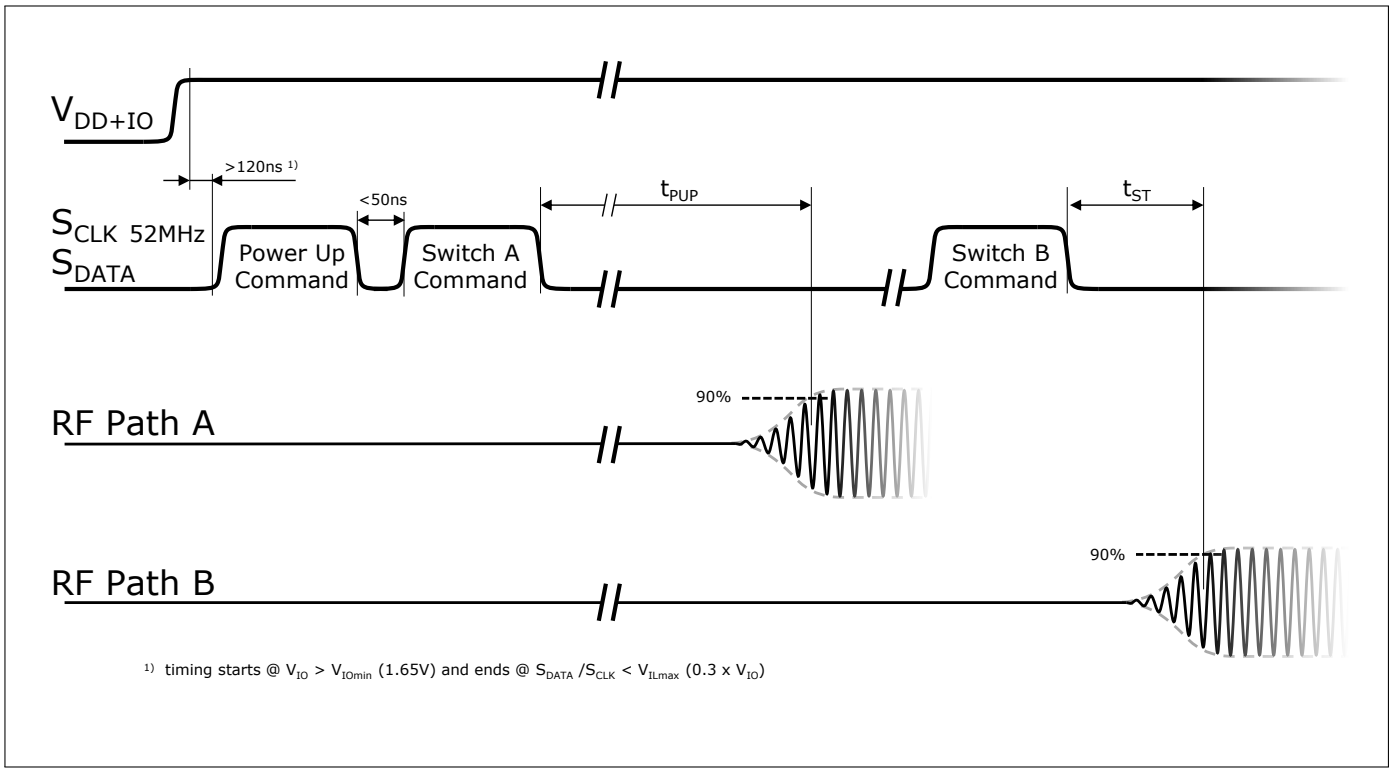

Figure 4: BGSA147ML10 Switching Time Behavior

Table 13: Register Mapping, Table I

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x00	REGISTER_0	7:0	MODE_CTRL	RF Switch Control	00000000	No	Yes Trigger 0-10	R/W
0x01	REGISTER_1	7:0	MODE_CTRL	RF Switch Control	00000000	No	Yes Trigger 0-10	R/W
0x1C	PM_TRIG	7	PWR_MODE(1) Operation Mode	0: Normal operation (ACTIVE) 1: Low Power Mode (LOW POWER)	1	Yes	No	R/W
		6	PWR_MODE(0) State Bit Vector	0: No action (ACTIVE) 1: Powered Reset (STARTUP to ACTIVE to LOW POWER)	0			
		5	TRIGGER_MASK_2	0: Data masked (held in shadow REG) 1: Data not masked (ready for transfer to active REG)	0	No		
		4	TRIGGER_MASK_1	0: Data masked (held in shadow REG) 1: Data not masked (ready for transfer to active REG)	0			
		3	TRIGGER_MASK_0	0: Data masked (held in shadow REG) 1: Data not masked (ready for transfer to active REG)	0			
		2	TRIGGER_2	0: No action (data held in shadow REG) 1: Data transferred to active REG	0	Yes		
		1	TRIGGER_1	0: No action (data held in shadow REG) 1: Data transferred to active REG	0			
		0	TRIGGER_0	0: No action (data held in shadow REG) 1: Data transferred to active REG	0			
0x1D	PRODUCT_ID	7:0	PRODUCT_ID	This is a read-only register. However, during the programming of the USID a write command sequence is performed on this register, even though the write does not change its value.	00110100	No	No	R
0x1E	MAN_ID	7:0	MANUFACTURER_ID [7:0]	This is a read-only register. However, during the programming of the USID, a write command sequence is performed on this register, even though the write does not change its value.	00011010	No	No	R
0x1F	MAN_USID	7:4	MANUFACTURER_ID [11:8]	These bits are read-only. However, during the programming of the USID, a write command sequence is performed on this register even though the write does not change its value.	0001			
		3:0	USID[3:0]	USID_Sel pin	See Tab. 10	No	No	R/W

Table 14: Register Mapping, Table II

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x20	EXT_PRODUCT_ID	7:0	EXT_PRODUCT_ID	Extension to PRODUCT_ID in register 0x1D. This is a read-only register. However, during the programming of the USID a write command sequence is performed on this register, even though the write does not change its value.	00000000	No	No	R
0x21	REV_ID	7:4	MAIN_REVISION	Chip main revision	0000	No	No	R
		3:0	SUB_REVISION	Chip sub revision	0000			
0x22	GSID	7:4	GSID0[3:0]	Primary Group Slave ID.	0000	No	No	R/W
		3:0	GSID1[3:0]	Secondary Group Slave ID.	0000			
0x23	UDR_RST	7	UDR_RST	Reset all configurable non-RFFE Reserved registers to default values. 0: Normal operation 1: Software reset	0	Yes	No	R/W
		6:0	RESERVED	Reserved for future use	0000000			
0x24	ERR_SUM	7	RESERVED	Reserved for future use	0	No	No	R
		6	COMMAND_FRAME_PARITY_ERR	Command Sequence received with parity error — discard command.	0			
		5	COMMAND_LENGTH_ERR	Command length error.	0			
		4	ADDRESS_FRAME_PARITY_ERR	Address frame with parity error.	0			
		3	DATA_FRAME_PARITY_ERR	Data frame with parity error.	0			
		2	READ_UNUSED_REG	Read command to an invalid address.	0			
		1	WRITE_UNUSED_REG	Write command to an invalid address.	0			
		0	BID_GID_ERR	Read command with a BROADCAST_ID or GROUP_ID.	0			
0x2B	BUS_LD	7:3	RESERVED	Reserved for future use	0x0	No	No	R/W
		2:0	BUS_LD[2:0]	Program the drive strength of the SDATA driver in readback modes. 0x0: 10 pF 0x1: 20 pF 0x2: 30 pF 0x3: 40 pF 0x4: 50 pF 0x5: 60 pF 0x6: 80 pF 0x7: 80 pF 0x8-0xF: Spare	0x4			

Table 15: Register Mapping, Table III

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x2D	EXT_TRIG_MASK	7	TRIGGER_MASK_10	0: Data writes to registers tied to EXT_TRIGGER_10 are masked. Data is held in shadow registers until the EXT_TRIGGER_10 bit is set to 1. 1: Data writes to registers tied to EXT_TRIGGER_10 are not masked. Data writes go directly to the active registers.	1	No	No	R/W
		6	TRIGGER_MASK_9	0: Data writes to registers tied to EXT_TRIGGER_9 are masked. Data is held in shadow registers until the EXT_TRIGGER_9 bit is set to 1. 1: Data writes to registers tied to EXT_TRIGGER_9 are not masked. Data writes go directly to the active registers.	1			
		5	TRIGGER_MASK_8	0: Data writes to registers tied to EXT_TRIGGER_8 are masked. Data is held in shadow registers until the EXT_TRIGGER_8 bit is set to 1. 1: Data writes to registers tied to EXT_TRIGGER_8 are not masked. Data writes go directly to the active registers.	1			
		4	TRIGGER_MASK_7	0: Data writes to registers tied to EXT_TRIGGER_7 are masked. Data is held in shadow registers until the EXT_TRIGGER_7 bit is set to 1. 1: Data writes to registers tied to EXT_TRIGGER_7 are not masked. Data writes go directly to the active registers.	1			
		3	TRIGGER_MASK_6	0: Data writes to registers tied to EXT_TRIGGER_6 are masked. Data is held in shadow registers until the EXT_TRIGGER_6 bit is set to 1. 1: Data writes to registers tied to EXT_TRIGGER_6 are not masked. Data writes go directly to the active registers.	1			
		2	TRIGGER_MASK_5	0: Data writes to registers tied to EXT_TRIGGER_5 are masked. Data is held in shadow registers until the EXT_TRIGGER_5 bit is set to 1. 1: Data writes to registers tied to EXT_TRIGGER_5 are not masked. Data writes go directly to the active registers.	1			
		1	TRIGGER_MASK_4	0: Data writes to registers tied to EXT_TRIGGER_4 are masked. Data is held in shadow registers until the EXT_TRIGGER_4 bit is set to 1. 1: Data writes to registers tied to EXT_TRIGGER_4 are not masked. Data writes go directly to the active registers.	1			
		0	TRIGGER_MASK_3	0: Data writes to registers tied to EXT_TRIGGER_3 are masked. Data is held in shadow registers until the EXT_TRIGGER_3 bit is set to 1. 1: Data writes to registers tied to EXT_TRIGGER_3 are not masked. Data writes go directly to the active registers.	1			

Table 16: Register Mapping, Table IV

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x2E	EXT_TRIG	7	TRIGGER_10	0: No action. Data is held in shadow registers.	0	Yes	No	R/W
				1: Data is transferred from shadow registers to active registers for refisters tied to EXT_TRIGGER_10				
		6	TRIGGER_9	0: No action. Data is held in shadow registers.	0			
				1: Data is transferred from shadow registers to active registers for refisters tied to EXT_TRIGGER_9				
		5	TRIGGER_8	0: No action. Data is held in shadow registers.	0			
				1: Data is transferred from shadow registers to active registers for refisters tied to EXT_TRIGGER_8				
		4	TRIGGER_7	0: No action. Data is held in shadow registers.	0			
				1: Data is transferred from shadow registers to active registers for refisters tied to EXT_TRIGGER_7				
		3	TRIGGER_6	0: No action. Data is held in shadow registers.	0			
				1: Data is transferred from shadow registers to active registers for refisters tied to EXT_TRIGGER_6				
		2	TRIGGER_5	0: No action. Data is held in shadow registers.	0			
				1: Data is transferred from shadow registers to active registers for refisters tied to EXT_TRIGGER_5				
		1	TRIGGER_4	0: No action. Data is held in shadow registers.	0			
				1: Data is transferred from shadow registers to active registers for refisters tied to EXT_TRIGGER_4				
		0	TRIGGER_3	0: No action. Data is held in shadow registers.	0			
				1: Data is transferred from shadow registers to active registers for refisters tied to EXT_TRIGGER_3				

Warning: Register_0 and Register_1 RF switch control bits are identical. Writing both Registers Register_0 and Register_1 simultaneously will lead to undefined behavior. The unused register (Register_0 or Register_1) must remain 0x00.

Table 17: Modes of Operation (Truth Table, Register_0)

State	Mode	D7	D6	D5	D4	D3	D2	D1	D0
0	ALL Series OFF (All Shunts OFF)	0	0	0	0	0	0	0	0
1	ALL Saries OFF (All Shunts ON)	1	1	1	1	0	0	0	0
2	RF1 Series	0	0	0	0	0	0	0	1
3	RF2 Series	0	0	0	0	0	0	1	0
4	RF3 Series	0	0	0	0	0	1	0	0
5	RF4 Series	0	0	0	0	1	0	0	0
6	RF1 Shunt	0	0	0	1	0	0	0	0
7	RF2 Shunt	0	0	1	0	0	0	0	0
8	RF3 Shunt	0	1	0	0	0	0	0	0
9	RF4 Shunt	1	0	0	0	0	0	0	0

Mapping of Switch Rows to Bit: ON = 1 OFF = 0

Table 18: Modes of Operation (Truth Table, Register_1)

State	Mode	D7	D6	D5	D4	D3	D2	D1	D0
0	ALL Series OFF (All Shunts OFF)	0	0	0	0	0	0	0	0
1	ALL Series OFF (All Shunts ON)	1	1	1	1	0	0	0	0
2	RF1 Series	0	0	0	0	0	0	0	1
3	RF2 Series	0	0	0	0	0	0	1	0
4	RF3 Series	0	0	0	0	0	1	0	0
5	RF4 Series	0	0	0	0	1	0	0	0
6	RF1 Shunt	0	0	0	1	0	0	0	0
7	RF2 Shunt	0	0	1	0	0	0	0	0
8	RF3 Shunt	0	1	0	0	0	0	0	0
9	RF4 Shunt	1	0	0	0	0	0	0	0

Mapping of Switch Rows to Bit: ON = 1 OFF = 0

BGSA147ML10 truth table allows to connect any combination of above bits in one single write to register_0 (respectively register_1) command. As an example RF1 series can be set ON while RF1 shunt is set OFF, RF2, RF3 and RF4 series set OFF and shunt set ON by using this single write to register_0 command «0b:11100001».

7 Application Information

Pin Configuration and Function

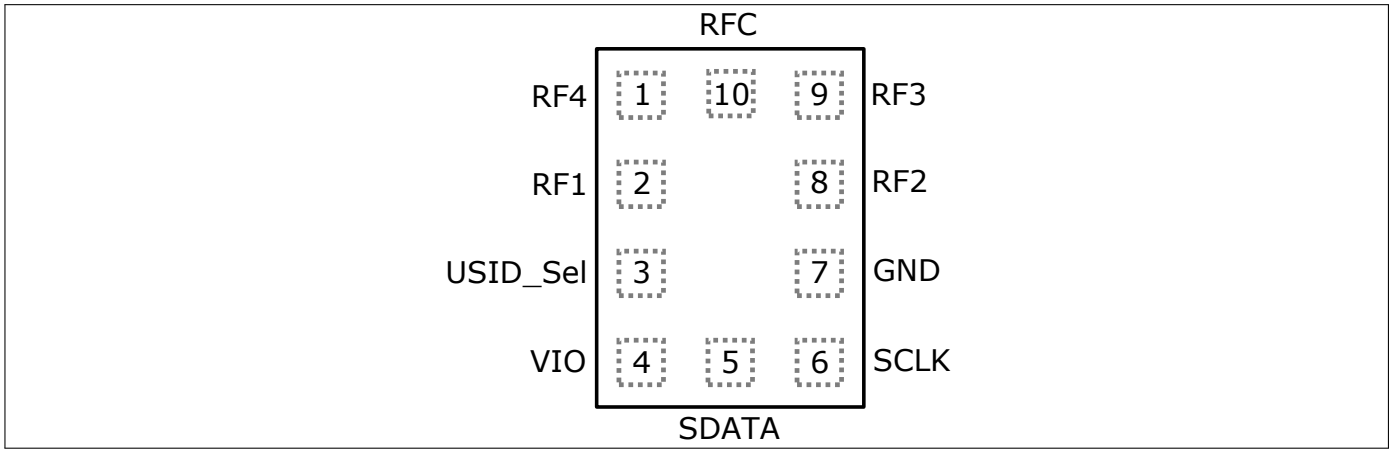

Figure 5: BGSA147ML10 Pin Configuration (top view)

Table 19: Pin Definition and Function

Pin No.	Name	Function
1	RF4	RF4 port
2	RF1	RF1 port
3	USID_Sel	USID_Sel port (see Tab. 10 for 3 different USID States)
4	VIO	RFFE Power Supply
5	SDATA	MIPI RFFE DATA
6	SCLK	MIPI RFFE CLOCK
7	GND	Ground
8	RF2	RF2 port
9	RF3	RF3 port
10	RFC	Common RF port

Evaluation Board Description

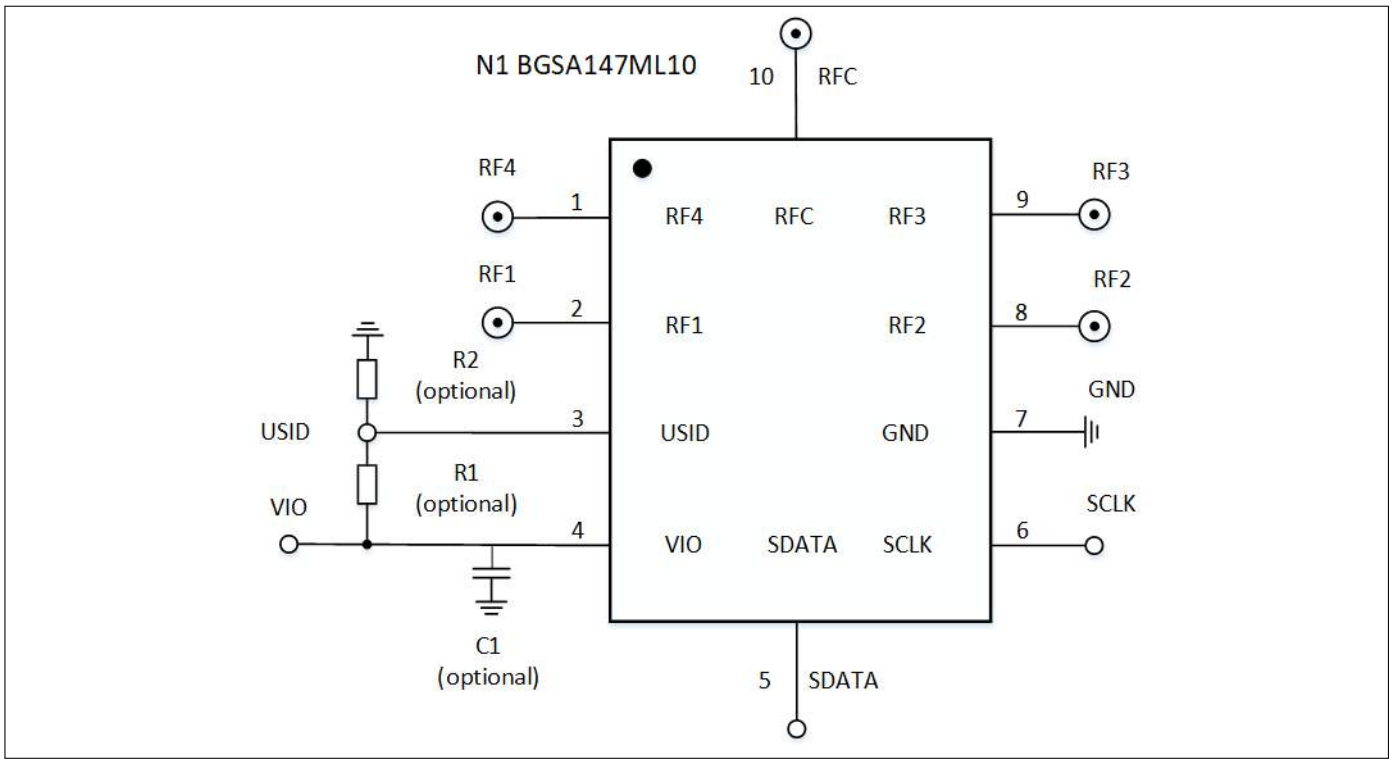

Figure 6: BGSA147ML10 Application Schematic

Table 20: Bill of Materials Table

Name	Part Type	Package	Manufacturer	Function
C1 (100pF optional)	Capacitor	0402	Various	De-coupling capacitor
N1	BGSA147ML10	TSLP-10-3	Infineon	Antenna Tuner
R1 (0 Ohm) R2 (do not place)	Resistor	0402	Various	Set USID default Address to 6 (VIO)
R2 (0 Ohm) R1 (do not place)	Resistor	0402	Various	Set USID default Address to 7 (GND)
R1 (do not place) R2 (do not place)	Resistor	0402	Various	Set USID default Address to 9 (FLOATING)

Table 21: ESD robustness, System Level Test (SLT)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ESD SLT [1]	$V_{ESD_{SLT}}$	-8	–	+8	kV	RF vs system GND, with 27 nH shunt inductor
ESD SLT [1]	$V_{ESD_{SLT}}$	-6	–	+6	kV	RF vs system GND, with 56 nH shunt inductor

[1] IEC 61000-4-2 (R = 330 Ω, C = 150 pF), contact discharge.

8 Package Information

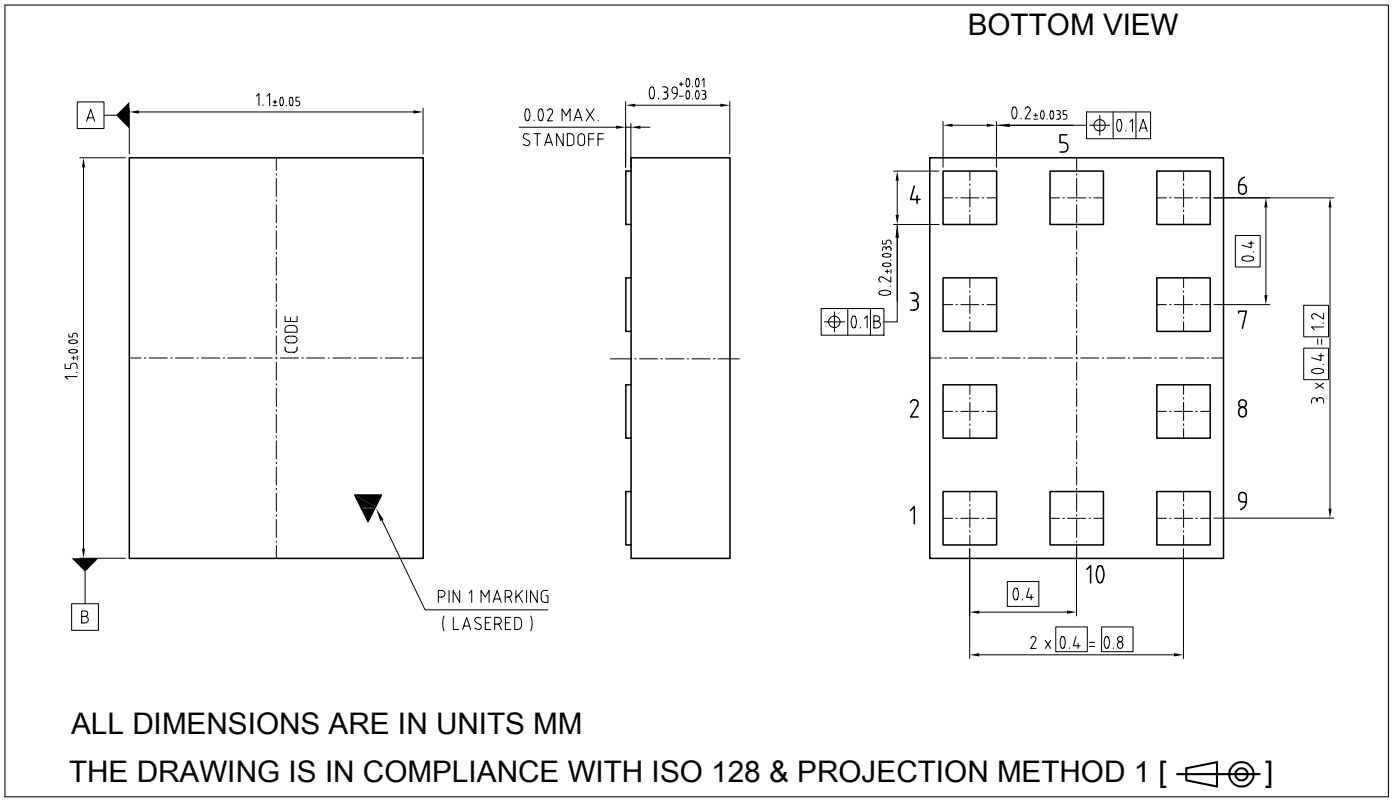

Figure 7: TSLP-10-3 Package Outline (top, side and bottom views)

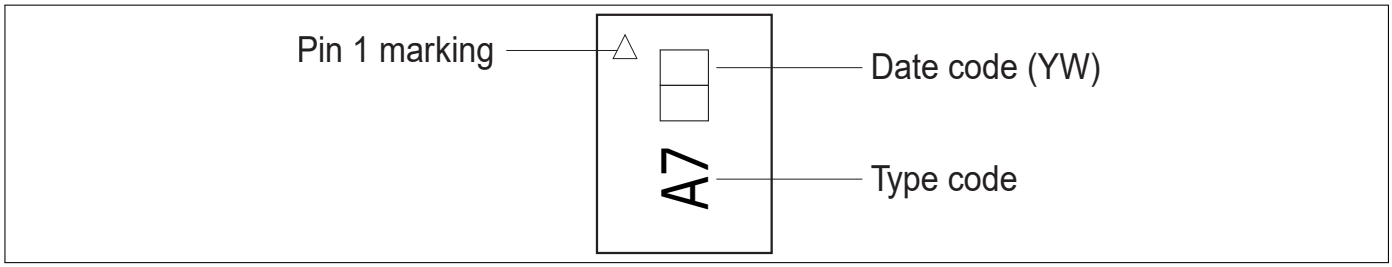

Figure 8: Marking Specification (top view): Date code digits Y and W defined in Table 22/23

Table 22: Year date code marking - digit "Y"

Year	"Y"	Year	"Y"	Year	"Y"
2010	0	2020	0	2030	0
2011	1	2021	1	2031	1
2012	2	2022	2	2032	2
2013	3	2023	3	2033	3
2014	4	2024	4	2034	4
2015	5	2025	5	2035	5
2016	6	2026	6	2036	6
2017	7	2027	7	2037	7
2018	8	2028	8	2038	8
2019	9	2029	9	2039	9

Table 23: Week date code marking - digit "W"

Week	"W"	Week	"W"	Week	"W"	Week	"W"	Week	"W"
1	A	12	N	23	4	34	h	45	v
2	B	13	P	24	5	35	j	46	x
3	C	14	Q	25	6	36	k	47	y
4	D	15	R	26	7	37	l	48	z
5	E	16	S	27	a	38	n	49	8
6	F	17	T	28	b	39	p	50	9
7	G	18	U	29	c	40	q	51	2
8	H	19	V	30	d	41	r	52	3
9	J	20	W	31	e	42	s	53	M
10	K	21	Y	32	f	43	t		
11	L	22	Z	33	g	44	u		

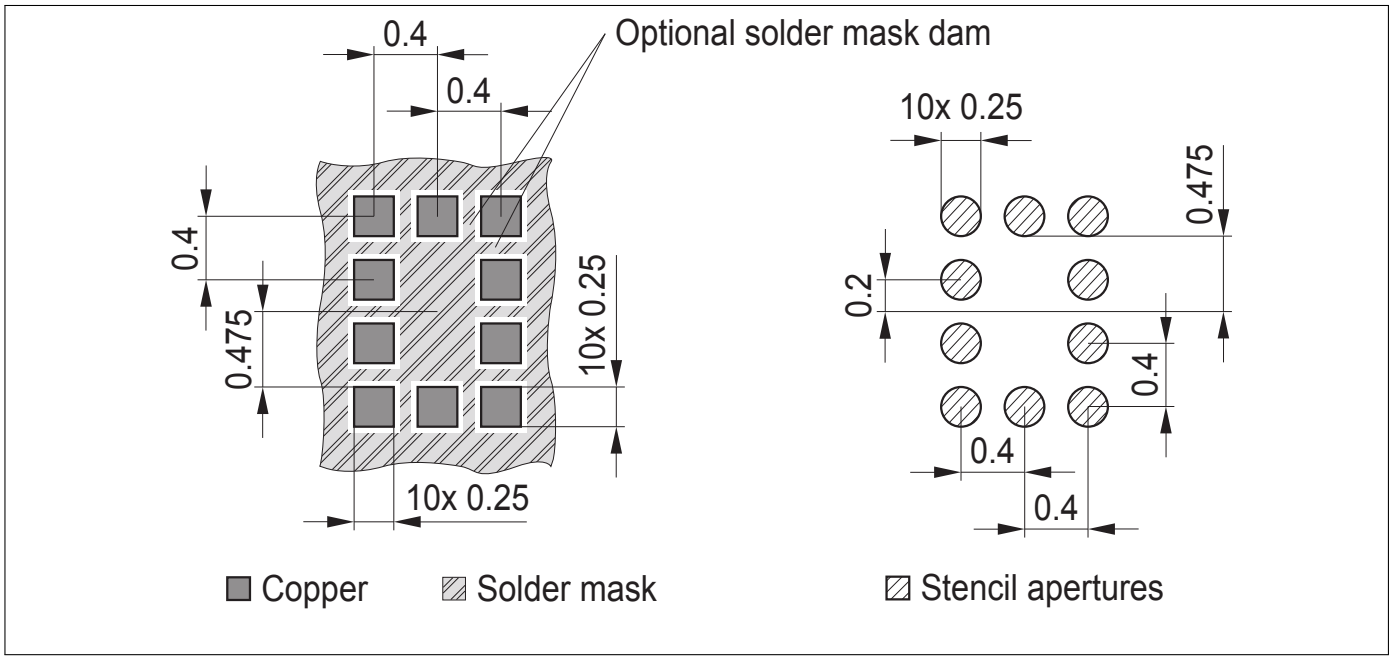

Figure 9: Footprint Recommendation (all dimensions are in units of mm)

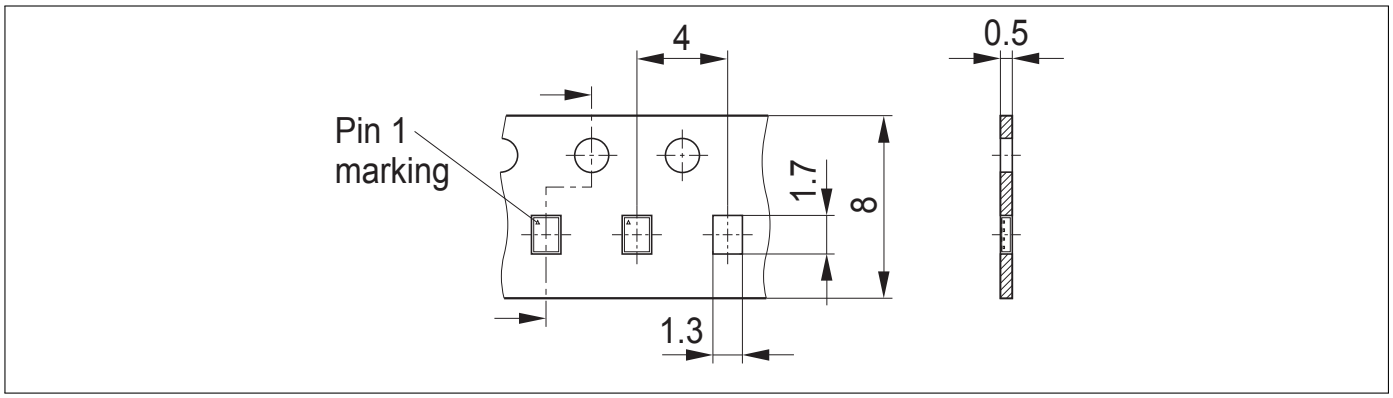

Figure 10: TSLP-10-3 Carrier Tape (all dimensions are in units of mm)

Revision History	
Page or Item	**Subjects (major changes since previous revision)**
Revision 2.1, 2020-12-22	
Cover page	Package height added
20	Reference design and BOM added

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