16DYYPWEVM Test board for SOT-23 THIN (DYY) and TSSOP (PW) packages User's Guide

This document is the EVM User's guide for the 16DYYPWEVM which provides an easy evaluation of TI's new SOT-23 thin and popular TSSOP packages.

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1 About this Manual

This user's guide describes the 16DYYPWEVM evaluation module (EVM) and its intended use.

2 Information About Cautions and Warnings

The information in the warning statement is provided for personal protection and the information in the caution statement is provided to protect the equipment from damage. Read each caution and warning statement carefully.

CAUTION

This EVM contains components that can potentially be damaged by electrostatic discharge. Always transport and store the EVM in its supplied ESD bag when not in use. Handle using an antistatic wristband. Operate on an antistatic work surface. For more information on proper handling, see *Electrostatic Discharge (ESD)*.

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3 Description

The 16DYYPWEVM allows for quick testing of TI's new SOT-23 thin and popular TSSOP packages. The board has a footprint to support both PW and DYY packages.

3.1 Features

The EVM has the following features:

- Dual footprint of SOT-23 THIN (DYY) and TSSOP (PW) packages
- Quick prototyping and testing of 16 pin IC in SOT-23 THIN (DYY) and TSSOP (PW) packages
- All 16 signals paths include 0603 pads for pull-up, pull-down, or load-capacitors
- Test site with 3 SMB connectors for high speed evalauation for TMUX1574 and SN3257-Q1 devices

Figure 1 illustrates the 16DYYPWEVM board.

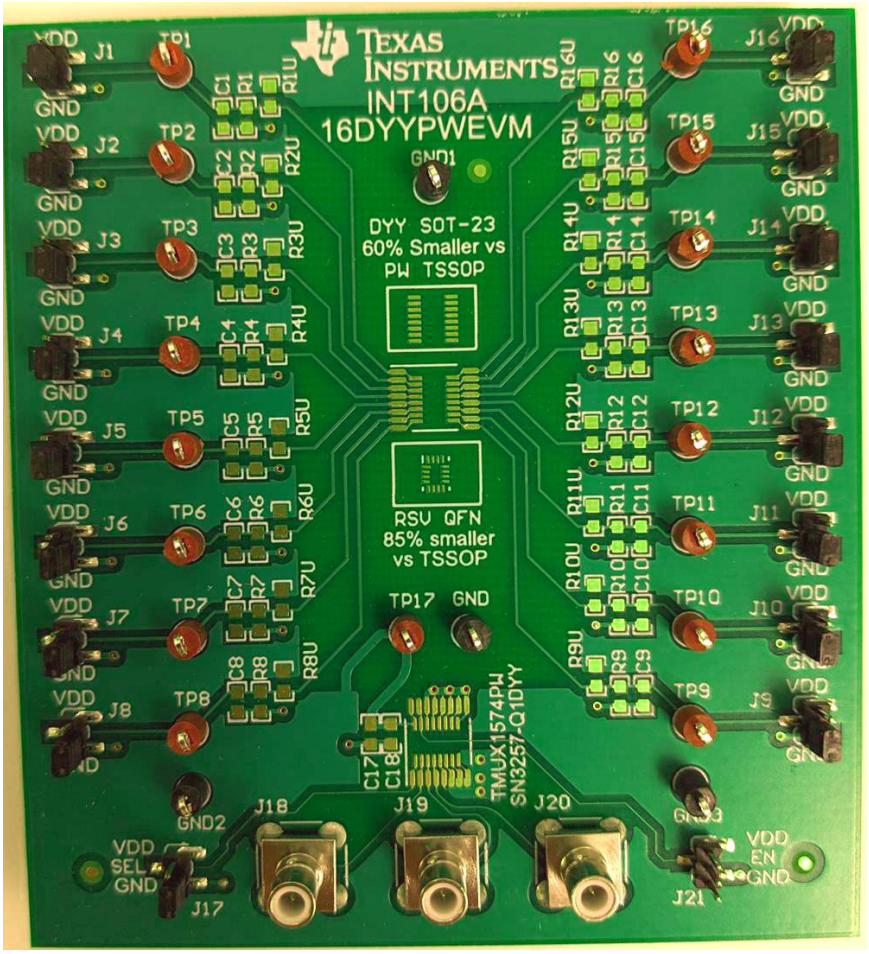

Figure 1. 16DYYPWEVM

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4 16DYYPWEVM Connections Overview

4.1 Usage Instructions

Instructions for IC use follow:

1. Solder ICs to the IC footprint in center of PCB. Parts may be hand-soldered or attached with infrared (IR) or hot air reflow techniques.
2. Power the board by placing power supply on TP17 and GND. TP17 is connected to the entire VDD plane and GND is connected to the entire GND plane
3. Jumpers J1-J16 may be used to easily connect the IC pin to VDD plane or GND plane
4. The 0603 footprints on the signal path may be used to add capacitive and resitive loads, pull-up resistors, or pull-down resistors.
5. J18-J20 provide SMB connections for high speed or timing measurements on pins 2-4 of an IC.

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4.1.1 Schematic

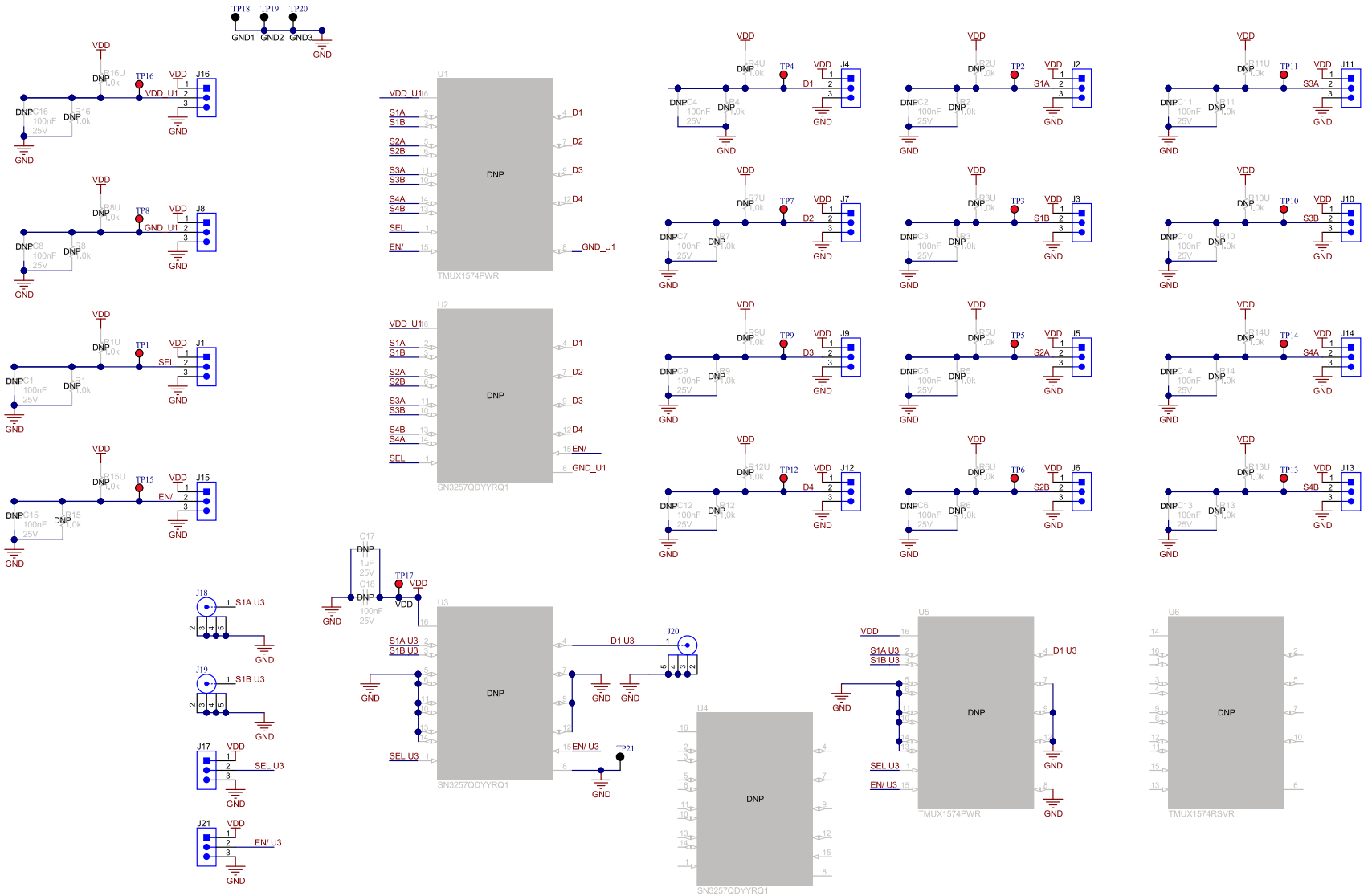

Figure 2. INT106A Schematic

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4.1.2 Layout

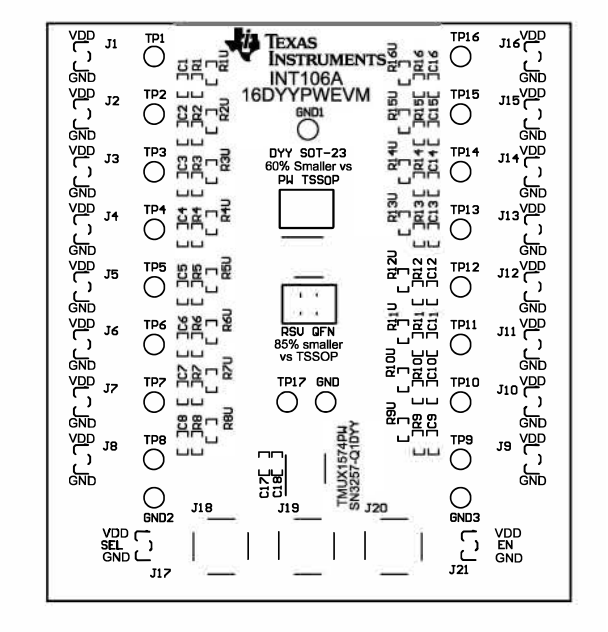

Figure 3. INT106 Top Overlay

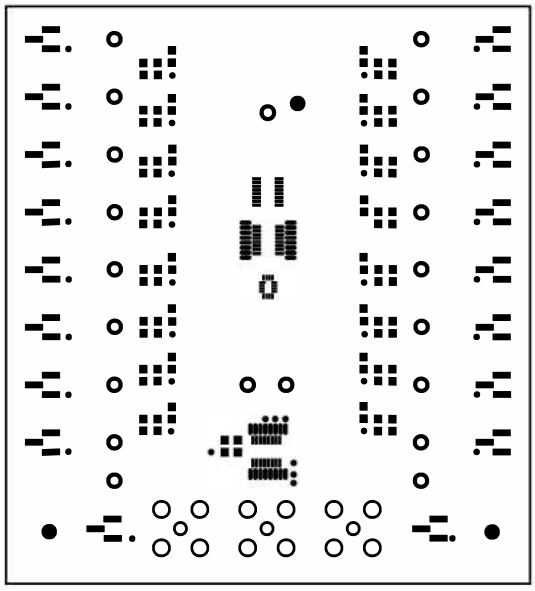

Figure 4. INT106 Top Solder

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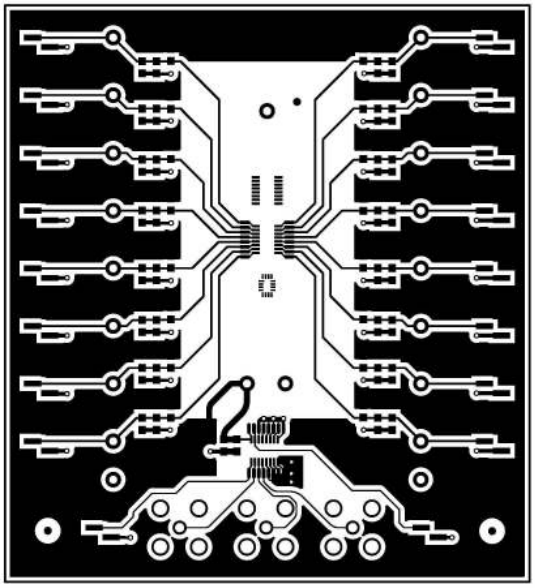

Figure 5. INT106 Top Layer

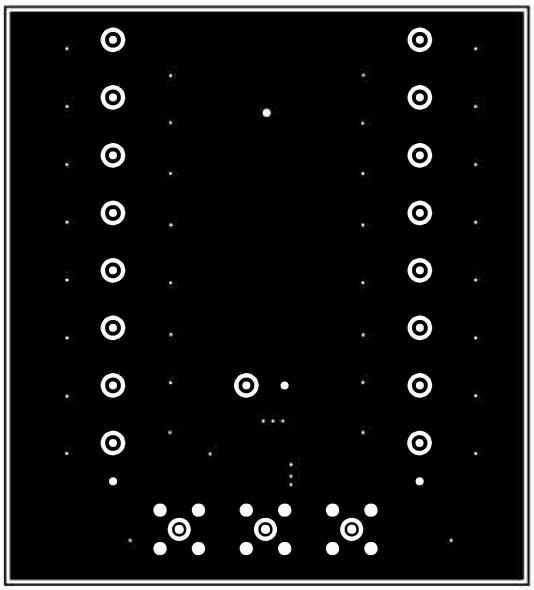

Figure 6. INT106 Bottom Layer

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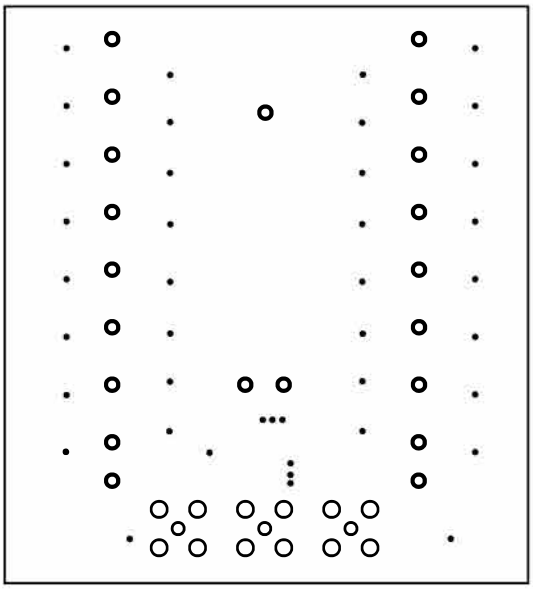

Figure 7. INT106 Bottom Solder

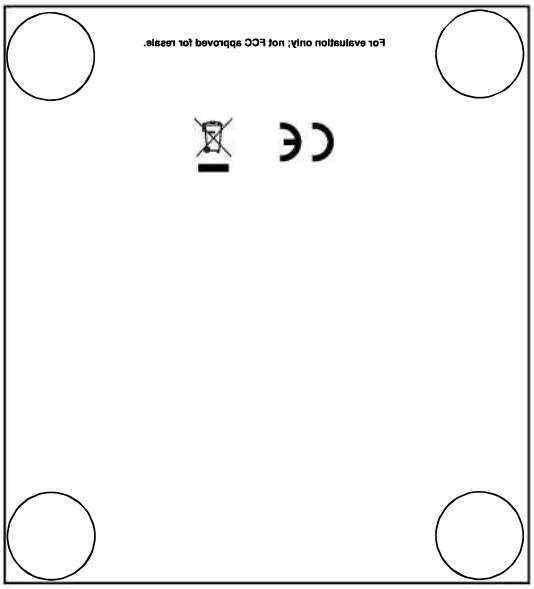

Figure 8. INT106 Bottom Overlay

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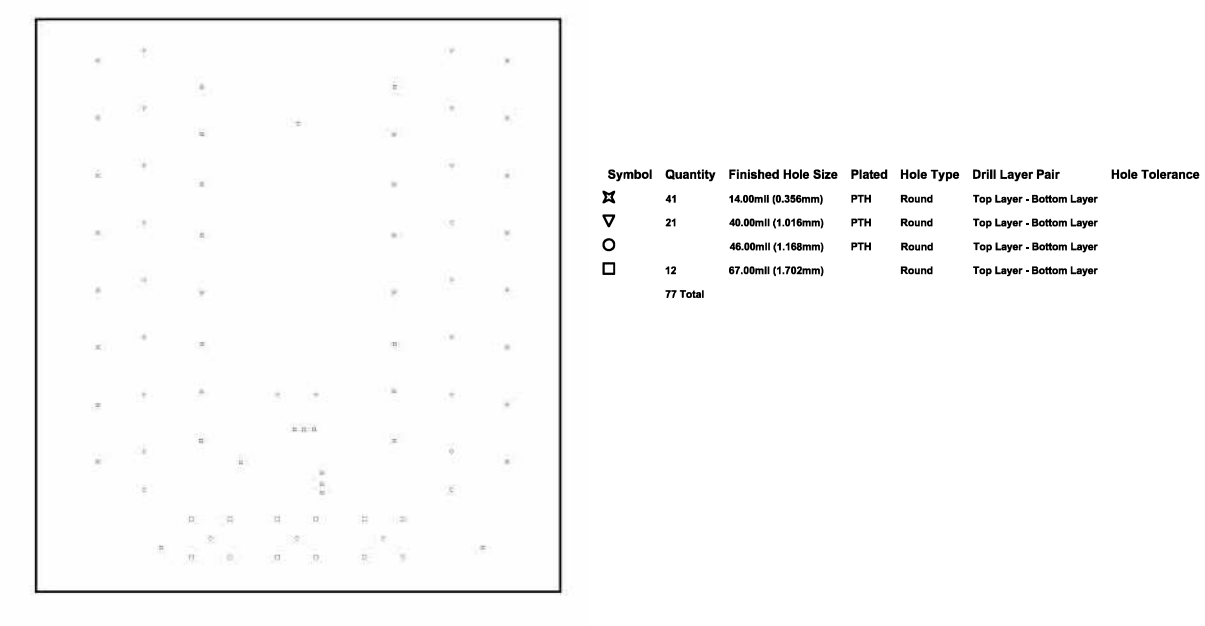

Symbol	Quantity	Finished Hole Size	Plated	Hole Type	Drill Layer Pair	Hole Tolerance
⊠	41	14.00mil (0.356mm)	PTH	Round	Top Layer - Bottom Layer	
▽	21	40.00mil (1.016mm)	PTH	Round	Top Layer - Bottom Layer	
○		46.00mil (1.168mm)	PTH	Round	Top Layer - Bottom Layer	
□	12	67.00mil (1.702mm)		Round	Top Layer - Bottom Layer	
	77 Total					

Figure 9. INT106 Drill Drawing

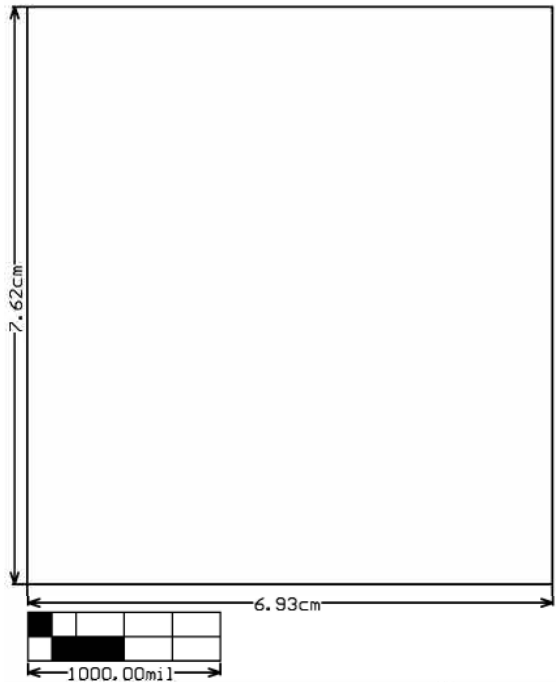

Figure 10. INT106 Board Dimensions

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