BURR-BROWN®

PCM1728

SoundPLUS™ 24-Bit, 96kHz Sampling CMOS Delta-Sigma Stereo Audio DIGITAL-TO-ANALOG CONVERTER

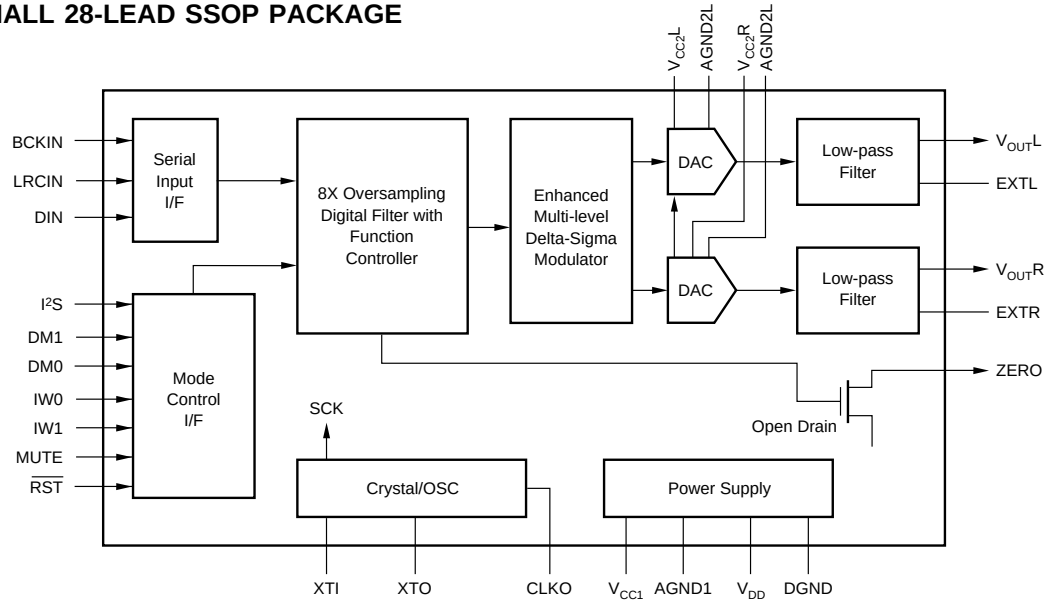
FEATURES

- ENHANCED MULTI-LEVEL DELTA-SIGMA DAC
- SAMPLING FREQUENCY (f_S): 16kHz - 96kHz
- INPUT AUDIO DATA WORD:
  16-, 20-, 24-Bit
- HIGH PERFORMANCE:
  THD+N: –96dB
  Dynamic Range: 106dB
  SNR: 106dB
  Analog Output Range: 0.62 x V_{CC} (Vp-p)
- 8x OVERSAMPLING DIGITAL FILTER:
  Stop Band Attenuation: –82dB
  Passband Ripple: ±0.002dB
- MULTI FUNCTIONS:
  Digital De-emphasis
  Soft Mute
  Zero Flag
- +5V SINGLE SUPPLY OPERATION
- SMALL 28-LEAD SSOP PACKAGE

DESCRIPTION

The PCM1728 is designed for mid- to high-grade digital audio applications which achieve 96kHz sampling rates with 24-bit audio data. PCM1728 uses a newly developed, enhanced multi-level delta-sigma modulator architecture that improves audio dynamic performance and reduces jitter sensitivity in actual applications. The internal digital filter operates at 8X oversampling at a 96kHz sampling rate.

The PCM1728 has superior audio dynamic performance, 24-bit resolution, and 96kHz sampling, making it ideal for mid- to high-grade audio applications such as CD, DVD, and musical instruments.



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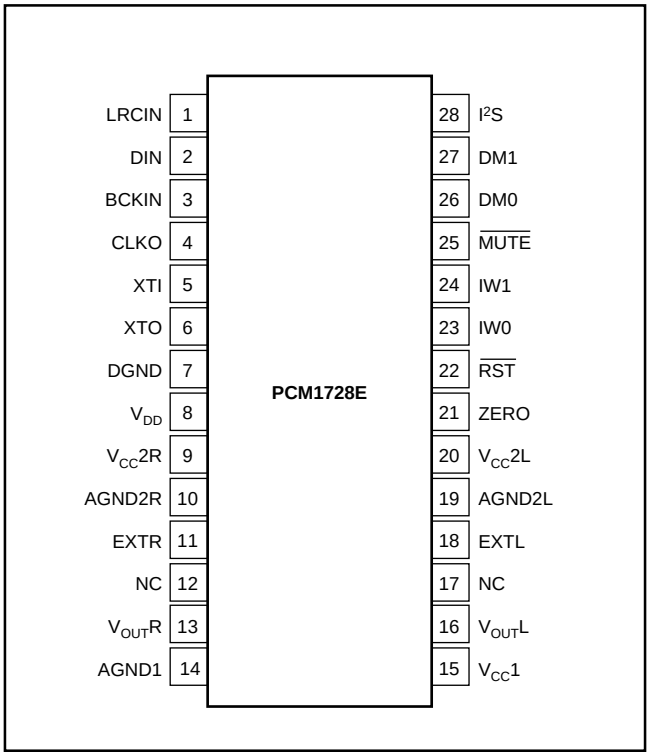
SPECIFICATIONS

All specifications at +25°C, $+V_{CC}$ = $+V_{DD}$ = +5V, f_S = 44.1kHz, and 24-bit input data, SYSCLK = 384f_S, unless otherwise noted.

PARAMETER	CONDITIONS	PCM1728 MIN	PCM1728 TYP	PCM1728 MAX	UNITS
RESOLUTION			24		Bits
DATA FORMAT					
Audio Data Interface Format			Standard/I²S		
Data Bit Length			16/20/24 Selectable		
Audio Data Format			MSB-First, Two's Binary Comp		
Sampling Frequency (f_S)		16		96	kHz
System Clock Frequency(1)			256/384/512/768f_S		
DIGITAL INPUT/OUTPUT LOGIC LEVEL					
Input Logic Level V_{IH}		2.0			V
V_{IL}				0.8	V
Output Logic Level (CLKO) V_{OH}	I_{OH} = 2mA	4.5			V
V_{OL}	I_{OL} = 4mA			0.5	V
CLKO PERFORMANCE(2)					
Output Rise Time	20 ~ 80% V_{DD}, 10pF		5.5		ns
Output Fall Time	80 ~ 20% V_{DD}, 10pF		4		ns
Output Duty Cycle	10pF Load		37		%
DYNAMIC PERFORMANCE(3) (24-Bit Data)					
THD+N V_O = 0dB	f_S = 44.1kHz		–97	–90	dB
	f_S = 96kHz		–94		dB
V_O = –60dB	f_S = 44.1kHz		–42		dB
Dynamic Range	f_S =44.1kHz EIAJ A-weighted	98	106		dB
	f_S = 96kHz A-weighted		103		dB
Signal-to-Noise Ratio	f_S =44.1kHz EIAJ A-weighted	98	106		dB
	f_S = 96kHz A-weighted		103		dB
Channel Separation	f_S = 44.1kHz	96	102		dB
	f_S = 96kHz		101		dB
DYNAMIC PERFORMANCE(3) (16-Bit Data)					
THD+N V_O = 0dB	f_S = 44.1kHz		–94		dB
	f_S = 96kHz		–92		dB
Dynamic Range	f_S = 44.1kHz EIAJ A-weighted		98		dB
	f_S = 96kHz A-weighted		97		dB
DC ACCURACY					
Gain Error			±1.0	±3.0	% of FSR
Gain Mismatch: Channel-to-Channel			±1.0	±3.0	% of FSR
Bipolar Zero Error	V_O = 0.5V_{CC} at Bipolar Zero		±30	±60	mV
ANALOG OUTPUT					
Output Voltage	Full Scale (0dB)		0.62 V_{CC}		Vp-p
Center Voltage			0.5 V_{CC}		V
Load Impedance	AC Load	5			kΩ
DIGITAL FILTER PERFORMANCE					
Filter Characteristics					
Passband	±0.002dB			0.454f_S	
	–3dB			0.490f_S	
Stopband		0.546f_S			
Passband Ripple				±0.002	dB
Stopband Attenuation	Stop Band = 0.546f_S	–75			dB
	Stop Band = 0.567f_S	–82			dB
Delay Time			30/f_S		sec
De-emphasis Error				±0.1	dB
INTERNAL ANALOG FILTER					
–3dB Bandwidth			100		kHz
Passband Response	f = 20kHz		–0.16		dB
POWER SUPPLY REQUIREMENTS					
Voltage Range	V_{DD}, V_{CC}	4.5	5	5.5	VDC
Supply Current: I_{CC} +I_{DD}	f_S = 44.1kHz		32	45	mA
	f_S = 96kHz		45		mA
Power Dissipation	f_S = 44.1kHz		160	225	mW
	f_S = 96kHz		225		mW
TEMPERATURE RANGE					
Operation		–25		+85	°C
Storage		–55		+100	°C

NOTES: (1) Refer section of system clock. (2) External buffer is recommended. (3) Dynamic performance specs are tested with 20kHz low pass filter and THD+N specs are tested with 30kHz LPF, 400Hz HPF, Average Mode.

PIN CONFIGURATION



PACKAGE INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)
PCM1728E	28-Pin SSOP	324

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	+6.5V
$+V_{CC}$ to $+V_{DD}$ Difference	±0.1V
Input Logic Voltage	–0.3V to (V_{DD} + 0.3V)
Input Current (except power supply)	±10mA
Power Dissipation	400mW
Operating Temperature Range	–25°C to +85°C
Storage Temperature	–55°C to +125°C
Lead Temperature (soldering, 5s)	+260°C

PIN ASSIGNMENTS

PIN	NAME	I/O	DESCRIPTION
1	LRCIN	IN	Left and Right Clock Input. This clock is equal to the sampling rate - f_S.(1)
2	DIN	IN	Serial Audio Data Input(1)
3	BCKIN	IN	Bit Clock Input for Serial Audio Data.(1)
4	CLKO	OUT	Buffered Output of Oscillator. Equivalent to System Clock.
5	XTI	IN	Oscillator Input (External Clock Input)
6	XTO	OUT	Oscillator Output
7	DGND	—	Digital Ground
8	V_{DD}	—	Digital Power +5V
9	V_{CC}2R	—	Analog Power +5V
10	AGND2R	—	Analog Ground
11	EXTR	OUT	Rch, Common Pin of Analog Output Amp
12	NC	—	No Connection
13	V_{OUT}R	OUT	Rch, Analog Voltage Output of Audio Signal
14	AGND1	—	Analog Ground
15	V_{CC}1	—	Analog Power +5V
16	V_{OUT}L	OUT	Lch, Analog Voltage Output of Audio Signal
17	NC	—	No Connection
18	EXTL	OUT	Lch, Common Pin of Analog Output Amp
19	AGND2L	—	Analog Ground
20	V_{CC}2L	—	Analog Power +5V
21	ZERO	OUT	Zero Data Flag
22	$\overline{\text{RST}}$	IN	Reset. When this pin is LOW, the DF and modulators are held in reset.(2)
23	IW0	IN	Input Format Selection(3)
24	IW1	IN	Input Format Selection(3)
25	$\overline{\text{MUTE}}$	IN	Mute Control
26	DM0	IN	De-emphasis Selection 1(2)
27	DM1	IN	De-emphasis Selection 2(2)
28	I²S	IN	Input Format Selection(2)

NOTES: (1) Pins 1, 2, 3; Schmitt Trigger input. (2) Pins 22, 25, 26, 27, 28; Schmitt Trigger input with pull-up resister. (3) Pins 23, 24; Schmitt Trigger input with pull-down resister.

ELECTROSTATIC DISCHARGE SENSITIVITY

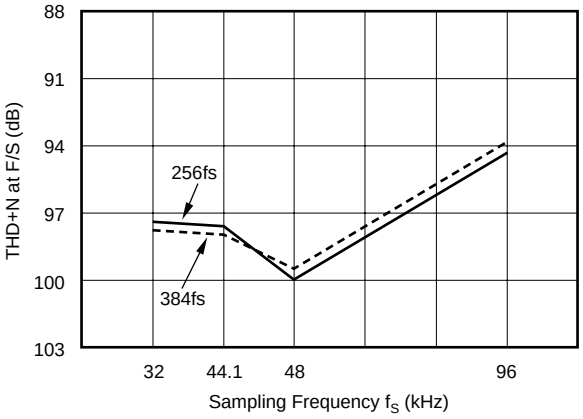
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

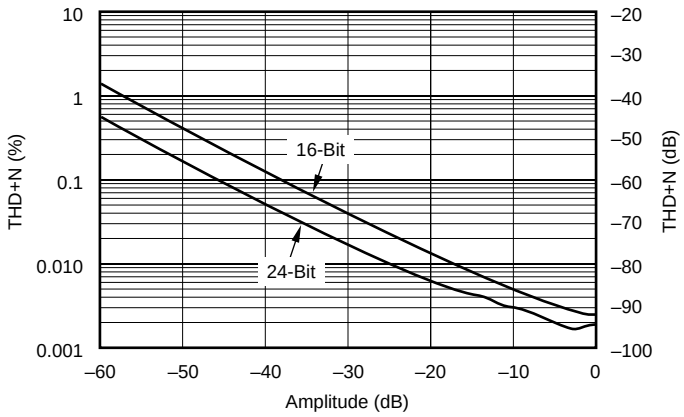
TYPICAL PERFORMANCE CURVES

All specifications at +25°C, $+V_{CC}$ = $+V_{DD}$ = +5V, f_S = 44.1kHz, and 24-bit input data, SYSCLK = 384f_S, unless otherwise noted.

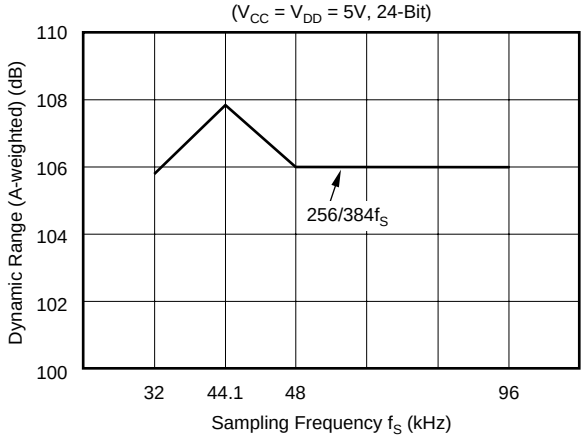
THD+N vs SAMPLING FREQUENCY
(V_{CC} = V_{DD} = 5V, 24-Bit)



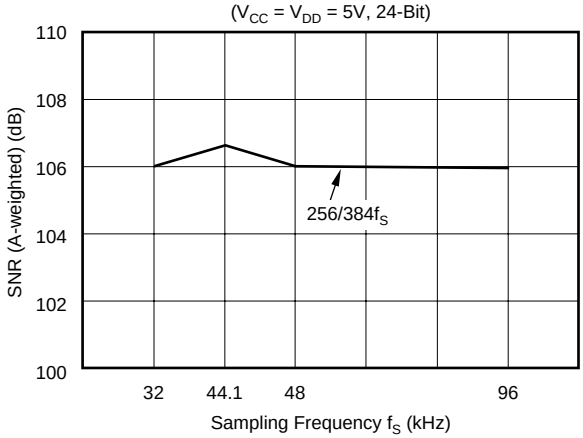
THD+N vs LEVEL
(f_S = 44.1kHz)



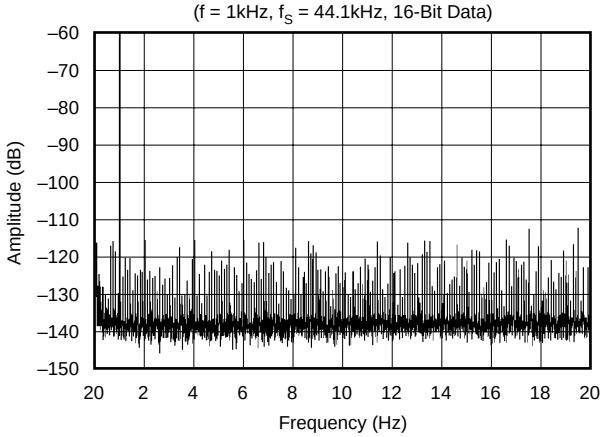
DYNAMIC RANGE vs SAMPLING FREQUENCY
(V_{CC} = V_{DD} = 5V, 24-Bit)



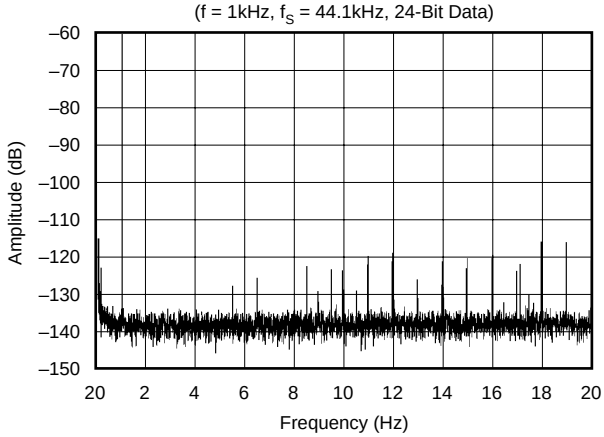
SNR vs SAMPLING FREQUENCY
(V_{CC} = V_{DD} = 5V, 24-Bit)



–60dB OUTPUT SPECTRUM
(f = 1kHz, f_S = 44.1kHz, 16-Bit Data)

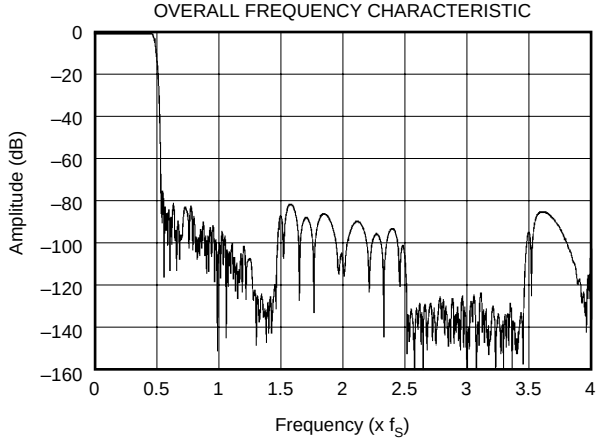


–60dB OUTPUT SPECTRUM
(f = 1kHz, f_S = 44.1kHz, 24-Bit Data)

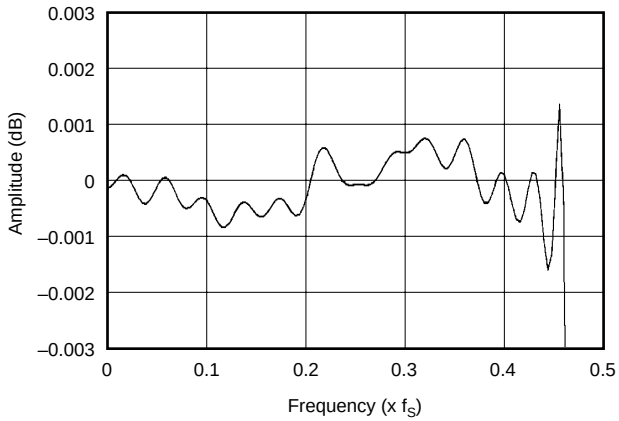


TYPICAL PERFORMANCE CURVES (CONT)

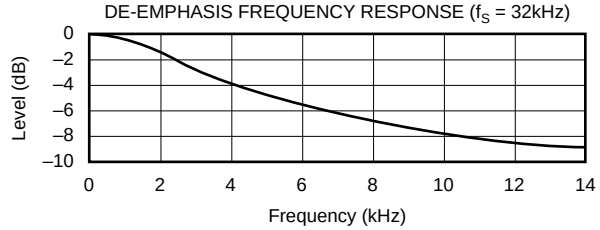
OVERALL FREQUENCY CHARACTERISTIC



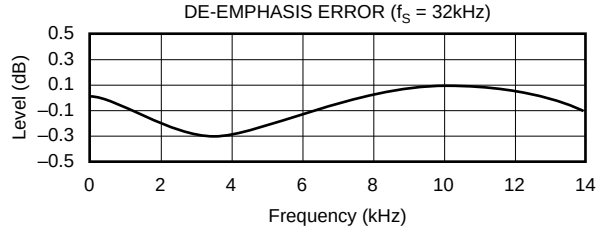
PASSBAND RIPPLE CHARACTERISTIC



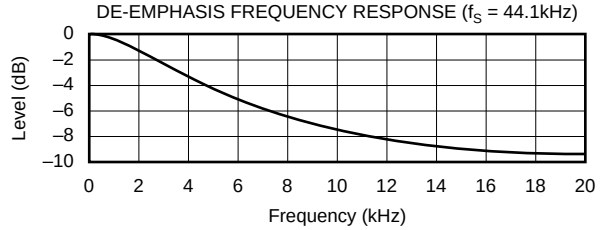
DE-EMPHASIS FREQUENCY RESPONSE (f_S = 32kHz)



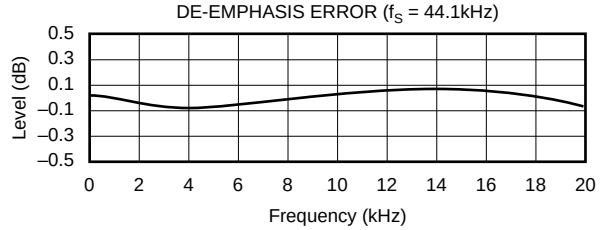
DE-EMPHASIS ERROR (f_S = 32kHz)



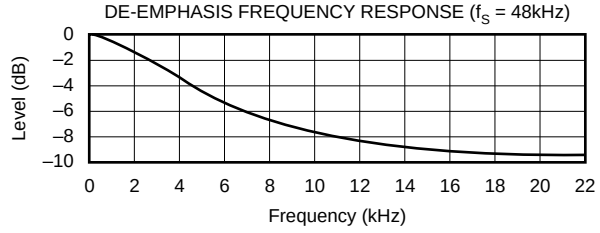
DE-EMPHASIS FREQUENCY RESPONSE (f_S = 44.1kHz)



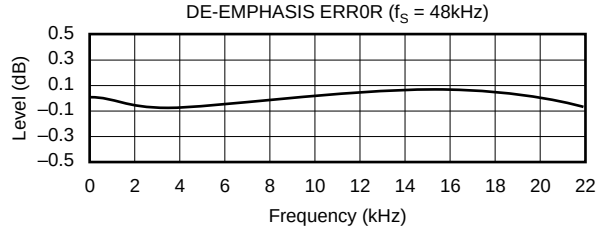
DE-EMPHASIS ERROR (f_S = 44.1kHz)



DE-EMPHASIS FREQUENCY RESPONSE (f_S = 48kHz)



DE-EMPHASIS ERR0R (f_S = 48kHz)



SYSTEM CLOCK

The system clock for PCM1728 must be either $256f_S$, $384f_S$, $512f_S$ or $768f_S$, where f_S is the audio sampling frequency (typically 32kHz, 44.1kHz, 48kHz, or 96kHz). But $768f_S$ at 96kHz is not accepted.

The system clock can be either a crystal oscillator placed between XTI (pin 5) and XTO (pin 6), or an external clock input to XTI. If an external system clock is used, XTO is open (floating). Figure 1 illustrates the typical system clock connections.

PCM1728 has a system clock detection circuit which automatically senses if the system clock is operating at $256f_S$ ~ $768f_S$. The system clock should be synchronized with LRCIN (pin 1) clock. LRCIN (left-right clock) operates at the sampling frequency f_S. In the event these clocks are not synchronized, PCM1728 can compensate for the phase difference internally. If the phase difference between left-right and system clocks is greater than 6-bit clocks (BCKIN), the synchronization is performed internally. While the synchronization is processing, the analog output is forced to a DC level at bipolar zero. The synchronization typically occurs in less than 1 cycle of LRCIN.

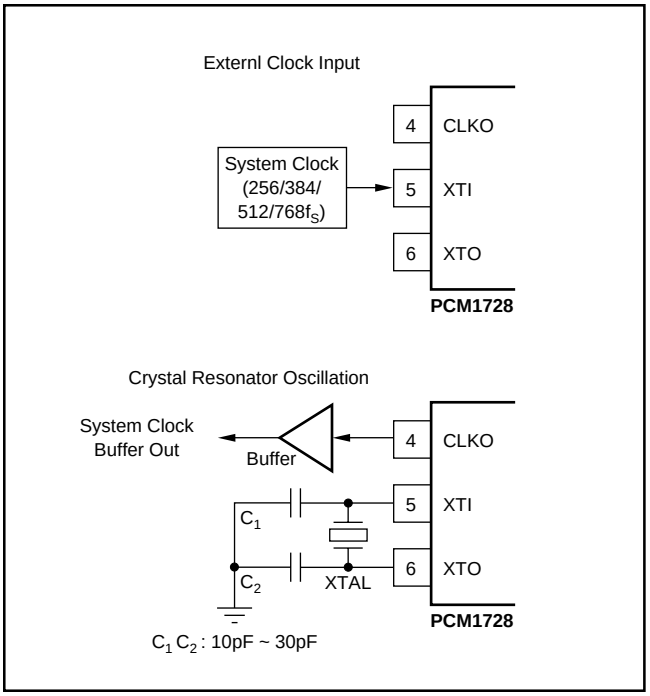


FIGURE 1. System Clock Connection.

Typical input system clock frequencies to the PCM1728 are shown in Table I, also, external input clock timing requirements are shown in Figure 2.

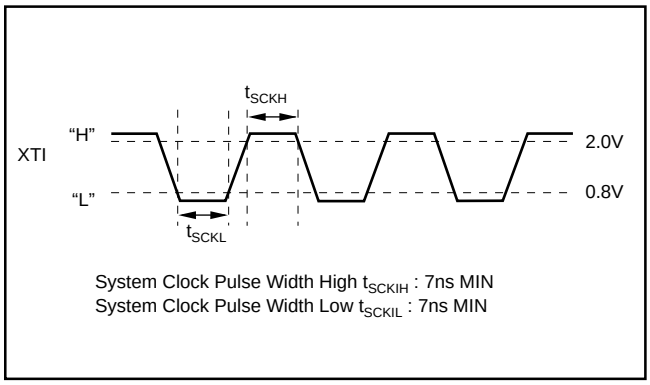


FIGURE 2. XTI Clock Timing.

DATA INTERFACE FORMATS

Digital audio data is interfaced to PCM1728 on pins 1, 2, and 3, LRCIN (left-right clock), DIN (data input) and BCKIN (bit clock). PCM1728 can accept both standard, I^2S, and left justified data formats.

Figure 3 illustrates acceptable input data formats. Figure 4 shows required timing specification for digital audio data.

Reset

PCM1728 has both internal power-on reset circuit and the $\overline{RST}$ pin (pin 22), which accepts an external forced reset by $\overline{RST}$ = LOW. For internal power on reset, initialization is done automatically at power on V_{DD} >2.2V (typ). During internal reset = LOW, the output of the DAC is invalid and the analog outputs are forced to $V_{CC}/2$. Figure 5 illustrates the timing of the internal power on reset.

PCM1728 accepts an external forced reset when $\overline{RST}$ = LOW. When $\overline{RST}$ = LOW, the output of the DAC is invalid and the analog outputs are forced to $V_{CC}/2$ after internal initialization (1024 system clocks count after $\overline{RST}$ = HIGH.) Figure 6 illustrates the timing of the $\overline{RST}$ pin.

Zero Out (pin 21)

If the input data is continuously zero for 65536 cycles of BCK, an internal FET is switched to "ON". The drain of the internal FET is the zero-pin, it will enable "wired-or" with external circuit.

SAMPLING RATE FREQUENCY (f_S) - LRCIN	SYSTEM CLOCK FREQUENCY - MHz			
	$256f_S$	$384f_S$	$512f_S$	$768f_S$
32kHz	8.1920	12.2880	16.3840	24.5760
44.1kHz	11.2896	16.9340	22.5792	33.8688(1)
48kHz	12.2880	18.4320	24.5760	36.8640(1)
96kHz	24.5760	36.8640(1)	49.1520(1)	—

NOTE: (1) The internal crystal oscillator frequency cannot be larger than 24.576MHz.

TABLE I. Typical System Clock Frequency.

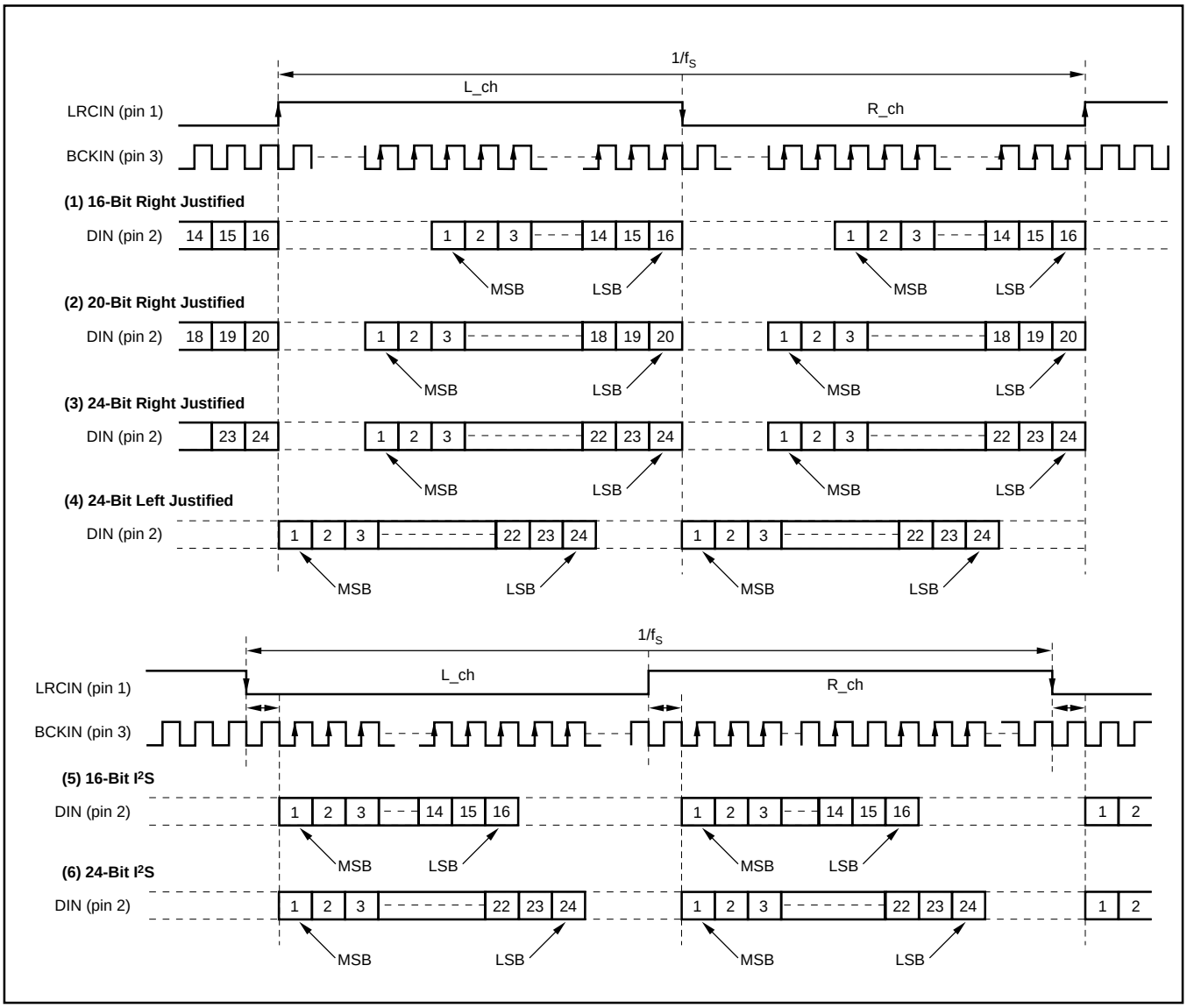
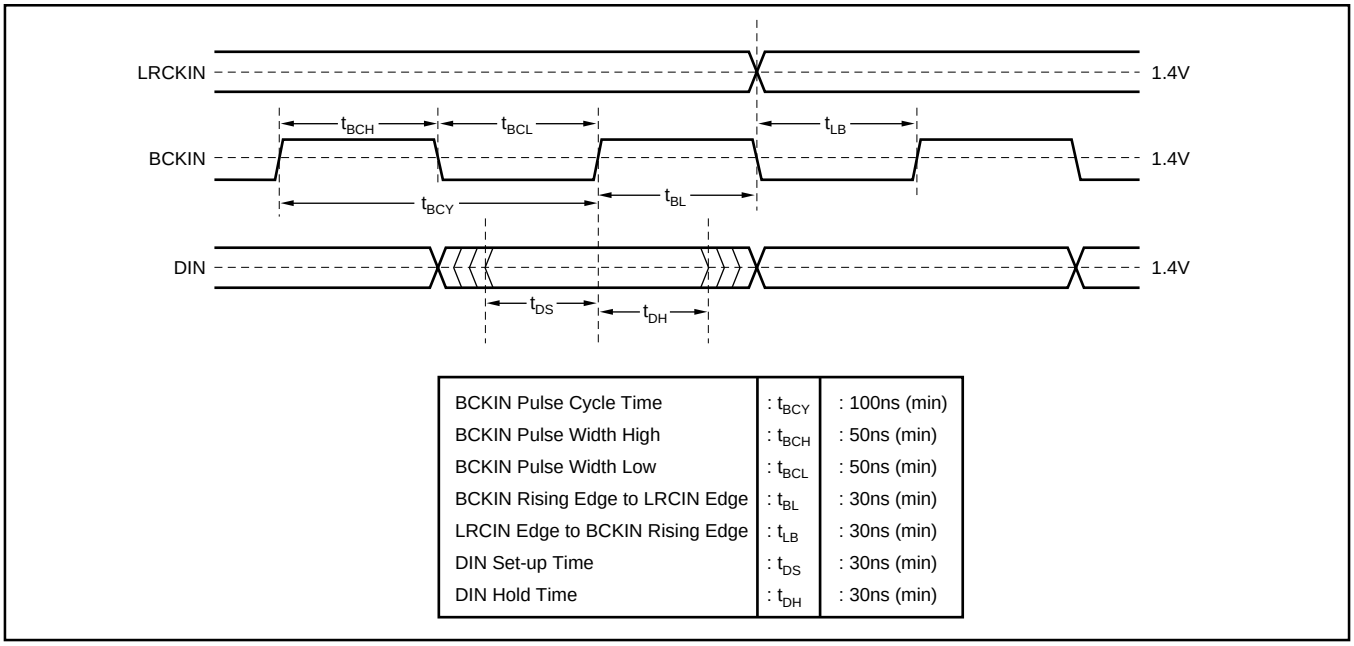


FIGURE 3. Audio Data Input Formats.



BCKIN Pulse Cycle Time	: t_{BCY}	: 100ns (min)
BCKIN Pulse Width High	: t_{BCH}	: 50ns (min)
BCKIN Pulse Width Low	: t_{BCL}	: 50ns (min)
BCKIN Rising Edge to LRCIN Edge	: t_{BL}	: 30ns (min)
LRCIN Edge to BCKIN Rising Edge	: t_{LB}	: 30ns (min)
DIN Set-up Time	: t_{DS}	: 30ns (min)
DIN Hold Time	: t_{DH}	: 30ns (min)

FIGURE 4. Audio Data Input Timing Specification.

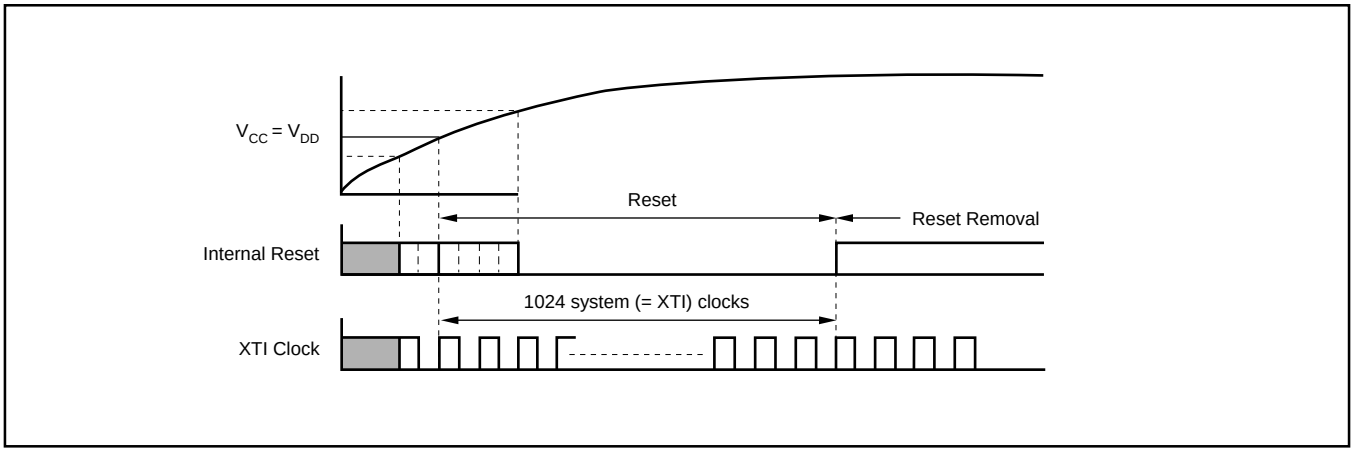


FIGURE 5. Internal Power-On Reset Timing.

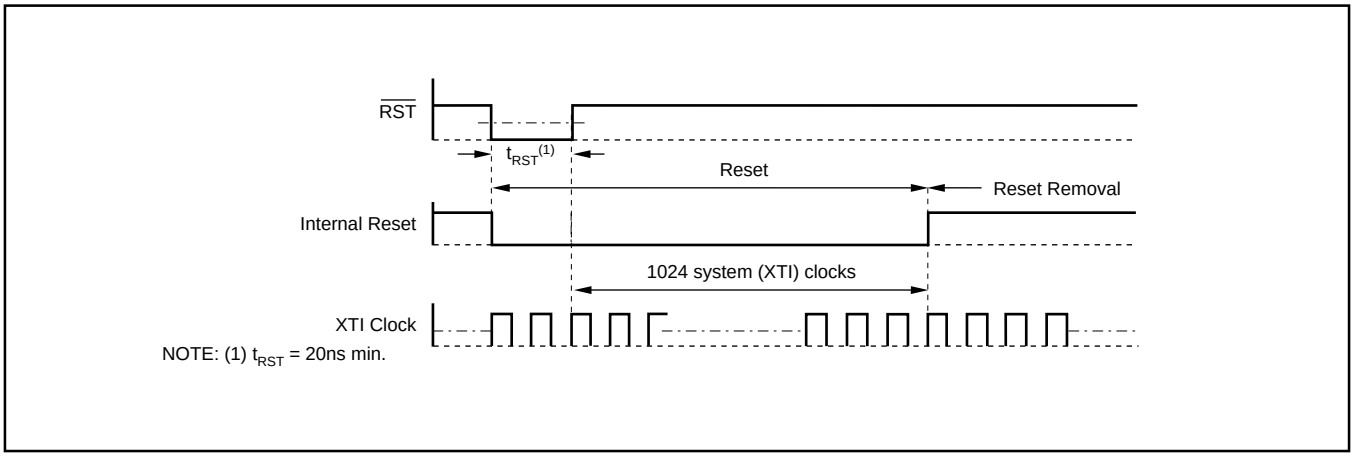


FIGURE 6. External Forced Reset Timing.

FUNCTIONAL DESCRIPTION

PCM1728 has several built-in functions including digital input data format selection, soft mute, and digital de-emphasis. These functions are hardware controlled where static control signals are used on pin 28 (I^2S), pin 27 (DM1), pin 26 (DM0), pin 25 (MUTE), pin 24 (IW1), and pin23 (IW0).

DATA FORMAL SELECTION

PCM audio data format can be selected by pin 28 (I^2S), pin 24 (IW1), and pin 23 (IW0), as shown in Table II.

IW1	IW0	I^2S	AUDIO INTERFACE
0	0	0	16-Bit Standard, Right-Justified
0	1	0	20-Bit Standard, Right-Justified
1	0	0	24-Bit Standard, Right-Justified
1	1	0	24-Bit Left-Justified, MSB-First
0	0	1	16-Bit I^2S
0	1	1	24-Bit I^2S
1	0	1	Reserved
1	1	1	Reserved

TABLE II. Data Format Control.

SOFT MUTE

Soft Mute function can be controlled by $\overline{MUTE}$ (pin 25).

$\overline{MUTE}$ (Pin 25)	SOFT MUTE
L	Mute ON
H	Mute OFF (Normal Operation)

TABLE III. Soft Mute Control.

DE-EMPHASIS CONTROL

De-emphasis control can be selected by DM1 (pin 27) and DM0 (pin 26).

DM1 (Pin 27)	DM0 (Pin 26)	DE-EMPHASIS
L	L	OFF
L	H	48kHz
H	L	44.1kHz
H	H	32kHz

TABLE IV. De-emphasis Control.

THEORY OF OPERATION

The delta-sigma section of PCM1728 is based on an 8-level amplitude quantizer and a 4th-order noise shaper. This section converts the oversampled input data to 8-level delta-sigma format.

This newly developed, "Enhanced Multi-level Delta-Sigma" architecture achieves high-grade audio dynamic performance and sound quality.

A block diagram of the 8-level delta-sigma modulator is shown in Figure 7. This 8-level delta-sigma modulator has the advantage of stability and clock jitter sensitivity over the typical one-bit (2-level) delta-sigma modulator.

The combined oversampling rate of the delta-sigma modulator and the internal 8-times interpolation filter is $64f_S$ for all system clock ratios ($256/384/512/768f_S$).

The theoretical quantization noise performance of the 8-level delta-sigma modulator is shown in Figure 8. This enhanced multi-level delta-sigma architecture also has advantages for input clock jitter sensitivity due to the multi-level quantizer, simulated jitter sensitivity is shown in Figure 9.

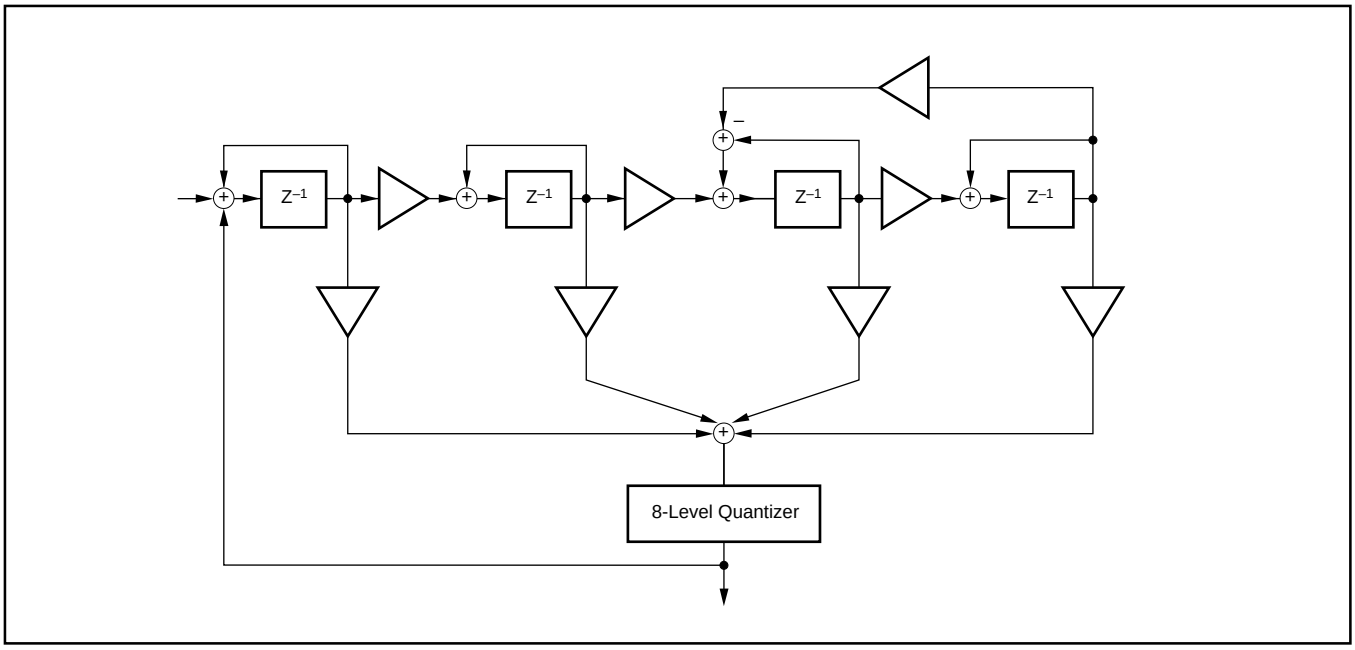


FIGURE 7. 8-Level Delta-Sigma Modulator.

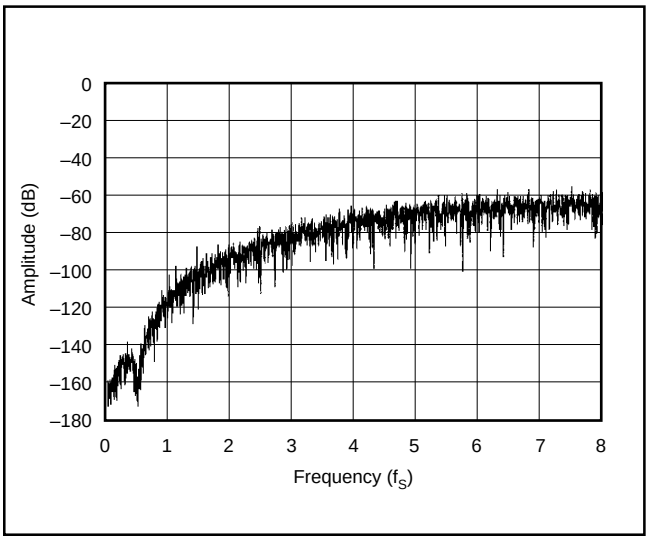


FIGURE 8. Quantization Noise Spectrum.

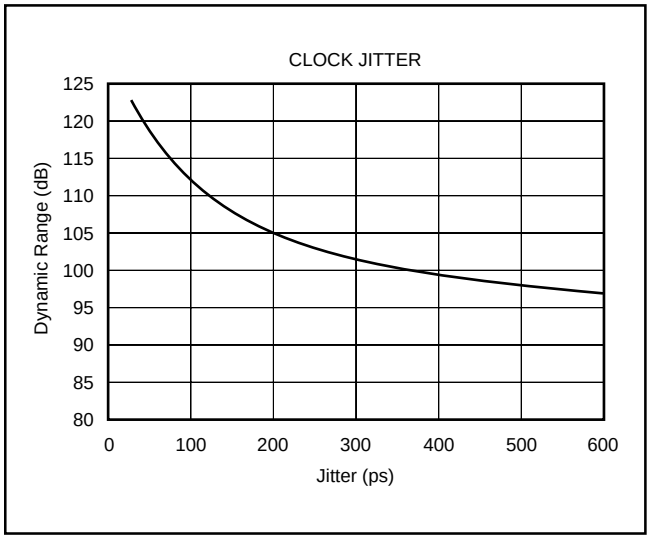


FIGURE 9. Jitter Sensitivity.

APPLICATION CONSIDERATIONS

DELAY TIME

There is a finite delay time in delta-sigma converters. In A/D converters, this is commonly referred to as latency. For a delta-sigma D/A converter, delay time is determined by the order number of the FIR filter stage, and the chosen sampling rate. The following equation expresses the delay time of PCM1728:

$$T_D = 30 \times 1/f_S$$

For f_S = 44.1kHz, T_D = 30/44.1kHz = 680µs

Applications using data from a disc or tape source, such as CD audio, DVD audio, Video CD, DAT, Minidisc, etc., generally are not affected by delay time. For some professional applications such as broadcast audio for studios, it is important for total delay time to be less than 2ms.

OUTPUT FILTERING

For testing purposes all dynamic tests are done on the PCM1728 using a 20kHz low pass filter. This filter limits the measured bandwidth for THD+N, etc. to 20kHz. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the specifications. The low pass filter removes out of band noise. Although it is not audible, it may affect dynamic specification numbers.

The performance of the internal low pass filter from DC to 40kHz is shown in Figure 10. The higher frequency roll-off of the filter is shown in Figure 11. If the user's application has the PCM1728 driving a wideband amplifier, it is recommended to use an external low pass filter.

BYPASSING POWER SUPPLIES

The power supplies should be bypassed as close as possible to the unit. Refer to Figure 12 for optimal values of bypass capacitors.

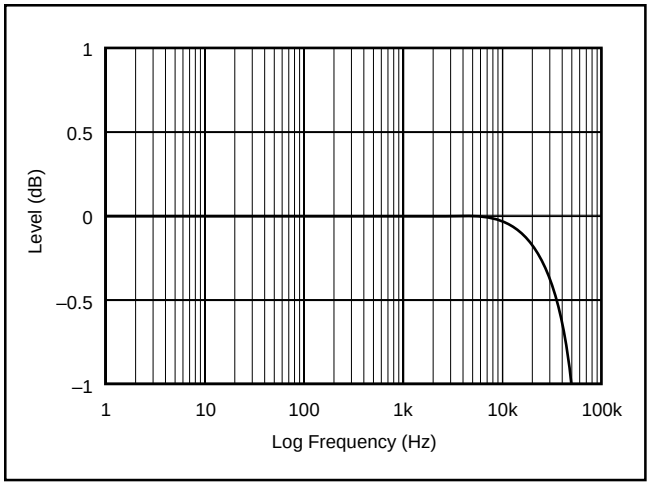


FIGURE 10. Low Pass Filter Response.

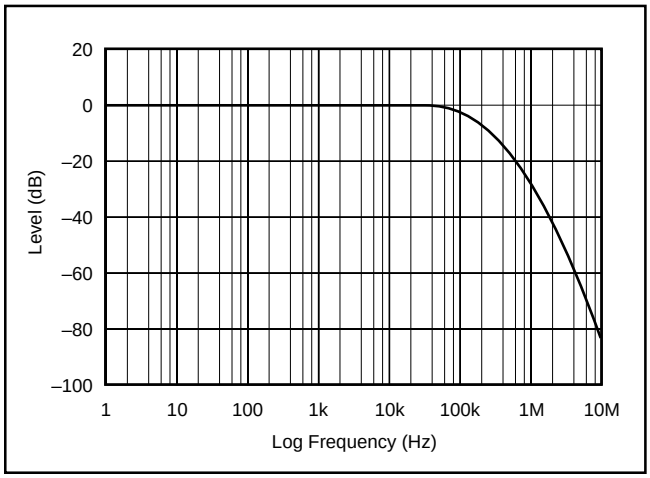


FIGURE 11. Low Pass Filter Response.

POWER SUPPLY CONNECTIONS

PCM1728 has four power supply pin for digital (V_{DD}), and analog (V_{CC}). Each connection also has a separate ground. If the power supplies turn on at different times, there is a possibility of a latch-up condition. To avoid this condition, it is recommended to have a common connection between the digital and analog power supplies. If separate supplies are used without a common connection, the delta between the two supplies during ramp-up time must be less than 0.1V.

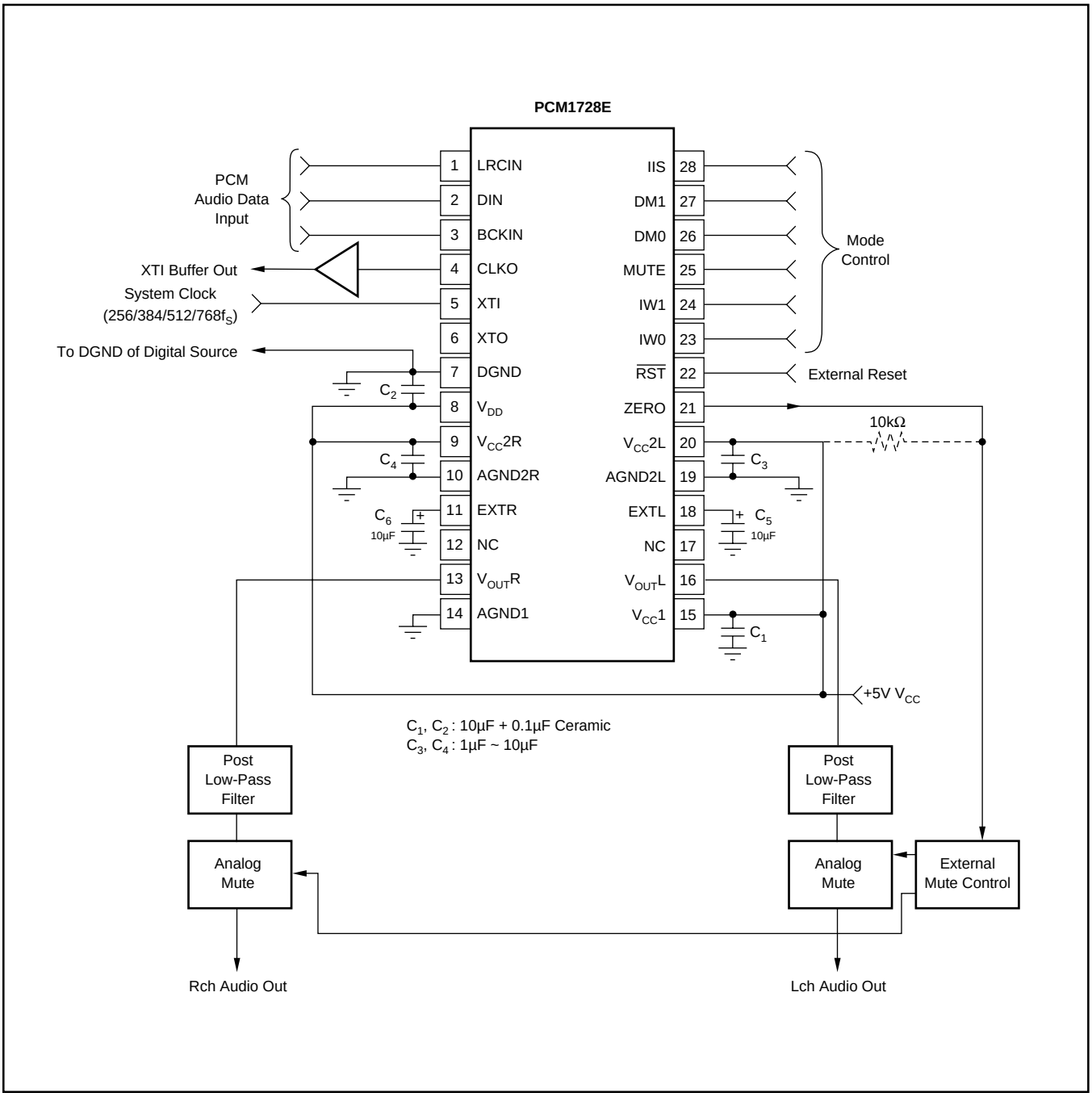


FIGURE 12. Typical Circuit Connection Diagram.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCM1728E	ACTIVE	SSOP	DB	28	47	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM		PCM1728E	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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