4-Channel Back-Boost White LED Driver with Integrated FET for up to 32 LEDs

BD81A04EFV-M

●General Description

BD81A04EFV-M is a white LED driver with the capability of withstanding high input voltage (40V MAX).This driver has 4ch constant-current drivers integrated in 1-chip, which each channel can draw up to 120mA max, so that high brightness LED driving can be realized. Furthermore, a current-mode buck-boost DC/DC controller is also integrated to achieve stable operation against unstable car-battery voltage input and also to remove the constraint of the number of LEDs in series connection. The brightness can be controlled by PWM techniques. The set board can be made a conserve area because MOSFET is built into

●Features

- Integrated buck-boost current-mode DC/DC controller
- Four integrated LED current driver channels (120 mA max. each channel)
- PWM Light Modulation
- Built-in protection functions (UVLO, OVP, TSD, OCP, SCP)
- Abnormal status detection function (OPEN/ SHORT)

●Key Specifications

■ Power supply voltage	4.5 to 35 [V]
■ LED output current accuracy	±3.0 % @50mA
■ Oscillation frequency	200 to 2200 KHz
■ Operating temperature range	-40 to 85 ℃
■ PWM minimum pulse width	1usec
■ LED maximum output current	120mA／ch

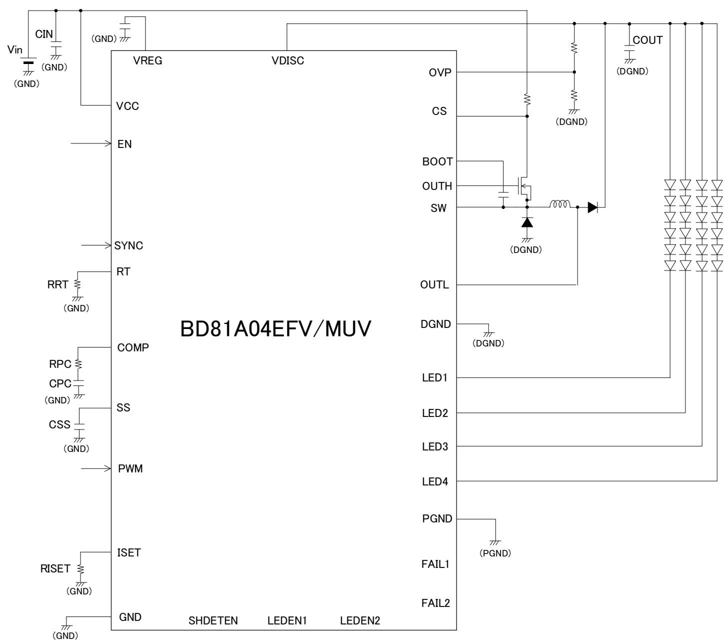
●Packages

HTSSOP-B28 6.5㎜×6.4㎜×1.0㎜

●Applications

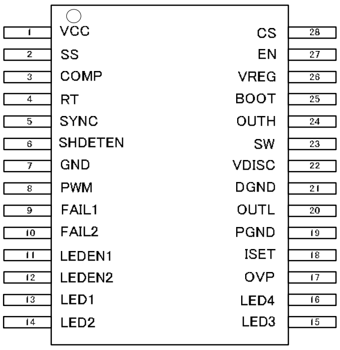
For display audio, Small and medium-sized type LCD panel

●Typical Application Circuits



○Product structure：Silicon monolithic integrated circuit
○This product is not designed protection against radioactive rays.

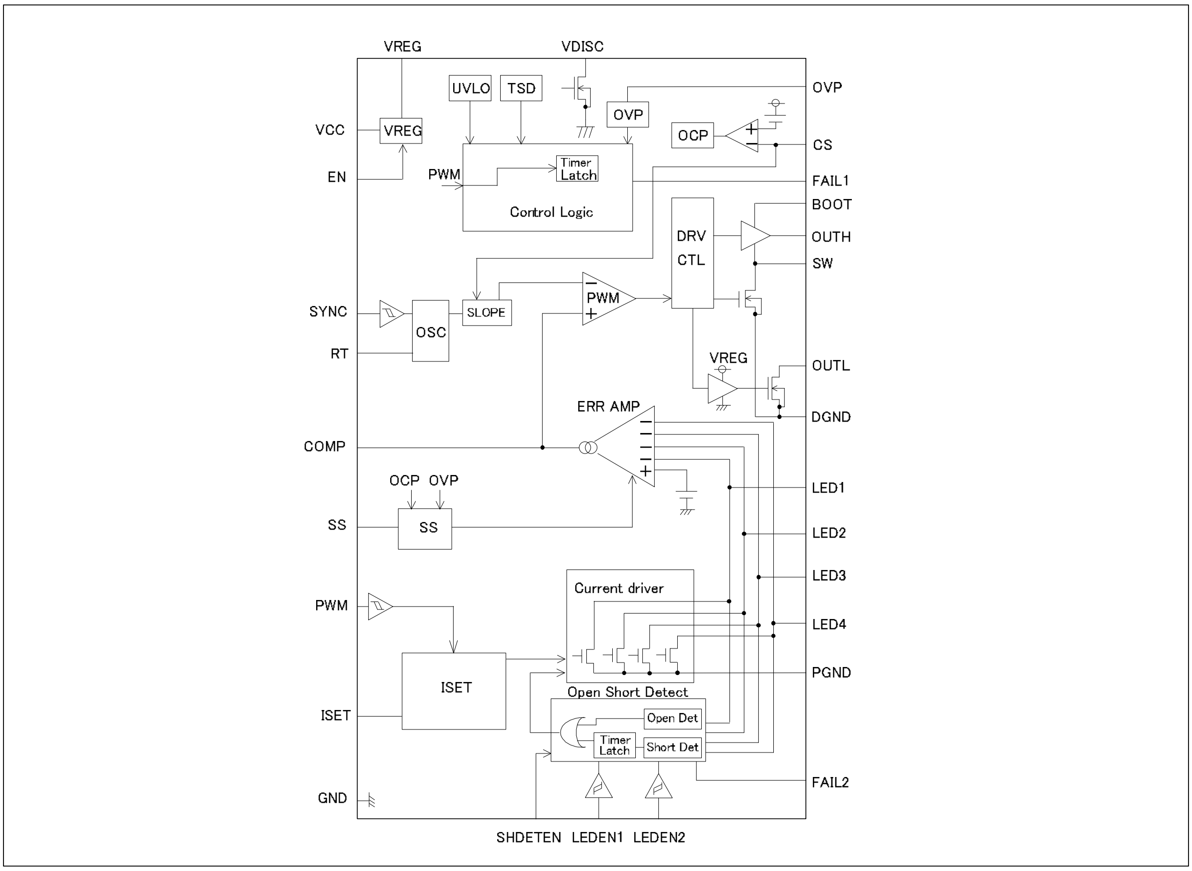
●Pin Configuration



●Pin Description

HTSSOP -B28	VQFN028 V5050	Symbol	Function
1	19	VCC	Input power supply
2	20	SS	Soft start time-setting capacitance input
3	21	COMP	Error amplifier output
4	22	RT	Oscillation frequency-setting resistance input
5	23	SYNC	External synchronization signal input
6	24	SHDETEN	LED short detection enable signal
7	25	GND	Small-signal GND
8	26	PWM	PWM light modulation input
9	27	FAIL1	Failure signal output
10	28	FAIL2	LED open/short detection signal output
11	1	LEDEN1	LED output enable input 1
12	2	LEDEN2	LED output enable input 2
13	3	LED1	LED output 1
14	4	LED2	LED output 2
15	5	LED3	LED output 3
16	6	LED4	LED output 4
17	7	OVP	Over voltage detection input
18	8	ISET	LED output current-setting resistance input
19	9	PGND	LED output GND
20	10	OUTL	Low-side internal MOSFET Drain output
21	11	DGND	DCDC output GND
22	12	VDISC	VOUT discharge signal
23	13	SW	High-side external MOSFET Source pin
24	14	OUTH	High-side external MOSFET Gate output
25	15	BOOT	High-side external MOSFET power supply pin
26	16	VREG	Internal reference voltage output
27	17	EN	Enable input
28	18	CS	DC/DC current sence pin

●Block Diagram



● **Absolute maximum ratings** (Ta=25℃)

Parameter	Symbol	Rating	Unit
Power supply voltage	VCC	40	V
BOOT ,OUTH Voltage	VBOOT, VOUTH	45	V
SW,CS,OUTL Voltage	VSW, VCS, VOUTL	40	V
BOOT-SW Voltage	VBOOT-SW	7	V
LED output, VDISC voltage	VLED1,2,3,4, VDISC	40	V
VREG, OVP, FAIL1, FAIL2, LEDEN1, LEDEN2 ISET, VDAC, PWM, SS, COMP, RT, SYNC, EN, SHDETEN Voltage	VVREG, VOVP, VFAIL1, VFAIL2, VLEDEN1, VLEDEN2, VISET, VPWM, VSS, VCOMP, VRT, VSYNC, VEN, VSHDETEN	-0.3～7 < VCC	V
Power Consumption	Pd	1.45 ※1	W
Operating temperature range	Topr	-40～+85	℃
Storage temperature range	Tstg	-55～+150	℃
LED maximum output current	ILED	120 ※2 ※3	mA
Junction temperature	Tjmax	150	℃

※1 IC mounted on glass epoxy board measuring 70mm×70mm×1.6mm, power dissipated at a rate of 11.6mw/℃ at temperatures above 25℃.

※2 Dispersion figures for LED maximum output current and V_F are correlated. Please refer to data on separate sheet.

※3 Amount of current per channel.

● **Operating conditions** (Ta=25℃)

Parameter	Symbol	Limits	Unit
Power supply voltage	VCC	4.5～35	V
Oscillating frequency range	FOSC	200～2200	KHz
External synchronization frequency range ※4 ※5	FSYNC	fosc～2200	KHz
External synchronization pulse duty range	FSDUTY	40～60	%

※4 Connect SYNC to GND or OPEN when not using external frequency synchronization.

※5 Do not switch between internal and external synchronization when an external synchronization signal is input to the device.

●**Electrical Characteristics** (unless otherwise specified, VCC=12V Ta=25℃)

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max.		
Circuit current	ICC	-	-	10	mA	EN=Hi, SYNC=Hi, RT=OPEN PWM=Low,ISET=OPEN,CIN=10μF
Standby current	IST	-	-	10	μA	EN=Low
[VREG Block (VREG)]						
Reference voltage	VREG	4.5	5	5.5	V	IREG=-5mA, CREG=2.2μF
[OUTH Block						
OUTHhigh-side ON resistance	RONHH	1.5	3.5	7.0	Ω	ION=-10mA
OUTH low-side ON resistance	RONHL	1.0	2.5	5.0	Ω	ION=10mA
OCP voltage	VOLIMIT	VCC-0.66	VCC-0.6	VCC-0.54	V	
[OUTL Block]						
OUTL ON resistance	RONL	0.44	0.8	1.15	Ω	ION=10mA
[SW Block]						
SW ON resistance	RON_SW	5.0	10.0	15.0	Ω	ION_SW=10mA
[Error Amplifie Block]						
LED control voltage	VLED	0.9	1.0	1.1	V	
COMP sink current	ICOMP SINK	20	80	160	μA	VLED=2V, Vcomp=1V
COMP source current	ICOMP SOURCE	-160	-80	-20	μA	VLED=0V, Vcomp=1V
[Oscillator Block]						
Oscillating frequency1	FOSC1	285	300	315	KHz	RT=27KΩ
Oscillating frequency2	FOSC2	1800	2000	2200	KHz	RT=3.9KΩ
[OVP Block]						
OVP voltage	VOVP	1.9	2.0	2.1	V	VOVP=Sweep up
OVP hysteresis width	VOHYS	0.45	0.55	0.65	V	VOVP=Sweep down
SCP Latch OFF Delay Time	TSCP	70	100	130	ms	RT=27KΩ
[UVLO Block]						
UVLO voltage	VUVLO	3.2	3.5	3.8	V	VCC : Sweep down
UVLO hysteresis width	VUHYS	250	500	750	mV	VCC : Sweep up,VREG>3.5V
[LED Output Block]						
LEDcurrentrelativedispersionwidth	ΔILED1	-3	-	+3	%	ILED=50mA, ΔILED1=(ILED/ILED_AVG-1)×100
LEDcurrentabsolutedispersionwidth	ΔILED2	-3	-	+3	%	ILED=50mA, ΔILED2=(ILED/50mA-1)×100
ISET voltage	VISET	0.9	1.0	1.1	V	RISET=100KΩ
PWM minimum pulse width	Tmin	1	-	-	μs	FPWM=150Hz, ILED=100mA
PWM maximum duty	Dmax	-	-	100	%	FPWM=150Hz, ILED=50mA
PWM frequency	FPWM	-	-	20	KHz	Duty=2%, ILED=50mA
Open detection voltage	VOPEN	0.2	0.3	0.4	V	VLED= Sweep down
LED Short detection voltage	VSHORT	4.2	4.5	4.8	V	VLED= Sweep up
LED Short Latch OFF Delay Time	TSHORT	70	100	130	ms	RT=27KΩ
PWM Latch OFF Delay Time	TPWM	70	100	130	ms	RT=27KΩ
[Logic Inputs (EN, SYNC, SHDETEN, PWM, LEDEN1, LEDEN2)]						
Input HIGH voltage	VINH	2.1	-	5.5	V	
Input LOW voltage	VINL	GND	-	0.8	V	
Input current	IIN	25	50	100	μA	VIN=5V(EN,SYNC,PWM, SHDETEN, LEDEN1, LEDEN2)
[FAIL Output (open drain)]						
FAIL LOW voltage	VOL	-	0.1	0.2	V	IOL=0.1mA

● **Reference data** (unless otherwise specified, Ta=25℃)

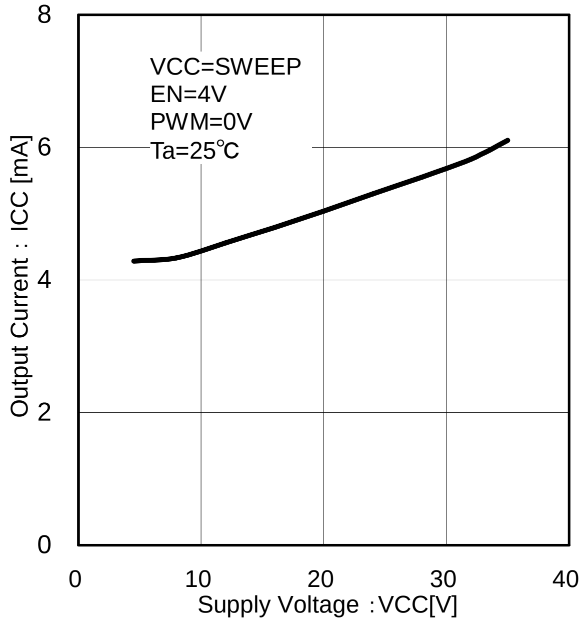


Fig.1 Circuit Current
(Switching OFF)

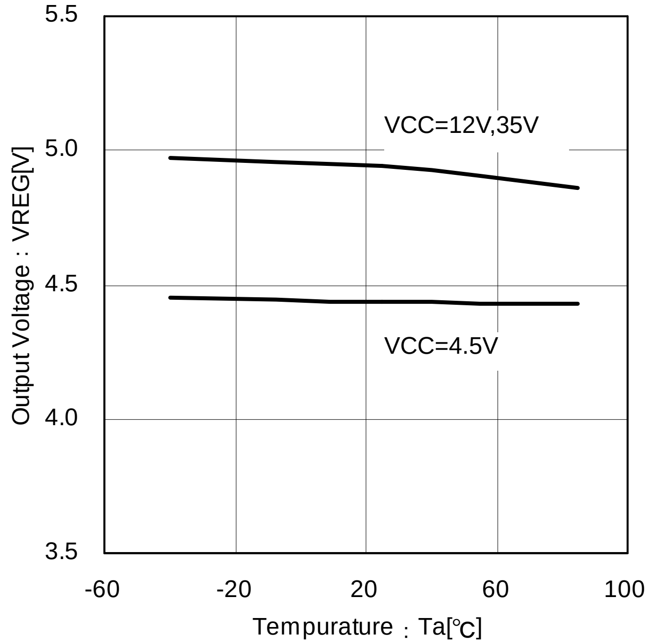


Fig.2 VREG temperature characteristic

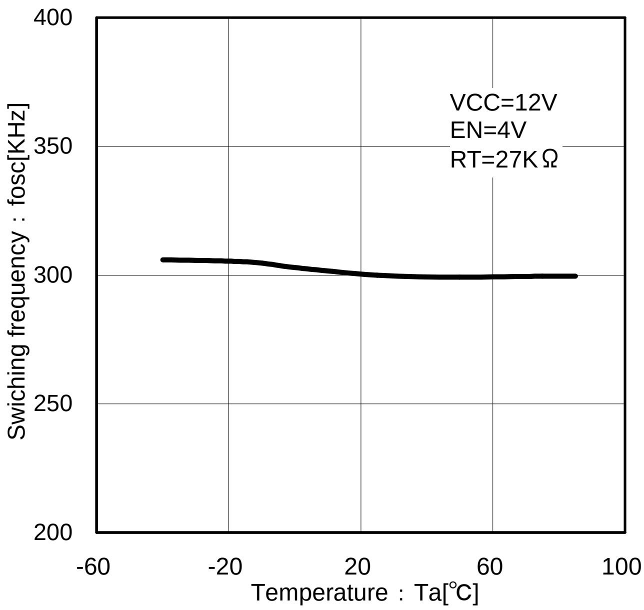


Fig.3 OSC temperature characteristic
(@300KHz)

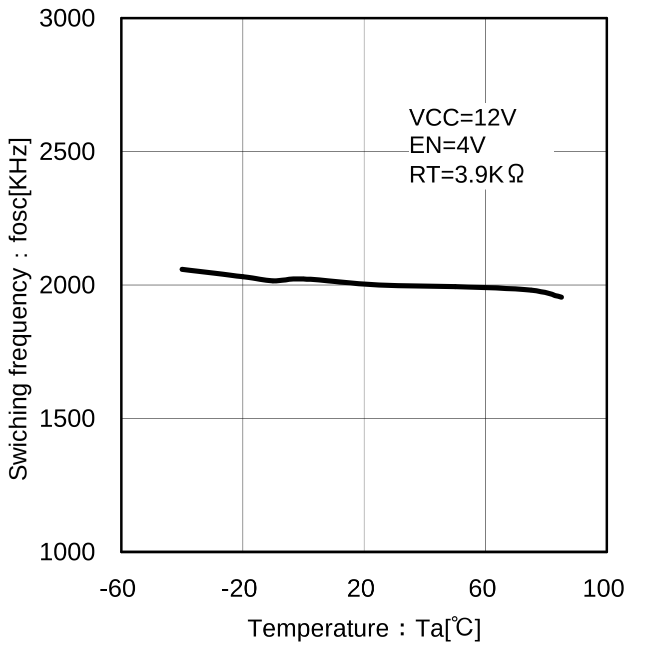


Fig.4 OSC temperature characteristic
(@2000KHz)

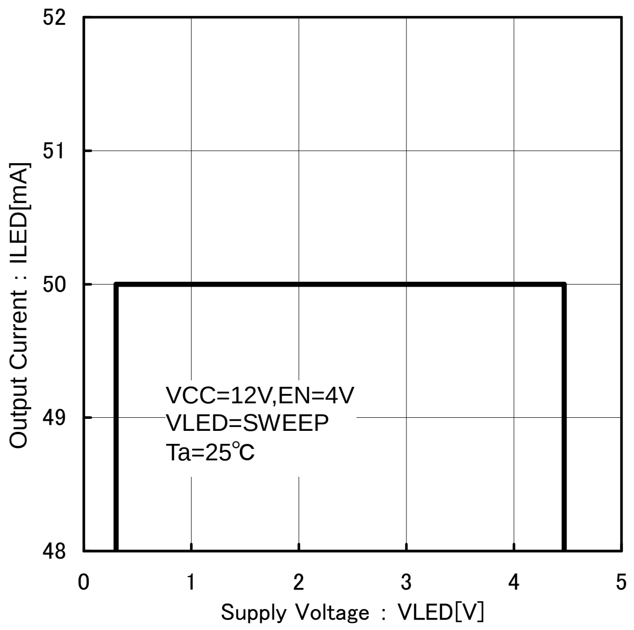


Fig.5 VLED vs ILED

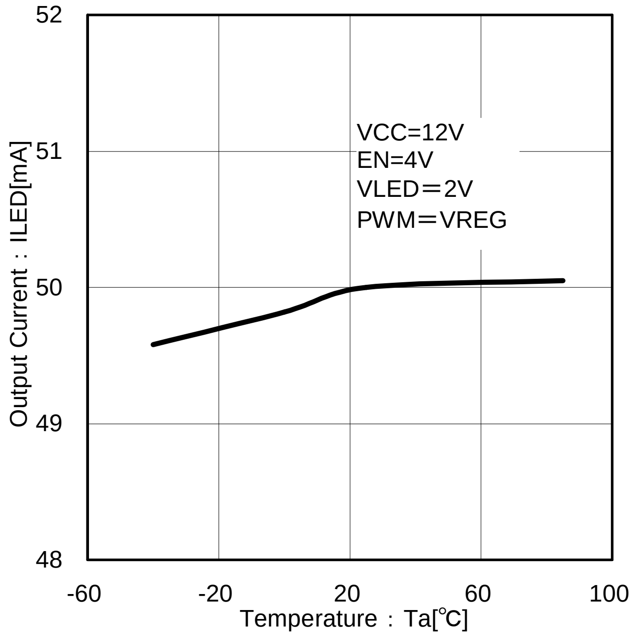


Fig.6 ILED temperature characteristic

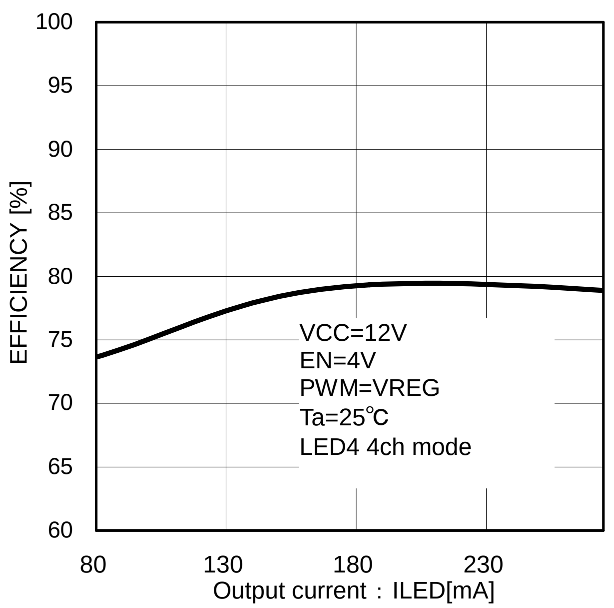


Fig.7 Efficiency (Back-boost application)

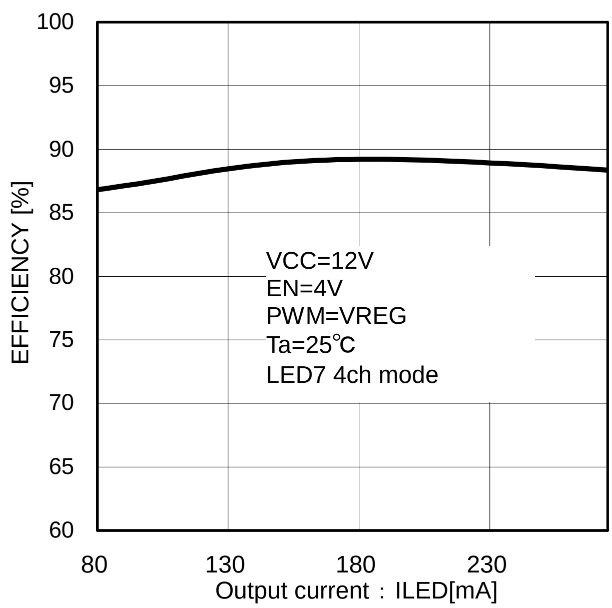


Fig.8 Efficiency (Boost application)

● Description of Blocks

1.voltage reference (VREG)

5V (Typ.) is generated from the VCC input voltage when the enable pin is set HI. This voltage is used to power internal circuitry, as well as the voltage source for device pins that need to be fixed to a logical HI.

UVLO protection is integrated into the VREG pin. The voltage regulation circuitry operates uninterrupted for VREG voltages VCC>4.0V(Typ.) and VREG>3.5V(Typ.), but if output voltage drops to VCC<3.5V(Typ.) or VREG<2.0V(Typ.) UVLO engages and turns the IC off.

Connect a capacitor (Creg = 2.2uF Typ.) to the VREG terminal for phase compensation. Operation may become unstable if Creg is not connected.

2. Constant-current LED drivers

Table1 LED voltage

LED EN		LED			
〈1〉	〈2〉	1	2	3	4
L	L	ON	ON	ON	ON
H	L	ON	ON	ON	OFF
L	H	ON	ON	OFF	OFF
H	H	ON	OFF	OFF	OFF

If less than four constant-current drivers are used, unused channels should be switched off via the LEDEN pin configuration. The truth table for these pins is shown above. If a driver output is enabled but not used (i.e. left open), the IC's open circuit-detection circuitry will operate. Please keep the unused pins open. The LEDEN terminals are pulled down internally in the IC, so if left open, the IC will recognize them as logic LOW. However, they should be connected directly to VREG or fixed to a logic HI when in use.

(1)**Output current setting**

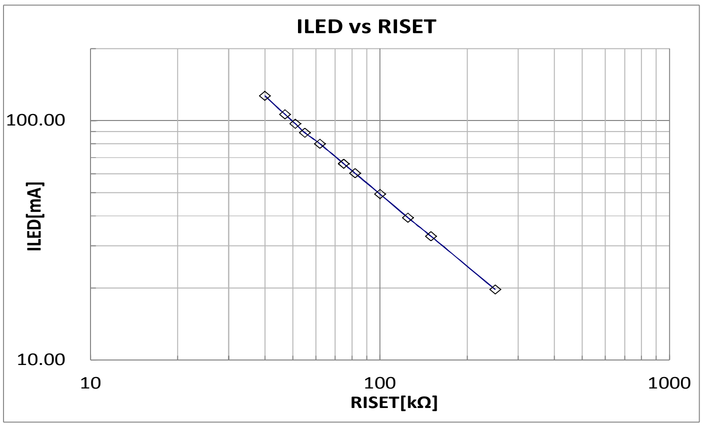


Fig.9 RISET vs ILED

LED current is computed via the following equation:

ILED= 1.0V / RISET x GAIN [A] :GAIN=5000(TYP.)

GAIN is a constant decided in the circuit .

(2)**PWM intensity control**

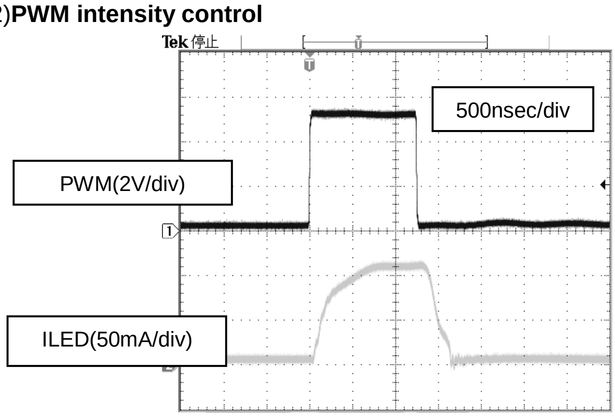


Fig.10 PWM=150Hz, Duty=0.02% ILED wave form

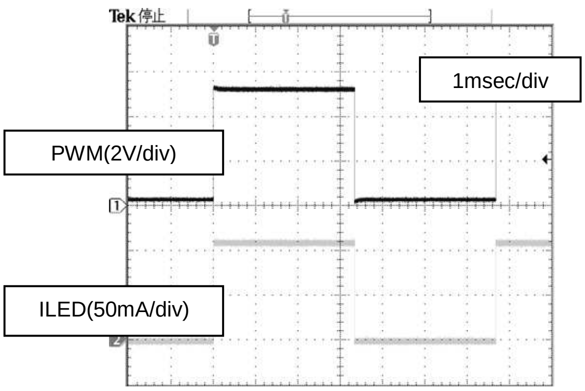


Fig.11 PWM=150Hz, Duty=50.0% ILED wave form

In PWM intensity control mode, the ON/OFF state of each current driver is controlled directly by the input signal on the PWM pin; thus, the duty ratio of the input signal on the PWM pin equals the duty ratio of the LED current. When not controlling intensity via PWM, fix the PWM terminal to a high voltage (100%). Output light intensity is greatest at 100% input.

3. **Buck-Boost DC/DC controller**

(1)Number of LEDs in series connection

Output voltage of the DCDC converter is controlled such that the forward voltage over each of the LEDs on the output is set to 1.0V (Typ.). DCDC operation is performed only when the LED output is operating. When two or more LED outputs are operating simultaneously, the LED voltage output is held at 1.0V (Typ.) per LED over the column of LEDs with the highest VF value. The voltages of other LED outputs are increased only in relation to the fluctuation of voltage over this column. Consideration should be given to the change in power dissipation due to variations in VF of the LEDs. Please determine the allowable maximum VF variance of the total LEDs in series by using the description as shown below:

VF variation allowable voltage 3.5V（Typ.） = short detecting voltage 4.5V（Typ.）－LED control voltage 1.0V（Typ.）

The number of LEDs that can be connected in series is limited due to the open-circuit protection circuit, which engages at 85% of the set OVP voltage. Therefore, the maximum output voltage of the under normal operation becomes

34 V (= **40** V x **0.85**, where (**34** V – **1.0** V) / **VF** > **N** [maximum number of LEDs in series]).

(2) **Over-voltage protection circuit (OVP)**

The output of the DCDC converter should be connected to the OVP pin via a voltage divider. In determining an appropriate trigger voltage of for OVP function, consider the total number of LEDs in series and the maximum variation in VF. Also, bear in mind that LED Open Detection is triggered at 0.85 x OVP trigger voltage.

If the OVP function engages, it will not release unless the DCDC voltage drops to 72.5% of the OVP trigger voltage. For example, if ROVP1 (GND side), ROVP2 (output voltage side), and DCDC voltage VOUT are conditions for OVP, then:

$$\mathbf{VOUT} \geq (\mathbf{ROVP1} + \mathbf{ROVP2}) / \mathbf{ROVP1} \times \mathbf{2.0}\ \text{V}.$$

OVP will engage when **VOUT** > **32** V if **ROVP1** = **22** kΩ and **ROVP2** = **330** kΩ.

(3) **Buck-boost DC/DC converter oscillation frequency (FOSC)**

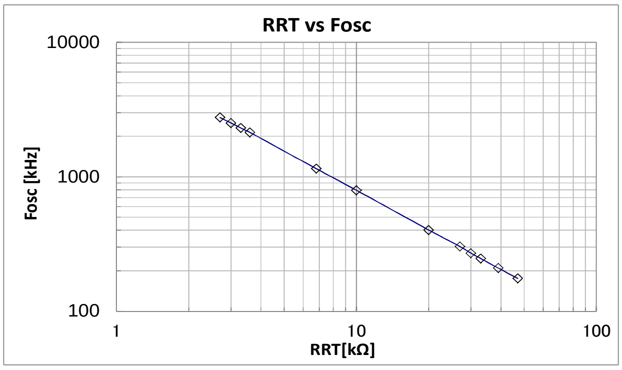


Fig.12 RRT VS FOSC

The regulator’s internal triangular wave oscillation frequency can be set via a resistor connected to the RT pin (pin 4). This resistor determines the charge/discharge current to the internal capacitor, thereby changing the oscillating frequency. Refer to the above graph and following expression when setting RT.

$$fosc = 81\times10^{8} / RRT[\Omega] \times \alpha\ [kHz]$$

81×10^{8} is constant value in IC (+-5%) and α is adjustment factor.

(RT :α = 43kΩ: 1.01, 27kΩ: 1.00 , 18kΩ: 0.99, 10 kΩ: 0.98, 4.7kΩ: 0.97, 3.9kΩ: 0.96)

A resistor in the range of 3 kΩ～33 kΩ is recommended. Settings that deviate from the frequency range shown below may cause switching to stop, and proper operation cannot be guaranteed.

(4) **External DC/DC converter oscillating frequency synchronization (FSYNC)**

Do not switch from external to internal oscillation of the DC/DC converter if an external synchronization signal is present on the SYNC pin. When the signal on the SYNC terminal is switched from high to low, a delay of about 30 µS (typ.) occurs before the internal oscillation circuitry starts to operate (only the rising edge of the input clock signal on the SYNC terminal is recognized). Moreover, if external input frequency is less than the internal oscillation frequency, the internal oscillator will engage after the above-mentioned 30 µS (typ.) delay; thus, do not input a synchronization signal with a frequency less than the internal oscillation frequency.

(5)**Soft Start Function**

The soft-start (SS) limits the current and slows the rise-time of the output voltage during the start-up, and hence leads to prevention of the overshoot of the output voltage and the inrush current.

4.**LED Short Detection**

Table2 Detecting condition and operation after detect about each protection

Protection	**Detecting Condition**		**Operation after detect**
	[Detect]	**[Release]**	
UVLO	VCC<3.5V or VREG<2.0V	VCC>4.0V and VREG>3.5V	All blocks shut down
TSD	Tj>175℃	Tj<150℃	All blocks (but except REG) shut down
OVP	VOVP>2.0V	VOVP<1.45V	SS discharged
OCP	VCS≦VCC-0.6V	VCS>VCC-0.6V	SS discharged
SCP	VLED<0.3V (100ms delay 300kHz)	EN or UVLO	Counter starts and then latches off all blocks (but except REG)
LED open	VLED<0.3V & VOVP>1.7V	EN or UVLO	The only detected channel latches off
LED short	VLED>4.5V (100ms delay 300kHz)	EN or UVLO	The only detected channel latches off (after the counter sets)

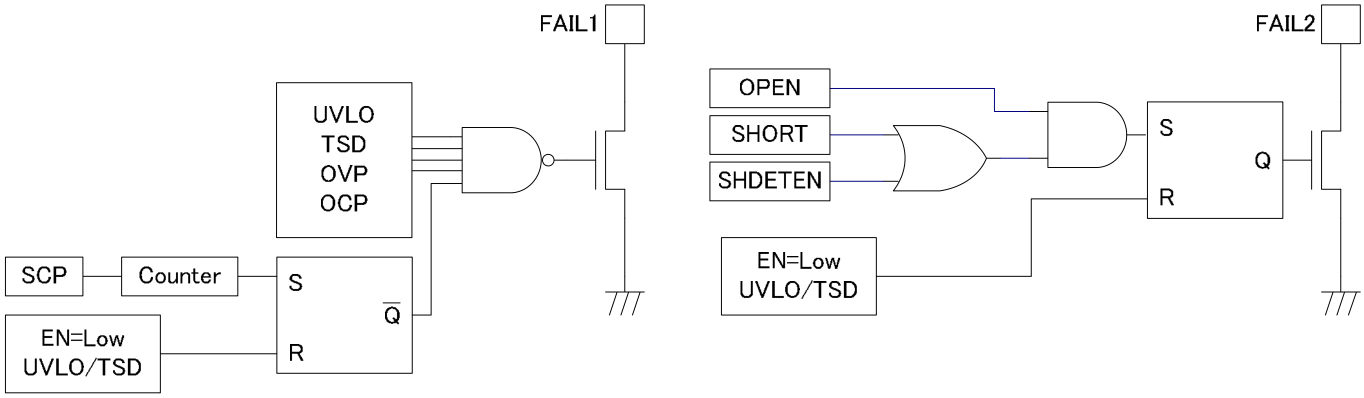


Fig.13 Protection flag output part block diagram

The operating status of the built-in protection circuitry is propagated to FAIL1 and FAIL2 pins (open-drain outputs). FAIL1 becomes low when UVLO, TSD, OVP, or SCP protection is engaged, whereas FAIL2 becomes low when open or short LED is detected.

●**Operation of the Protection Circuitry**

(1)Under-Voltage Lock Out (UVLO)

The UVLO shuts down all the circuits other than REG when VCC<3.5V(Typ.) or VREG<2.0V（Typ.）

(2)Thermal Shut Down (TSD)

The TSD shuts down all the circuits other than REG when the Tj reaches 175℃ (TYP), and releases when the Tj becomes below 150℃ (TYP).

(3)Over Current Protection (OCP)

The OCP detects the current through the power-FET by monitoring the voltage of the high-side resistor, and activates when the CS voltage becomes less than VCC-0.6V (TYP).

When the OCP is activated, the external capacitor of the SS pin becomes discharged and the switching operation of the DCDC turns off.

(4) Over Voltage Protection (OVP)

The output voltage of the DCDC is detected with the OVP-pin voltage, and the protection activates when the OVP-pin voltage becomes greater than 2.0V (TYP).

When the OVP is activated, the external capacitor of the SS pin becomes discharged and the switching operation of the DCDC turns off.

(5)Short Circuit Protection (SCP)

When the LED-pin voltage becomes less than 0.3V (TYP), the internal counter starts operating and latches off the circuit approximately after 100ms (when FOSC = 300kHz). If the LED-pin voltage becomes over 0.3V before 100ms, then the counter resets.

When the LED anode (i.e. DCDC output voltage) is shorted to ground, then the LED current becomes off and the LED-pin voltage becomes low. Furthermore, the LED current also becomes off when the LED cathode is shorted to ground. Hence in summary, the SCP works with both cases of the LED anode and the cathode being shorted.

(6)LED Open Detection

When the LED-pin voltage ≤ 0.3V (TYP) as well as OVP-pin voltage ≥ 1.7V (TYP) simultaneously, the device detects as LED open and latches off that particular channel.

(7)PWM OFF detection circuit

Built-in counter operation is begun after EN is turned on, PWM OFF detection circuit operates by about 100ms(FOSC:300KHz), and power consumption is reduced.

(8)Output voltage electrical discharge circuit (VDISC)

It is a function to prevent LED from flickering by the residual electric charge at PWM=L⇒H. The residual electric charge of the DC/DC output terminal can be discharged by connecting the terminal VDISC with the DC/DC output terminal.

(9)LED Short detection

The internal counter starts operating, and approximately after 100ms (when FOSC = 300kHz) the only detected channel (as LED short) latches off. With the PWM brightness control, the detecting operation is processed only when PWM-pin = High. If the condition of the detection operation is released before 100ms (when FOSC = 300kHz), then the internal counter resets.

※ The counter frequency is the DCDC switching frequency determined by the RT. The latch proceeds at the count of 32770.

If you don’t need Short Detection, please short SHDETEN terminal to VREG.

SHDETEN terminal setting is OPEN or GND, Short Detection is available.

●Timing Chart

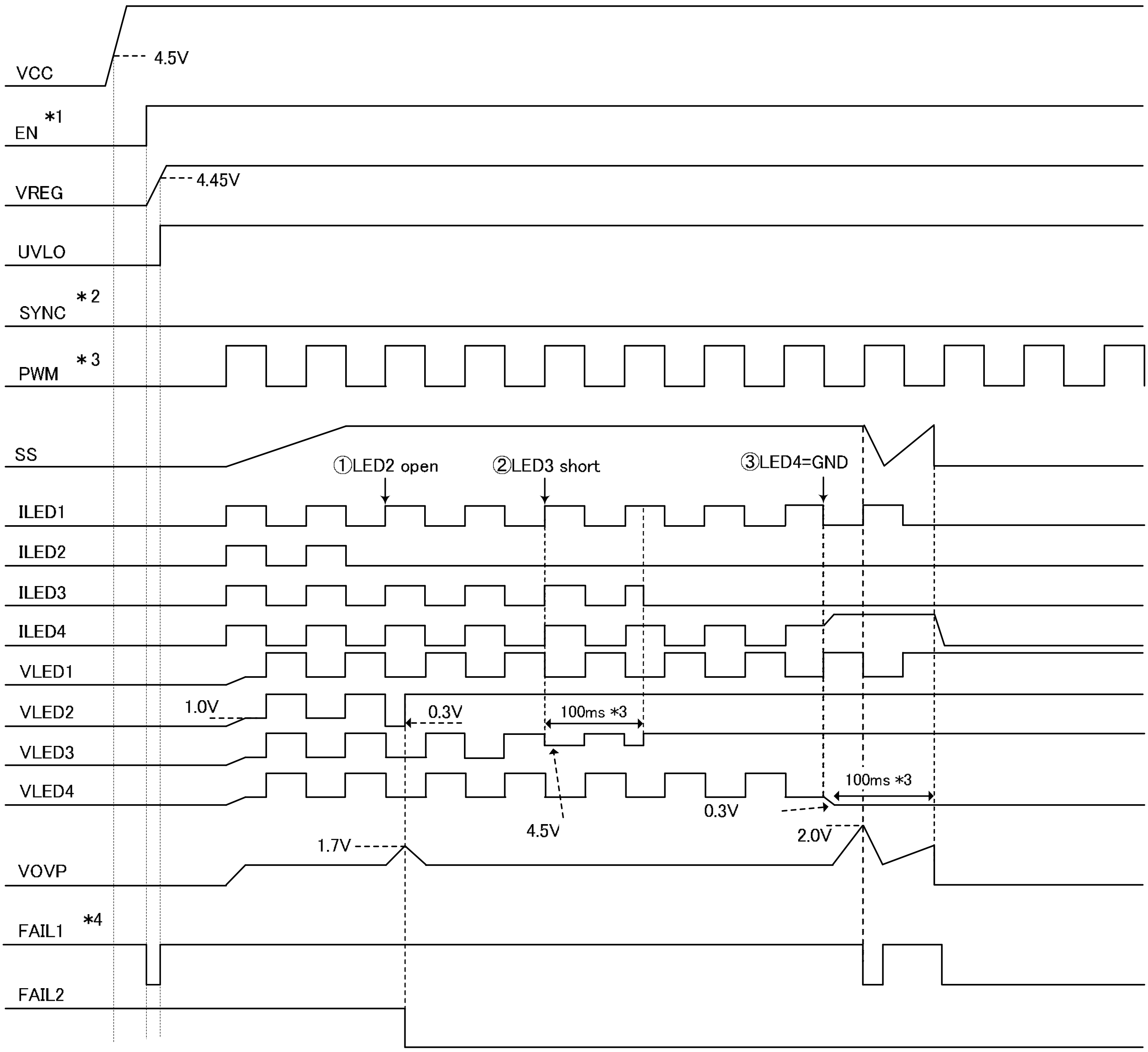


Fig.14 Protection Sequence timing Chart

＊1 Turn on the EN after the VCC is on
Turn on the PWM and SYNC after VREG≧4.45V.

＊2 The order of turning on PWM and SYNC is arbitrary.

＊3 Aprox 100ms of delay when Fosc = 300kHz

＊4 It is the timing chart that Fail is pull-up in an external voltage.

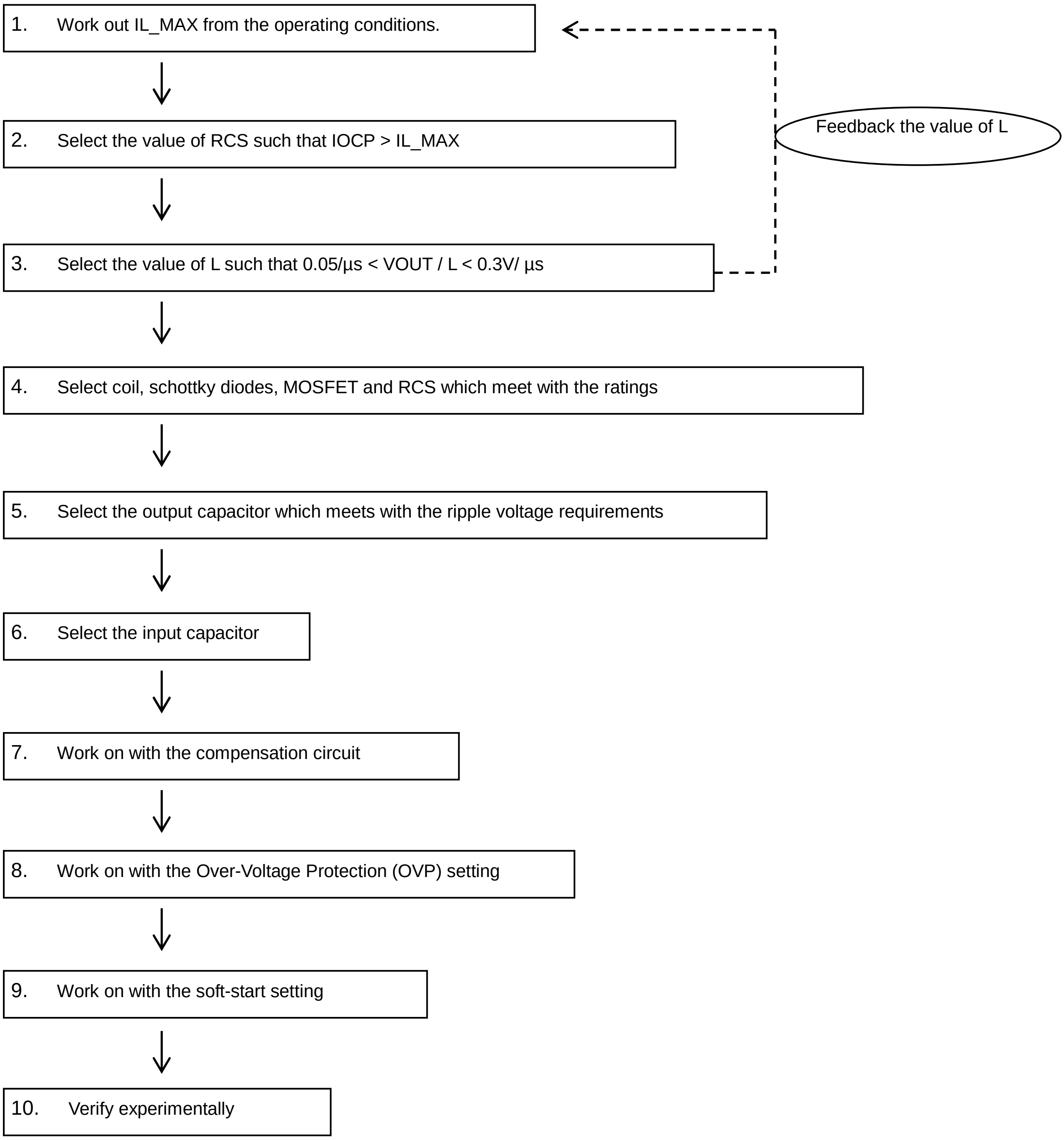
① LED2 is open mode.
VLED2<0.3V VOVP and > detects 1.7V, and LED2 is turned off.
→FAIL2 becomes Low.

② LED3 is short mode.
VLED3>4.5V is detected, and LED3 after about 100ms is turned off.

③ VLED4 is GND- shorted.
③-1 The output voltage lifts, and OVP is detected with VOVP>2.0V.
→SS pulling out
→FAIL1 becomes Low.
③-2 Shutdown after about 100ms when LED4<0.3V is detected.

●Procedure for external components selection

Follow the steps as shown below for selecting the external components



1. Computation of the Input Peak Current and IL_MAX

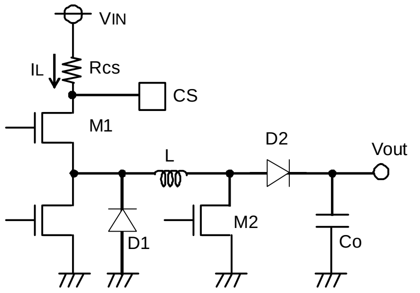


Fig.15 Output application circuit diagram

① Calculation of the maximum output voltage (Vout_max)

To calculate the Vout_max, it is necessary to take into account of the VF variation and the number of LED connection in series.

$Vout\_max = (VF + \Delta VF) \times N + 1.1V$

ΔVF : VF Variation
N : Number of LED connection in series

② Calculation of the max output current Iout_max

$Iout\_max = ILED \times 1.03 \times M$

M: Number of LED connection in parallel

③Calculation of the max input peak current IL_MAX

$IL\_MAX = IL\_AVG + 1/2 \Delta IL$

$IL\_AVG = (VIN + Vout\_max) \times Iout\_max / (n \times VIN)$

n: efficiency Fosc: switching frequency

$$\Delta IL = \frac{VIN}{L} \times \frac{1}{Fosc} \times \frac{Vout}{VIN+Vout}$$

・The worst case scenario for VIN is when it is at the minimum, and thus the minimum value should be applied in the equation.

・The L value of 2.2µH ~ 47µH is recommended. The current-mode type of DC/DC conversion is adopted for BD81A04EFV-M, which is optimized with the use of the recommended L value in the design stage. This recommendation is based upon the efficiency as well as the stability. The L values outside this recommended range may cause irregular switching waveform and hence deteriorate stable operation.

・n (efficiency) is approximately 80%

2. The setting of over-current protection

Choose Rcs with the use of the equation

(VIN - Vocp_min (=0.54V)) / Rcs > IL_MAX

3. The selection of the L

In order to achieve stable operation of the current-mode DC/DC converter, we recommend selecting the L value in the range indicated below:

$$0.05\ [V/\mu S] < \frac{Vout \times Rcs}{L} < 0.3\ [V/\mu S]$$

When investigating the margin, it is worth noting that the L value may vary by approximately ±30%.

The smaller $\frac{Vout \times Rcs}{L}$ allows stability improvement but slows down the response time.

4. Selection of coil L, diode D1 and D2, MOSFET M1 and M2, and Rcs

	Current rating	Voltage rating	Heat loss
Coil L	> IL_MAX	—	
Diode D1	> Iocp	> VIN_MAX	
Diode D2	> Iocp	> Vout	
MOSFET M1	> Iocp	> VIN_MAX	
MOSFET M2	> Iocp	> Vout	
Rcs	—	—	$> Iocp^2 \times Rcs$

※ Allow some margin, such as the tolerance of the external components, when selecting.

※ In order to achieve fast switching, choose the MOSFETs with the smaller gate-capacitance.

5. Selection of the output capacitor

Select the output capacitor Cout based on the requirement of the ripple voltage Vpp.

$$Vpp = \frac{Iout}{Cout} \times \frac{Vout}{Vout+V_{IN}} \times \frac{1}{Fosc} + \Delta IL \times R_{ESR}$$

Choose Cout that allows the Vpp to settle within the requirement. Allow some margin also, such as the tolerance of the external components.

6. Selection of the input capacitor

A capacitor at the input is also required as the peak current flows between the input and the output in DC/DC conversion. We recommend an input capacitor greater than 10µF with the ESR smaller than 100mΩ. The input capacitor outside of our recommendation may cause large ripple voltage at the input and hence lead to malfunction.

7. Phase Compensation Guidelines

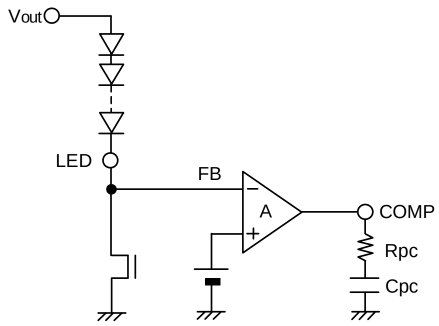


Fig.16 COMP part application circuit diagram

In general, the negative feedback loop is stable when the following condition is met

・Overall gain of 1 (0dB) with a phase lag of less than 150º (i.e., a phase margin of 30º or more)

However, as the DC/DC converter constantly samples the switching frequency, the gain-bandwidth (GBW) product of the entire series should be set to 1/10 the switching frequency of the system. Therefore, the overall stability characteristics of the application are as follows:

- Overall gain of 1 (0dB) with a phase lag of less than 150º (i.e., a phase margin of 30º or more)
- GBW (frequency at gain 0dB) of 1/10 the switching frequency

Thus, to improve response within the GBW product limits, the switching frequency must be increased.

※ R_L is the load impedance. (R_L = VOUT / IOUT)

The key for achieving stability is to place fz near to the GBW.

Phase-lead $fz = \frac{1}{2\pi CpcRpc}$ [Hz]

Phase-lag $fp1 = \frac{1}{2\pi R_L Cout}$ [Hz]

Good stability would be obtained when the fz is set between 1kHz～10kHz.

In buck-boost applications, Right-Hand-Plane (RHP) Zero exists. This Zero has no gain but a pole characteristic in terms of phase. As this Zero would cause instability when it is in the control loop, so it is necessary to bring this zero before the GBW.

$$fRHP = \frac{Vout \times \{VIN/(Vout+VIN)\}^2}{2\pi I_{LOAD} L} \text{ [Hz]}$$

I_{LOAD}: MAXIMUM LOAD CURRENT

It is important to keep in mind that these are very loose guidelines, and adjustments may have to be made to ensure stability in the actual circuitry. It is also important to note that stability characteristics can change greatly depending on factors such as substrate layout and load conditions. Therefore, when designing for mass-production, stability should be thoroughly investigated and confirmed in the actual physical design.

8. Setting of the over-voltage protection

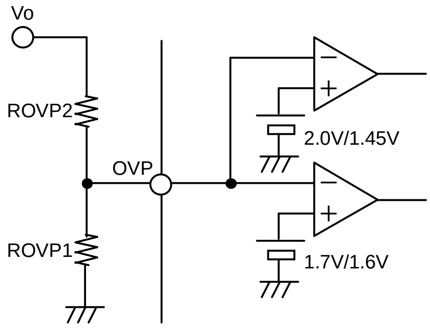


Fig.17 OVP part application circuit diagram

* We recommend setting the over-voltage protection Vovp 1.2V to 1.5V greater than Vout which is adjusted by the number of LEDs in series connection. Less than 1.2V may cause unexpected detection of the LED open and short during the PWM brightness control. For the Vovp greater than 1.5V, the LED short detection may become invalid.

9. Setting of the soft-start

The soft-start allows minimization of the coil current as well as the overshoot of the output voltage at the start-up.

For the capacitance we recommend in the range of 0.001 to 0.1uF. For the capacitance less than 0.001uF may cause overshoot of the output voltage. For the capacitance greater than 0.1uF may cause massive reverse current through the parasitic elements of the IC and damage the whole device. In case it is necessary to use the capacitance greater than 0.1uF, ensure to have a reverse current protection diode at the VCC or a bypass diode placed between the SS-pin and the VCC.

Soft-start time TSS [TYP.]

TSS = CSSX0.7V / 5uA [s]　　　CSS: The capacitance at the SS-pin

There is the possibility of SCP error detection hang on CSS setting and Oscillating frequency setting.
Please check the following condition.

Trise = CSS X V1 / Iss
　　Trise : DCDC start up time, V1 : IC constant voltage(MAX 2.5V), Iss : SS source current(MIN 3.0uA)
Tscp = 32770 X (1/Fosc)
　　Tscp : SCP Latch OFF Delay Time, Fosc : Oscillating frequency
SCP error detection avoid condition : Trise < Tscp

10. Verification of the operation by taking measurements
The overall characteristic may change by load current, input voltage, output voltage, inductance, load capacitance, switching frequency, and the PCB layout. We strongly recommend verifying your design by taking the actual measurements.

●**Recommended operating range**

The following data is recommended operating range of BD81A04EFV-M (VCC vs Vout).
The following data is reference data in Rohm evaluation board. So please check the behavior of practice board and use this IC.

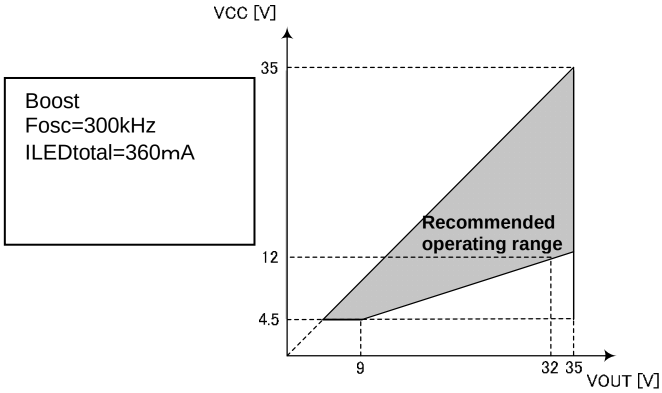


Fig.18 Boost operating range (1)

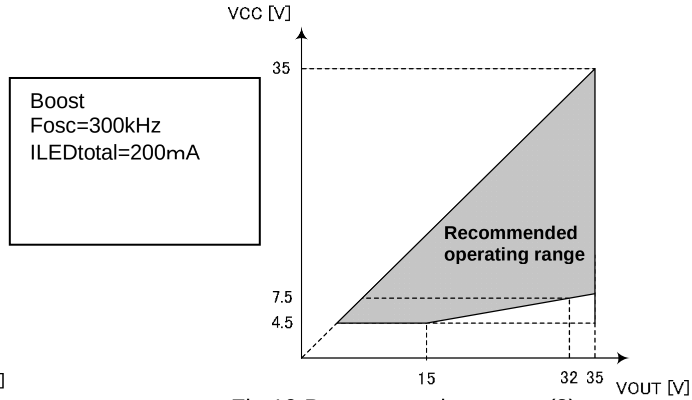


Fig.19 Boost operating range (2)

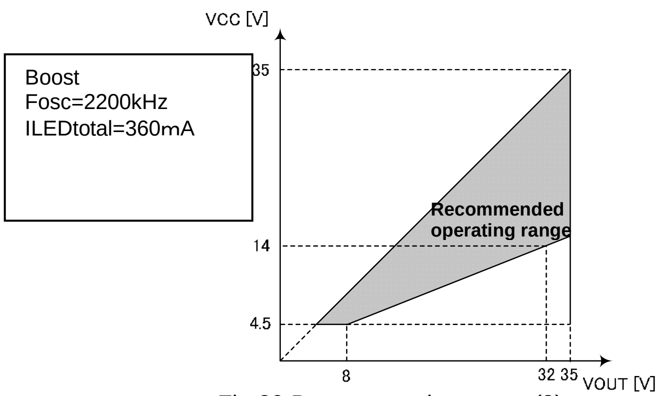


Fig.20 Boost operating range (3)

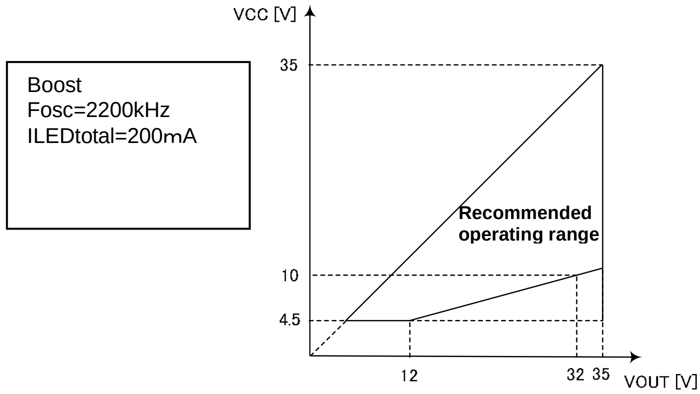


Fig.21 Boost operating range (4)

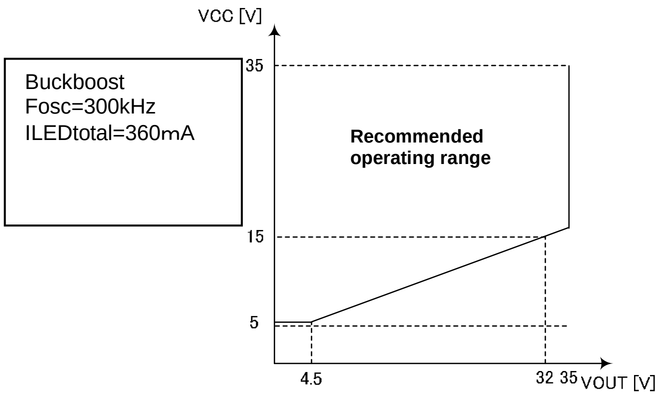


Fig.22 Buck-boost operating range (1)

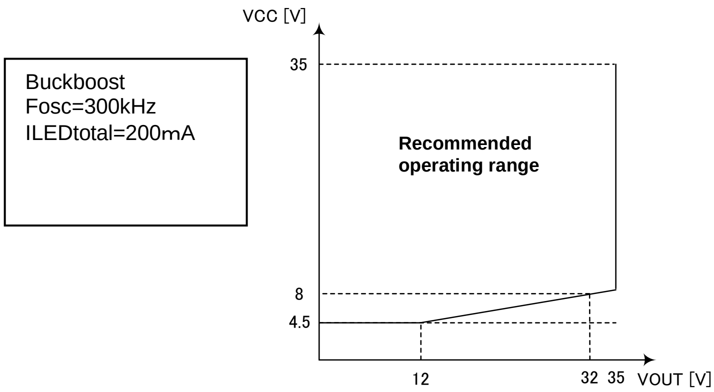


Fig.23 Buck-boost operating range (2)

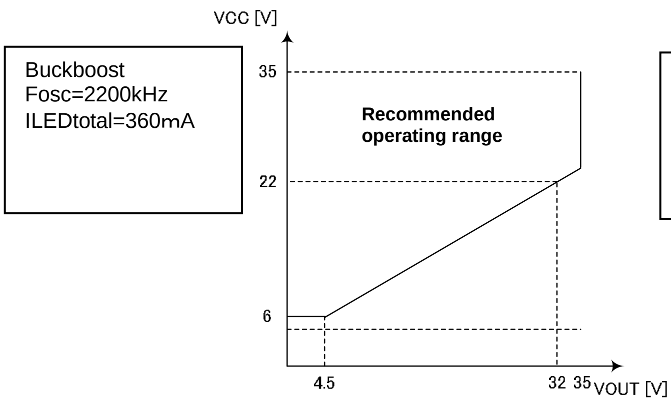


Fig.24 Buck-boost operating range (3)

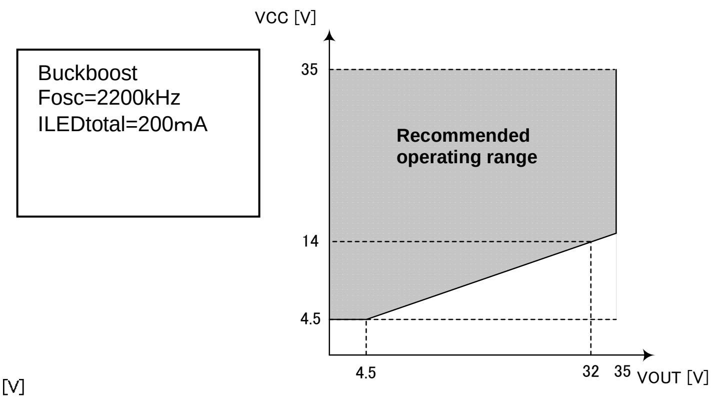


Fig.25 Buck-boost operating range (4)

● **PCB application circuit diagram**

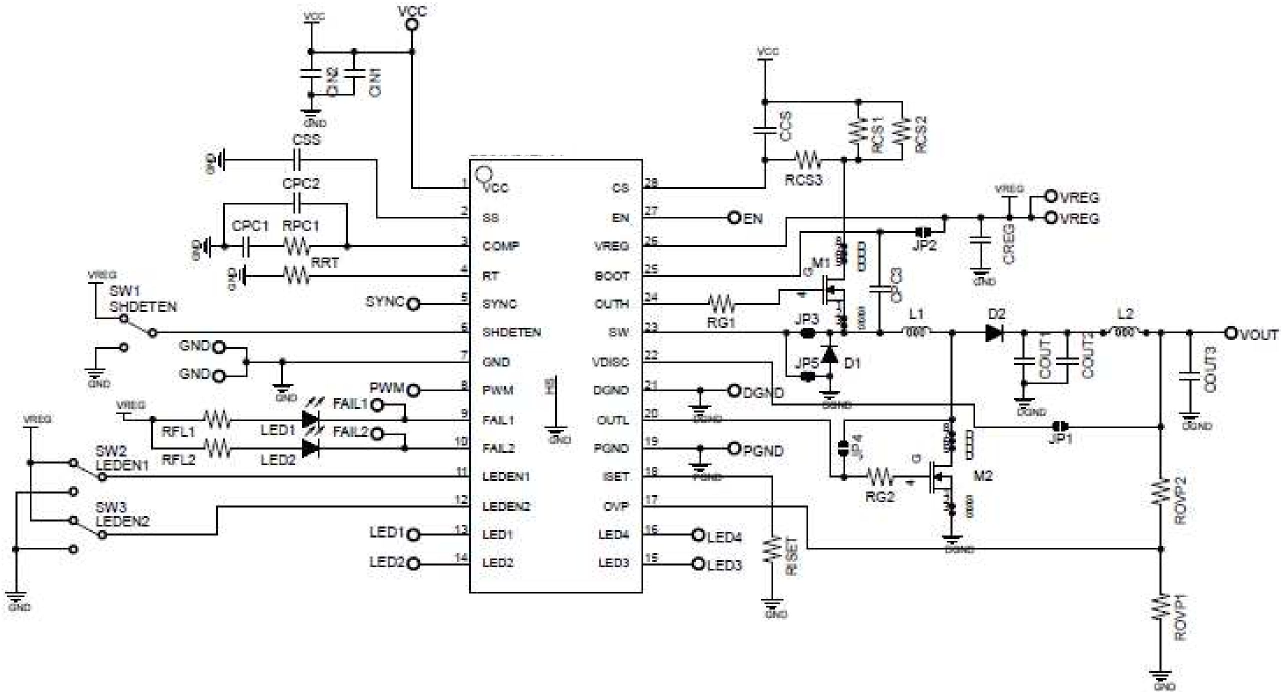


Fig.26 PCB application circuit diagram

- The coupling capacitors CVCC and CREG should be mounted as close as possible to the IC's pins.
- Large currents may pass through DGND and PGND, so each should have its own low-impedance routing to the system ground.
- Noise should be minimized as much as possible on pins PWM, ISET, RT and COMP.
- PWM,OUTH,SW,SYNC and LED1-4 carry switching signals, so ensure during layout that surrounding traces are not affected by crosstalk.

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● Application Board Daigram

When using it as Boost DCDC converter

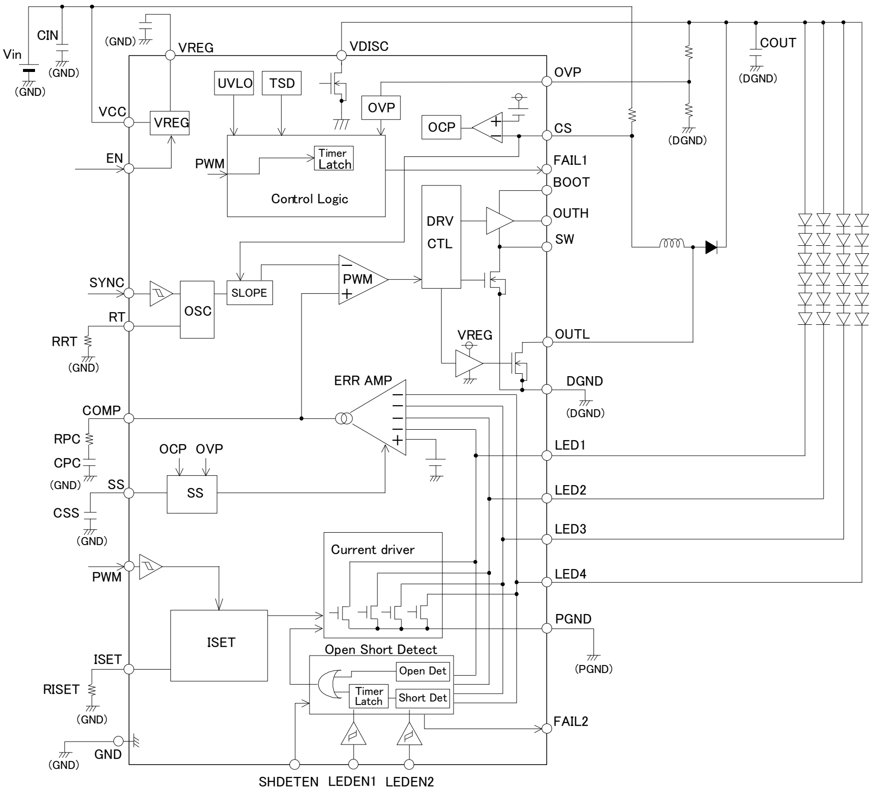


Fig.27 Boost application circuit diagram

When using it as Buck DCDC converter

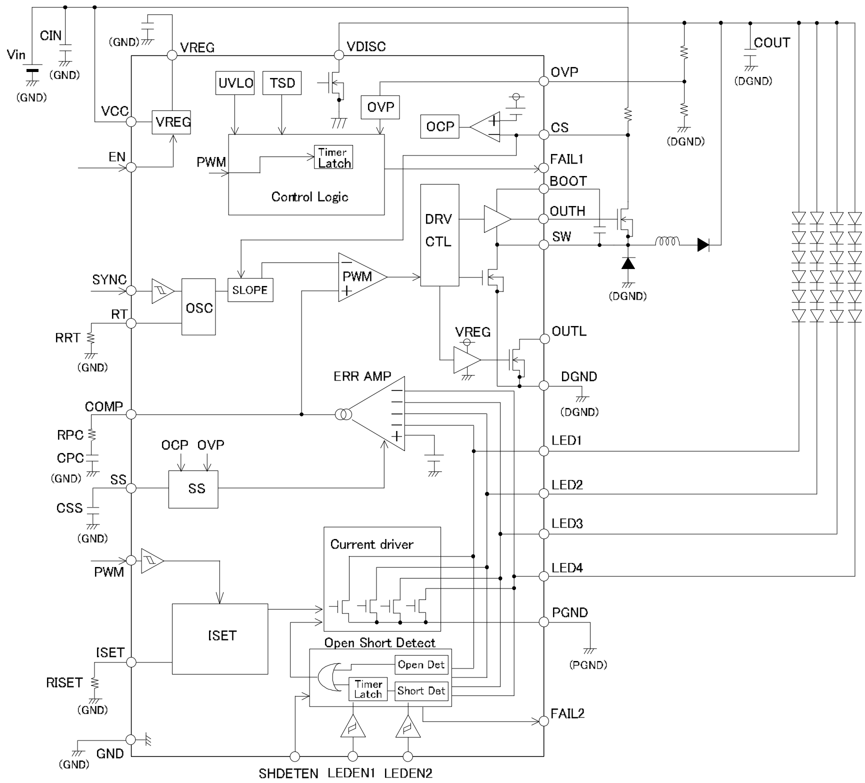


Fig.28 Buck application circuit diagram

Note：When VOUT and the LED terminal are shorted to GND, the overcurrent from VIN cannot be obstructed when using it as stated above as the Step-up DCDC converter. Therefore, please do measures of the insertion of the fuse between VCC and RCS etc.

●PCB board external part list

serial No.	component name	component value	product name	Manufacturer
1	CIN1	10µF	GRM31CB31E106KA75B	murata
2	CIN2	－	－	－
3	CPC1	0.1µF	GRM188B31H104KA92	murata
4	CPC2	－	－	－
5	RPC1	510Ω	MCR03 Series	Rohm
6	CSS	0.1µF	GRM188B31H104KA92	murata
7	RRT	27kΩ	MCR03 Series	Rohm
8	RFL1	100kΩ	MCR03 Series	Rohm
9	RFL2	100kΩ	MCR03 Series	Rohm
10	CCS	－	－	－
11	RCS1	620mΩ	MCR100JZHFLR620	Rohm
12	RCS2	620mΩ	MCR100JZHFLR620	Rohm
13	RCS3	0Ω	－	－
14	CREG	2.2µF	GRM188B31A225KE33	murata
15	CPC3	0.1µF	GRM188B31H104KA92	murata
16	M1	－	RSH070N05	Rohm
17	M2	－	－	－
18	D1	－	RB050L-40	Rohm
19	D2	－	RF201L2S	Rohm
20	L1	33µH	SLF10145T-330M1R6-H	TDK
21	L2	-	－	－
22	COUT1	10µF	GRM31CB31E106KA75B	murata
23	COUT2	10µF	GRM31CB31E106KA75B	murata
24	COUT3	-	－	－
25	ROVP1	30kΩ	MCR03 Series	Rohm
26	ROVP2	360kΩ	MCR03 Series	Rohm
27	RISET	100kΩ	MCR03 Series	Rohm
28	RG1	0Ω	－	－
29	RG2	－	－	－
30	LED1	0Ω	－	Rohm
31	LED2	0Ω	－	Rohm
32	JP1	0Ω	－	－
33	JP2	0Ω	－	－
34	JP3	－	－	－
35	JP4	0Ω	－	－
36	JP5	0Ω	－	－
37	JP6	－	－	－

● Power Dissipation Calculation

Pc	=	$I_{cc} \times VCC$	･･･①Power of circuit
	＋	$Ciss1 \times VREG \times Fsw \times VREG$	･･･②Boost FET (internal) drive power
	＋	$Ciss2 \times VREG \times Fsw \times VREG$	･･･③Buck FET (external) drive power
	＋	$\{ VLED \times M + \Delta Vf \times (M-1) \} \times ILED$	･･･④Power of current driver
	＋	$RonFET \times IFET \times IFET$	･･･⑤Internal FET power

IL_AVG =	$(VCC+Vout)/VCC \times Iout/n$	･･･⑥Inductance average current
IFET=	$IL\_AVG \times Vout/(VCC+Vout)$	･･･⑦Current that flows to Boost FET (internal)
Iout =	$ILED \times 1.03 \times M$	･･･⑧LED output current
Vout =	$(Vf + \Delta Vf) \times N + VLED$	･･･⑨DCDC output voltage

Pc : IC power consumption	Icc : Current of the maximum circuit	VCC : Power-supply voltage
Ciss1 : Boost FET gate capacitance	Ciss2 : Buck FET gate capacitance	VREG : VREG voltage
Fsw : Switching frequency	VLED : LED control voltage	ILED : LED output current
N : LED number	M : Parallel number of LED	Vf : LED forward voltage
ΔVf : LED Vf difference	RonFET : Step-up FET (internal) ON resistance	n : Efficiency

＜Calculation example＞

When assuming Icc=10mA, VCC=12V, Ciss1=65pF, Ciss2=2000pF, VREG=5V, Fsw=2200kHz, VLED=1V, ILED=50mA, N=7steps, M=4 row, Vf=3.5V, ΔVf=0.5V, RonFET=1.15Ω, n=80%

Vout =	$(3.5V+0.5V) \times 7\ \text{steps} + 1V = 29V$
Iout =	$50mA \times 1.03 \times 4\ \text{row} = 0.206A$
IL_AVG=	$(12+29V)/12V \times 0.206A/0.8 = 0.88A$
IFET=	$0.88A \times 29V/(12V+29V) = 0.622A$
Pc (4) =	$10mA \times 12V + 65pF \times 5V \times 2200kHz \times 5V + 2000pF \times 5V \times 2200kHz \times 5V +$
	$\{1.0V \times 4 + 0.5V \times (4-1)\} \times 50mA + 1.15\Omega \times 0.622A \times 0.622A = 0.898[W]$

● Power Dissipation of packaging

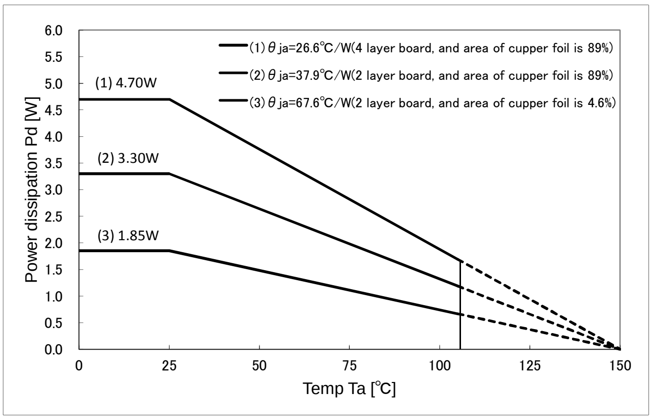


Fig.29 HTSSOP-B28 Power dissipation

Note 1: Power dissipation calculated when mounted on 70mm X 70mm X 1.6mm glass epoxy substrate (1-layer platform/copper thickness 18µm)

Note 2: Power dissipation changes with the copper foil density of the board. This value represents only observed values, not guaranteed values.

HTSSOP-B28

Pd=1.85W (0.97W): Board copper foil area 225m㎡

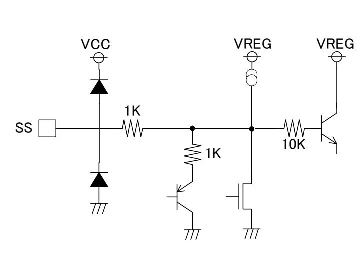
Pd=3.30W (1.72W): Board copper foil area 4900m㎡

Pd=4.70W (2.44W): Board copper foil area 4900m㎡

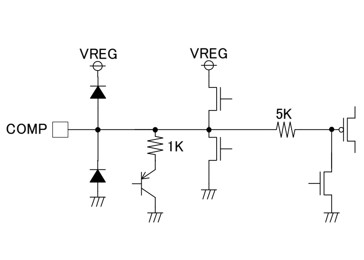
(Value within parentheses represents power dissipation when Ta=85℃)

● **Input/output Equivalent Circuits** (terminal name follows pin number)

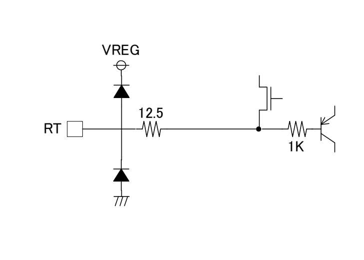
2.SS



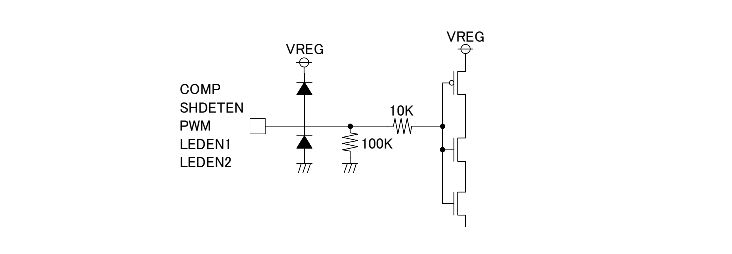
3.COMP



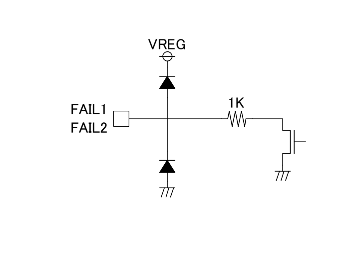
4.RT



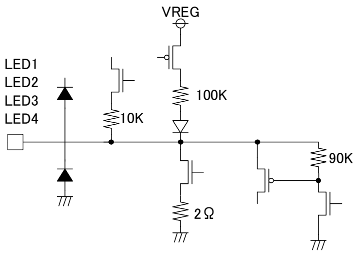
5.SYNC,6.SHDETEN,8.PWM,11.LEDEN1,12.LEDEN2



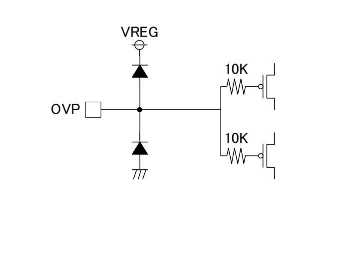
9.FAIL1,10.FAIL2



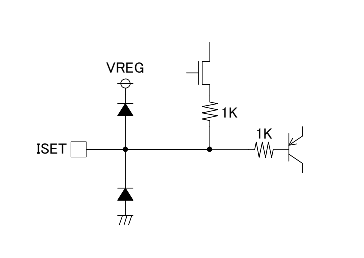
13～16. LED1～4



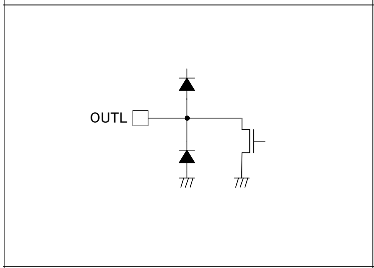
17.OVP



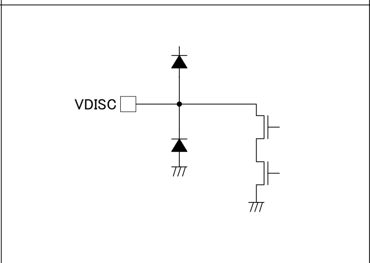
18.ISET



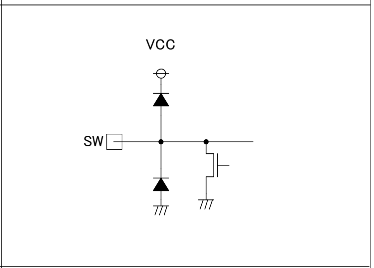
20.OUTL



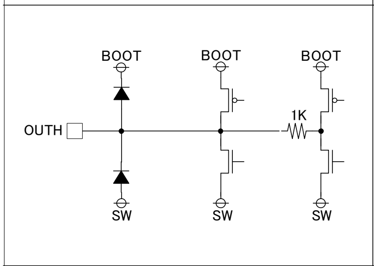
22.VDISC



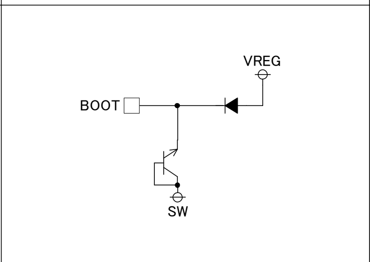
23.SW



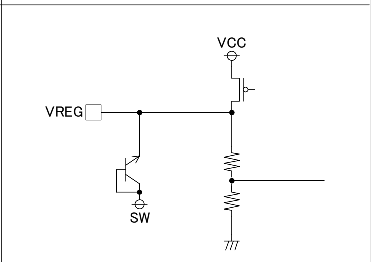
24.OUTH



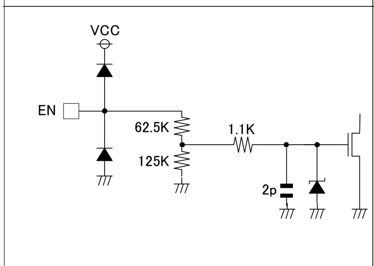
25.BOOT



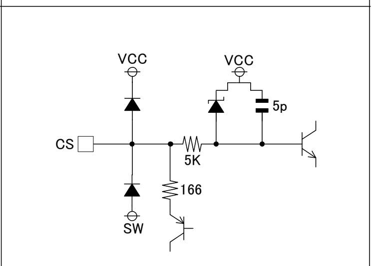
26.VREG



27.EN



28.CS



※All values typical.

● **Operating Notes**

1) Absolute maximum ratings

Use of the IC in excess of absolute maximum ratings (such as the input voltage or operating temperature range) may result in damage to the IC. Assumptions should not be made regarding the state of the IC (e.g., short mode or open mode) when such damage is suffered. If operational values are expected to exceed the maximum ratings for the device, consider adding protective circuitry (such as fuses) to eliminate the risk of damaging the IC.

2) GND potential

Ensure that the GND pin is held at the minimum potential in all operating conditions.

3) Thermal Design

Use a thermal design that allows for a sufficient margin for power dissipation (Pd) under actual operating conditions.

4) Inter-pin shorts and mounting errors

Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Shorts between output pins or between output pins and the power supply and GND pins caused by poor soldering or foreign objects may result in damage to the IC.

5) Operation in strong electromagnetic fields

Exercise caution when using the IC in the presence of strong electromagnetic fields as doing so may cause the IC to malfunction.

6) Testing on application boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from a jig or fixture during the evaluation process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

7) Ground wiring patterns

When using both small-signal and large-current GND traces, the two ground traces should be routed separately but connected to a single ground potential within the application in order to avoid variations in the small-signal ground caused by large currents. Also ensure that the GND traces of external components do not cause variations on GND voltage.

8) IC input pins and parasitic elements

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. PN junctions are formed at the intersection of these P layers with the N layers of other elements, creating parasitic diodes and/or transistors. For example (refer to the figure below):

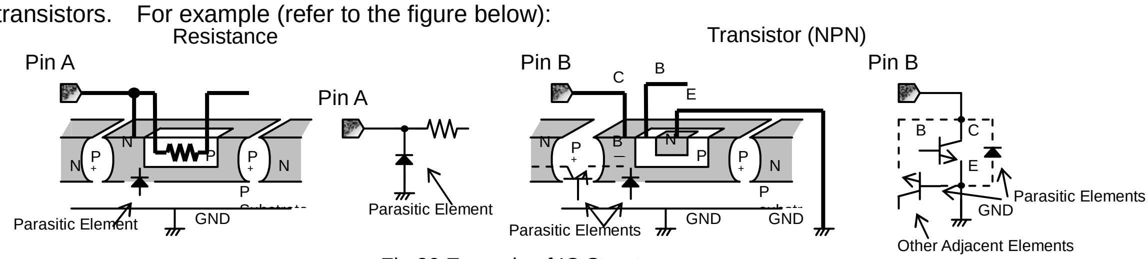


Fig.30 Example of IC Structure

- When GND > Pin A and GND > Pin B, the PN junction operates as a parasitic diode
- When GND > Pin B, the PN junction operates as a parasitic transistor

Parasitic diodes occur inevitably in the structure of the IC, and the operation of these parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

9) Over-current protection circuits

An over-current protection circuit (designed according to the output current) is integrated into the IC to prevent damage in the event of load shorting. This protection circuit is effective in preventing damage due to sudden and unexpected overloads on the output. However, the IC should not be used in applications where operation of the OCP function is anticipated or assumed

10) Thermal shutdown circuit (TSD)

This IC also incorporates a built-in TSD circuit for the protection from thermal destruction. The IC should be used within the specified power dissipation range. However, in the event that the IC continues to be operated in excess of its power dissipation limits, the rise in the chip's junction temperature T_j will trigger the TSD circuit, shutting off all output power elements. The circuit automatically resets itself once the junction temperature T_j drops down to normal operating temperatures. The TSD protection will only engage when the IC's absolute maximum ratings have been exceeded; therefore, application designs should never attempt to purposely make use of the TSD function.

The Japanese version of this document is the formal specification.
A customer may use this translation version only for a reference to help reading the formal version.
If there are any differences in translation version of this document, formal version takes priority.

●Ordering Information

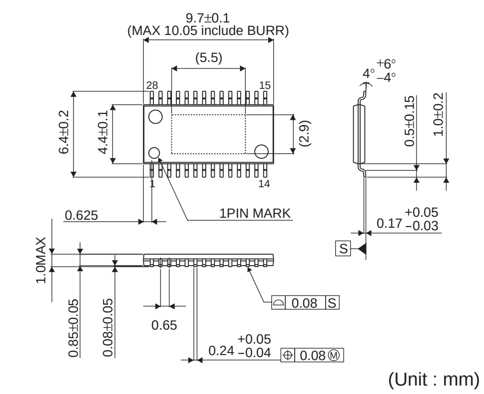
B	D	8	1	A	0	4	E	F	V	-	ME2

Package
EFV: HTSSOP-B28

Packaging
M: high reliability
E2: Embossed carrier tape
(HTSSOP-B28)

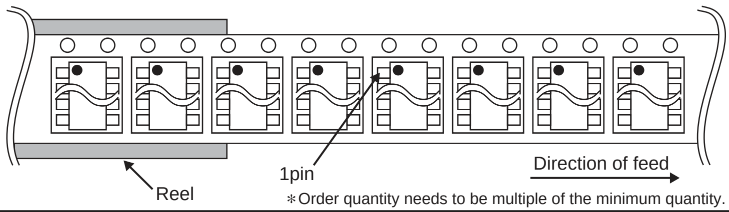
●Physical Dimension Tape and Reel Information

HTSSOP-B28



<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



＊Order quantity needs to be multiple of the minimum quantity.

●Marking Diagram