

TS3A5017-Q1 2-Channel, 4:1, Analog Switch for Automotive Applications

1 Features

- AEC-Q100 Qualified for Automotive Applications
 - Device Temperature: -40°C to 125°C , T_A
 - Device HBM Classification Level: $\pm 1500\text{-V}$
 - Device CDM Classification Level: $\pm 1000\text{-V}$
- Supports Powered-off Protection, I/O Pins Hi-Z When $V_{CC} = 0\text{V}$
- Low ON-State Resistance
- Low Charge Injection
- $1\ \Omega$ ON-State Resistance Matching
- 0.25% Total Harmonic Distortion (THD+N)
- 2.3-V to 3.6-V Single-Supply Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

2 Applications

- Sample-and-Hold Circuits
- Infotainment Audio and Video Signal Routing
- Telematics Control Unit

3 Description

The TS3A5017-Q1 device is a 2-channel 4:1 multiplexer that is designed to operate from 2.3 V to 3.6 V. This device is bidirectional and can handle both digital and analog signals. The powered-off protection feature of this device ensures the signal path is high impedance when $V_{CC} = 0\text{ V}$ which simplifies power sequencing and improves system reliability.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TS3A5017-Q1	VQFN (16)	4.00 mm × 3.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram

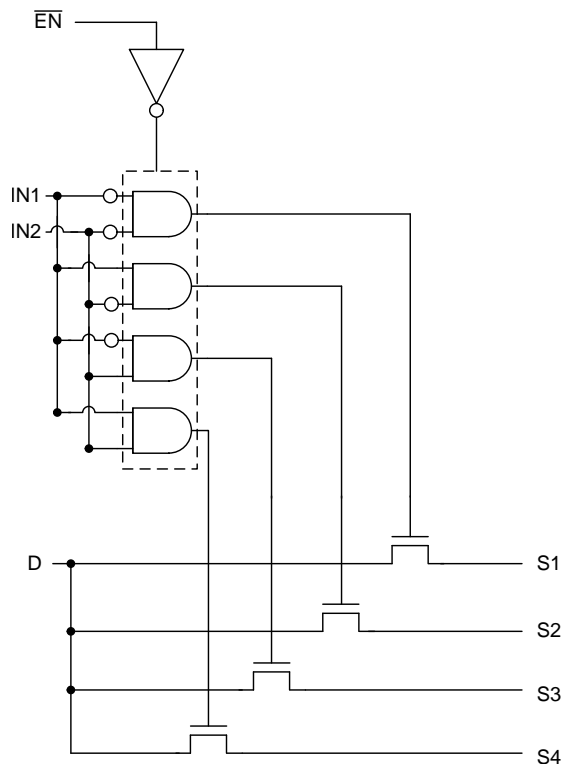


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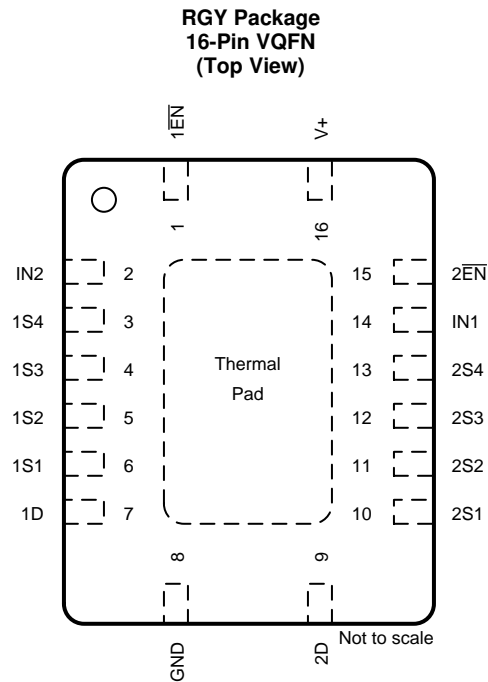
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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
October 2018	*	Initial release

5 Pin Configuration and Functions



If exposed thermal pad is used, it must be connected as a secondary ground or left electrically open.

Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
7	1D	I/O	Common path for switch 1
1	$\overline{1EN}$	I	Active-low enable for switch 1
6	1S1	I/O	Switch 1 channel 1
5	1S2	I/O	Switch 1 channel 2
4	1S3	I/O	Switch 1 channel 3
3	1S4	I/O	Switch 1 channel 4
9	2D	I/O	Common path for switch 2
15	$\overline{2EN}$	I	Active-low enable for switch 2
10	2S1	I/O	Switch 2 channel 1
11	2S2	I/O	Switch 2 channel 2
12	2S3	I/O	Switch 2 channel 3
13	2S4	I/O	Switch 2 channel 4
8	GND	–	Ground
14	IN1	I	Switch 1 input select
2	IN2	I	Switch 2 input select
16	V+	–	Supply voltage

6 Specifications

6.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)^{(1) (2)}

			MIN	MAX	UNIT
V ₊	Supply voltage ⁽³⁾		-0.5	4.6	V
V _S , V _D	Analog voltage ^{(3) (4)}		-0.5	4.6	V
I _{SK} , I _{DK}	Analog port clamp current	V _S , V _D < 0	-50		mA
I _S , I _D	ON-state switch current	V _S , V _D = 0 to 7 V	-128	128	mA
V _I	Digital input voltage		-0.5	4.6	V
I _{IK}	Digital input clamp current ^{(3) (4)}	V _I < 0	-50		mA
I ₊	Continuous current through V ₊			100	mA
I _{GND}	Continuous current through GND		-100		mA
T _{stg}	Storage temperature		-65	150	°C

- Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
- All voltages are with respect to ground, unless otherwise specified.
- The input and output voltage ratings may be exceeded if their input and output clamp-current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	

- JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{I/O}	Switch input/output voltage range	0	3.6	V
V ₊	Supply voltage range	2.3	3.6	V
V _I	Control input voltage range	0	3.6	V
T _A	Operating Temperature Range	-40	125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TS3A5017-Q1	UNIT
		RGY (VQFN)	
		16 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	47.1	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	58.5	°C/W
R _{θJB}	Junction-to-board thermal resistance	24.0	°C/W
ψ _{JT}	Junction-to-top characterization parameter	1.8	°C/W
ψ _{JB}	Junction-to-board characterization parameter	24.0	°C/W

- For more information about traditional and new thermal metrics, see the [IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics for 3.3-V Supply

 $V_+ = 2.7 \text{ V to } 3.6 \text{ V}$, $T_A = -40^\circ\text{C to } 125^\circ\text{C}$ (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
Analog Switch								
V_D, V_S	Analog signal range				0		V_+	V
r_{on}	ON-state resistance	$0 \leq V_S \leq V_+$, $I_D = -32 \text{ mA}$,	Switch ON, see Figure 12	$T_A = 25^\circ\text{C}$ $V_+ = 3 \text{ V}$		11		Ω
				$T_A = \text{Full}$ $V_+ = 3 \text{ V}$			16	
Δr_{on}	ON-state resistance match between channels	$V_S = 2.1 \text{ V}$, $I_D = -32 \text{ mA}$,	Switch ON, see Figure 12	$T_A = 25^\circ\text{C}$ $V_+ = 3 \text{ V}$		1		Ω
				$T_A = \text{Full}$ $V_+ = 3 \text{ V}$			5	
$r_{on(\text{flat})}$	ON-state resistance flatness	$0 \leq V_S \leq V_+$, $I_D = -32 \text{ mA}$,	Switch ON, see Figure 12	$T_A = 25^\circ\text{C}$ $V_+ = 3 \text{ V}$		7		Ω
				$T_A = \text{Full}$ $V_+ = 3 \text{ V}$			12	
$I_{S(\text{OFF})}$	S OFF leakage current	$V_S = 1 \text{ V}, V_D = 3 \text{ V}$, or $V_S = 3 \text{ V}, V_D = 1 \text{ V}$,	Switch OFF, see Figure 13	$T_A = 25^\circ\text{C}$ $V_+ = 3.6 \text{ V}$		0.05		μA
				$T_A = \text{Full}$ $V_+ = 3.6 \text{ V}$			0.3	
$I_{SPWR(\text{OFF})}$		$V_S = 0 \text{ to } 3.6 \text{ V}$, $V_D = 3.6 \text{ V to } 0$,	Switch OFF, see Figure 13	$T_A = 25^\circ\text{C}$ $V_+ = 0 \text{ V}$		0.5		μA
				$T_A = \text{Full}$ $V_+ = 0 \text{ V}$			10	
$I_{D(\text{OFF})}$	D OFF leakage current	$V_S = 1 \text{ V}, V_D = 3 \text{ V}$, or $V_S = 3 \text{ V}, V_D = 1 \text{ V}$,	Switch OFF, see Figure 13	$T_A = 25^\circ\text{C}$ $V_+ = 3.6 \text{ V}$		0.05		μA
				$T_A = \text{Full}$ $V_+ = 3.6 \text{ V}$			0.3	
$I_{DPWR(\text{OFF})}$		$V_D = 0 \text{ to } 3.6 \text{ V}$, $V_S = 3.6 \text{ V to } 0$,	Switch OFF, see Figure 13	$T_A = 25^\circ\text{C}$ $V_+ = 0 \text{ V}$		0.5		μA
				$T_A = \text{Full}$ $V_+ = 0 \text{ V}$			20	
$I_{S(\text{ON})}$	S ON leakage current	$V_S = 1 \text{ V}, V_D = \text{Open}$, or $V_S = 3 \text{ V}, V_D = \text{Open}$,	Switch ON, see Figure 14	$T_A = 25^\circ\text{C}$ $V_+ = 3.6 \text{ V}$		0.05		μA
				$T_A = \text{Full}$ $V_+ = 3.6 \text{ V}$			0.3	
$I_{D(\text{ON})}$	D ON leakage current	$V_D = 1 \text{ V}, V_S = \text{Open}$, or $V_D = 3 \text{ V}, V_S = \text{Open}$,	Switch ON, see Figure 14	$T_A = 25^\circ\text{C}$ $V_+ = 3.6 \text{ V}$		0.05		μA
				$T_A = \text{Full}$ $V_+ = 3.6 \text{ V}$			0.3	
Digital Control Inputs (IN1, IN2, $\overline{\text{EN}}$)⁽²⁾								
V_{IH}	Input logic high			$T_A = \text{Full}$	2		V_+	V
V_{IL}	Input logic low			$T_A = \text{Full}$	0		0.8	V
I_{IH}, I_{IL}	Input leakage current	$V_I = V_+ \text{ or } 0$		$T_A = 25^\circ\text{C}$ $V_+ = 3.6 \text{ V}$		0.05		μA
				$T_A = \text{Full}$ $V_+ = 3.6 \text{ V}$			-1	
Q_C	Charge injection	$V_{GEN} = 0, R_{GEN} = 0$, $C_L = 0.1 \text{ nF}$,	See Figure 21	$T_A = 25^\circ\text{C}$ $V_+ = 3.3 \text{ V}$		5		pC
$C_{S(\text{OFF})}$	S OFF capacitance	$V_S = V_+ \text{ or GND}$, Switch OFF,	See Figure 15	$T_A = 25^\circ\text{C}$ $V_+ = 3.3 \text{ V}$		4.5		pF
$C_{D(\text{OFF})}$	D OFF capacitance	$V_D = V_+ \text{ or GND}$, Switch OFF,	See Figure 15	$T_A = 25^\circ\text{C}$ $V_+ = 3.3 \text{ V}$		19		pF
$C_{S(\text{ON})}$	S ON capacitance	$V_S = V_+ \text{ or GND}$, Switch ON,	See Figure 15	$T_A = 25^\circ\text{C}$ $V_+ = 3.3 \text{ V}$		27		pF

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics for 3.3-V Supply (continued)

 $V_+ = 2.7 \text{ V to } 3.6 \text{ V}$, $T_A = -40^\circ\text{C to } 125^\circ\text{C}$ (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$C_{D(ON)}$	D ON capacitance	$V_D = V_+$ or GND, Switch ON,	See Figure 15	$T_A = 25^\circ\text{C}$ $V_+ = 3.3 \text{ V}$		27		pF
C_I	Digital input capacitance	$V_I = V_+$ or GND,	See Figure 15	$T_A = 25^\circ\text{C}$ $V_+ = 3.3 \text{ V}$		3		pF
BW	Bandwidth	$R_L = 50 \ \Omega$, Switch ON,	See Figure 17	$T_A = 25^\circ\text{C}$ $V_+ = 3.3 \text{ V}$		165		MHz
O_{ISO}	OFF isolation	$R_L = 50 \ \Omega$, $f = 1 \text{ MHz}$,	See Figure 18	$T_A = 25^\circ\text{C}$ $V_+ = 3.3 \text{ V}$		-69		dB
O_{ISO}	OFF isolation	$R_L = 50 \ \Omega$, $f = 10 \text{ MHz}$,	See Figure 18	$T_A = 25^\circ\text{C}$ $V_+ = 3.3 \text{ V}$		-49		dB
X_{TALK}	Crosstalk	$R_L = 50 \ \Omega$, $f = 1 \text{ MHz}$,	See Figure 19	$T_A = 25^\circ\text{C}$ $V_+ = 3.3 \text{ V}$		-69		dB
$X_{TALK(ADJ)}$	Crosstalk adjacent	$R_L = 50 \ \Omega$, $f = 1 \text{ MHz}$,	See Figure 20	$T_A = 25^\circ\text{C}$ $V_+ = 3.3 \text{ V}$		-80		dB
THD	Total harmonic distortion	$R_L = 600 \ \Omega$, $C_L = 50 \text{ pF}$,	$f = 20 \text{ Hz to } 20 \text{ kHz}$, see Figure 22	$T_A = 25^\circ\text{C}$ $V_+ = 3.3 \text{ V}$		0.25		%
Supply								
I_+	Positive supply current	$V_I = V_+$ or GND,	Switch ON or OFF	$T_A = 25^\circ\text{C}$ $V_+ = 3.6 \text{ V}$		2.5	7	μA
				$T_A = \text{Full}$ $V_+ = 3.6 \text{ V}$			10	

6.6 Electrical Characteristics for 2.5-V Supply

 $V_+ = 2.3 \text{ V to } 2.7 \text{ V}$, $T_A = -40^\circ\text{C to } 125^\circ\text{C}$ (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
Analog Switch								
V_D, V_S	Analog signal range				0		V_+	V
r_{on}	ON-state resistance	$0 \leq V_S \leq V_+$, $I_D = -24 \text{ mA}$,	Switch ON, see Figure 12	$T_A = 25^\circ\text{C}$ $V_+ = 2.3 \text{ V}$		22		Ω
				$T_A = \text{Full}$ $V_+ = 2.3 \text{ V}$			28	
Δr_{on}	ON-state resistance match between channels	$V_S = 1.6 \text{ V}$, $I_D = -24 \text{ mA}$,	Switch ON, see Figure 12	$T_A = 25^\circ\text{C}$ $V_+ = 2.3 \text{ V}$		1		Ω
				$T_A = \text{Full}$ $V_+ = 2.3 \text{ V}$			5	
$r_{on(\text{flat})}$	ON-state resistance flatness	$0 \leq V_S \leq V_+$, $I_D = -24 \text{ mA}$,	Switch ON, see Figure 12	$T_A = 25^\circ\text{C}$ $V_+ = 2.3 \text{ V}$		18		Ω
				$T_A = \text{Full}$ $V_+ = 2.3 \text{ V}$			24	
$I_{S(\text{OFF})}$	S OFF leakage current	$V_S = 0.5 \text{ V}$, $V_D = 2.2 \text{ V}$, or $V_S = 2.2 \text{ V}$, $V_D = 0.5 \text{ V}$,	Switch OFF, see Figure 13	$T_A = 25^\circ\text{C}$ $V_+ = 2.7 \text{ V}$		0.05		μA
				$T_A = \text{Full}$ $V_+ = 2.7 \text{ V}$		-0.3	0.3	
$I_{SPWR(\text{OFF})}$		$V_S = 0 \text{ to } 2.7 \text{ V}$, $V_D = 2.7 \text{ V to } 0$,		$T_A = 25^\circ\text{C}$ $V_+ = 0 \text{ V}$		0.5		
				$T_A = \text{Full}$ $V_+ = 0 \text{ V}$		-15	15	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

Electrical Characteristics for 2.5-V Supply (continued)
 $V_+ = 2.3 \text{ V to } 2.7 \text{ V}$, $T_A = -40^\circ\text{C to } 125^\circ\text{C}$ (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{D(OFF)}$	D OFF leakage current	$V_S = 0.5 \text{ V}$, $V_D = 2.2 \text{ V}$, or $V_S = 2.2 \text{ V}$, $V_D = 0.5 \text{ V}$,	Switch OFF, see Figure 13	$T_A = 25^\circ\text{C}$ $V_+ = 2.7 \text{ V}$	0.05		μA
				$T_A = \text{Full}$ $V_+ = 2.7 \text{ V}$	-0.3	0.3	
$I_{DPWR(OFF)}$		$V_D = 0 \text{ to } 2.7 \text{ V}$, $V_S = 2.7 \text{ V to } 0$,		$T_A = 25^\circ\text{C}$ $V_+ = 0 \text{ V}$	0.5		
				$T_A = \text{Full}$ $V_+ = 0 \text{ V}$	-20	20	
$I_{S(ON)}$	S ON leakage current	$V_S = 0.5 \text{ V}$, $V_D = \text{Open}$, or $V_S = 2.2 \text{ V}$, $V_D = \text{Open}$,	Switch ON, see Figure 14	$T_A = 25^\circ\text{C}$ $V_+ = 2.7 \text{ V}$	0.05		μA
				$T_A = \text{Full}$ $V_+ = 2.7 \text{ V}$	-0.3	0.3	
$I_{D(ON)}$	D ON leakage current	$V_D = 0.5 \text{ V}$, $V_S = \text{Open}$, or $V_D = 2.2 \text{ V}$, $V_S = \text{Open}$,	Switch ON, see Figure 14	$T_A = 25^\circ\text{C}$ $V_+ = 2.7 \text{ V}$	0.05		μA
				$T_A = \text{Full}$ $V_+ = 2.7 \text{ V}$	-0.3	0.3	
Logic Inputs (IN1, IN2, EN)⁽²⁾							
V_{IH}	Input logic high			$T_A = \text{Full}$	1.7	V_+	V
V_{IL}	Input logic low			$T_A = \text{Full}$	0	0.7	V
I_{IH} , I_{IL}	Input leakage current	$V_I = V_+ \text{ or } 0$		$T_A = 25^\circ\text{C}$ $V_+ = 2.7 \text{ V}$	0.05		μA
				$T_A = \text{Full}$ $V_+ = 2.7 \text{ V}$	-1	1	
Q_C	Charge injection	$V_{GEN} = 0$, $R_{GEN} = 0$, $C_L = 0.1 \text{ nF}$,	See Figure 21	$T_A = \text{Full}$ $V_+ = 2.5 \text{ V}$	3		pC
$C_{S(OFF)}$	S OFF capacitance	$V_S = V_+ \text{ or GND}$, Switch OFF,	See Figure 15	$T_A = \text{Full}$ $V_+ = 2.5 \text{ V}$	4.5		pF
$C_{D(OFF)}$	D OFF capacitance	$V_D = V_+ \text{ or GND}$, Switch OFF,	See Figure 15	$T_A = \text{Full}$ $V_+ = 2.5 \text{ V}$	18.5		pF
$C_{S(ON)}$	S ON capacitance	$V_S = V_+ \text{ or GND}$, Switch ON,	See Figure 15	$T_A = \text{Full}$ $V_+ = 2.5 \text{ V}$	26		pF
$C_{D(ON)}$	D ON capacitance	$V_D = V_+ \text{ or GND}$, Switch ON,	See Figure 15	$T_A = \text{Full}$ $V_+ = 2.5 \text{ V}$	26		pF
C_I	Digital input capacitance	$V_I = V_+ \text{ or GND}$,	See Figure 15	$T_A = \text{Full}$ $V_+ = 2.5 \text{ V}$	3		pF
BW	Bandwidth	$R_L = 50 \Omega$, Switch ON,	See Figure 17	$T_A = \text{Full}$ $V_+ = 2.5 \text{ V}$	165		MHz
O_{ISO}	OFF isolation	$R_L = 50 \Omega$, $f = 1 \text{ MHz}$,	See Figure 18	$T_A = \text{Full}$ $V_+ = 2.5 \text{ V}$	-69		dB
O_{ISO}	OFF isolation	$R_L = 50 \Omega$, $f = 10 \text{ MHz}$,	See Figure 18	$T_A = \text{Full}$ $V_+ = 2.5 \text{ V}$	-49		dB
X_{TALK}	Crosstalk	$R_L = 50 \Omega$, $f = 1 \text{ MHz}$,	See Figure 19	$T_A = \text{Full}$ $V_+ = 2.5 \text{ V}$	-69		dB
$X_{TALK(ADJ)}$	Crosstalk adjacent	$R_L = 50 \Omega$, $f = 1 \text{ MHz}$,	See Figure 20	$T_A = \text{Full}$ $V_+ = 2.5 \text{ V}$	-85		dB
THD	Total harmonic distortion	$R_L = 600 \Omega$, $C_L = 50 \text{ pF}$,	$f = 20 \text{ Hz to } 20 \text{ kHz}$, see Figure 22	$T_A = \text{Full}$ $V_+ = 2.5 \text{ V}$	0.3		%
Supply							

(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics for 2.5-V Supply (continued)

 $V_+ = 2.3 \text{ V to } 2.7 \text{ V}$, $T_A = -40^\circ\text{C to } 125^\circ\text{C}$ (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
I_+	Positive supply current	$V_I = V_+$ or GND,	Switch ON or OFF	$T_A = \text{Full}$ $V_+ = 2.7 \text{ V}$	2.5	7	μA	
				$T_A = \text{Full}$ $V_+ = 2.7 \text{ V}$				

6.7 Switching Characteristics for 3.3-V Supply

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{ON}	Turnon time ⁽¹⁾	$V_D = 2 \text{ V}$, $R_L = 300 \Omega$,	$C_L = 35 \text{ pF}$, see Figure 16	$T_A = 25^\circ\text{C}$ $V_+ = 3.3 \text{ V}$	5	9.5	ns	
				$T_A = \text{Full}$ $V_+ = 3 \text{ V to } 3.6 \text{ V}$				
t_{OFF}	Turnoff time ⁽¹⁾	$V_D = 2 \text{ V}$, $R_L = 300 \Omega$,	$C_L = 35 \text{ pF}$, see Figure 16	$T_A = 25^\circ\text{C}$ $V_+ = 3.3 \text{ V}$	1.5	3.5	ns	
				$T_A = \text{Full}$ $V_+ = 3 \text{ V to } 3.6 \text{ V}$				

(1) Specified by design, not tested in production

6.8 Switching Characteristics for 2.5-V Supply

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{ON}	Turnon time ⁽¹⁾	$V_{\text{COM}} = 2 \text{ V}$, $R_L = 300 \Omega$,	$C_L = 35 \text{ pF}$, see Figure 16	$T_A = 25^\circ\text{C}$ $V_+ = 2.5 \text{ V}$	5	8	ns	
				$T_A = \text{Full}$ $V_+ = 2.3 \text{ V to } 2.7 \text{ V}$				
t_{OFF}	Turnoff time ⁽¹⁾	$V_{\text{COM}} = 2 \text{ V}$, $R_L = 300 \Omega$,	$C_L = 35 \text{ pF}$, see Figure 16	$T_A = 25^\circ\text{C}$ $V_+ = 2.5 \text{ V}$	2	4.5	ns	
				$T_A = \text{Full}$ $V_+ = 2.3 \text{ V to } 2.7 \text{ V}$				

(1) Specified by design, not tested in production.

6.9 Typical Characteristics

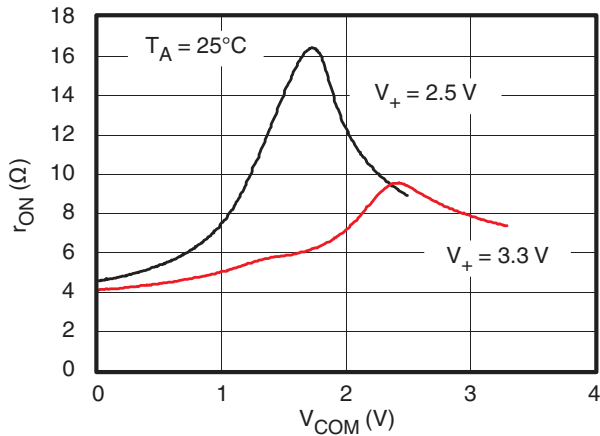


Figure 1. r_{on} vs V_{COM}

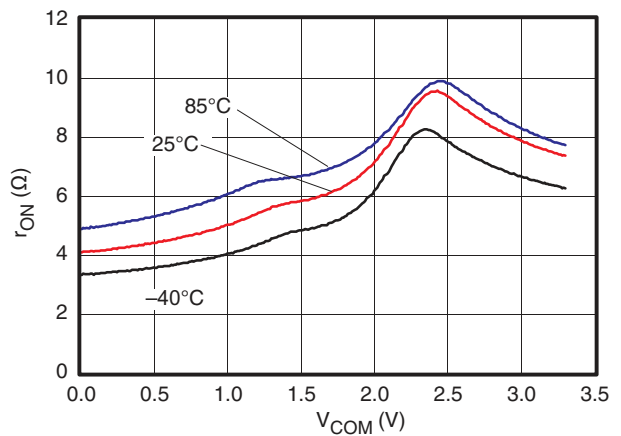


Figure 2. r_{on} vs V_{COM} ($V_+ = 3.3$ V)

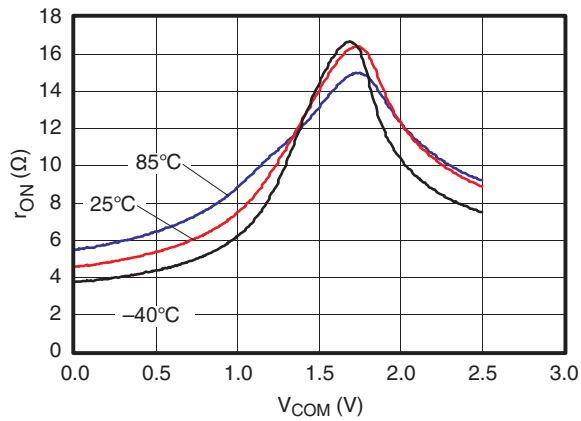


Figure 3. r_{on} vs V_{COM} ($V_+ = 2.5$ V)

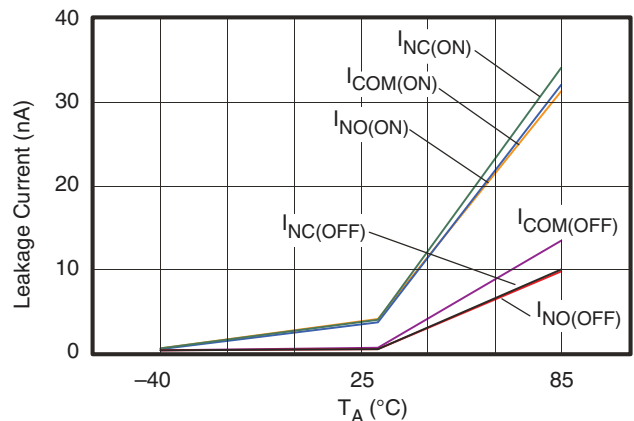


Figure 4. Leakage Current vs Temperature ($V_+ = 3.6$ V)

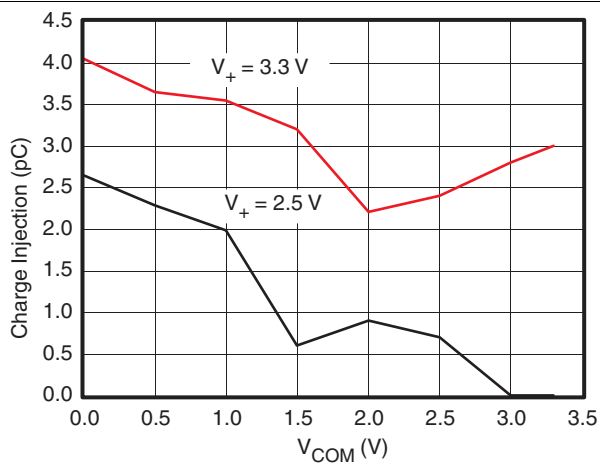


Figure 5. Charge Injection (Q_C) vs V_{COM}

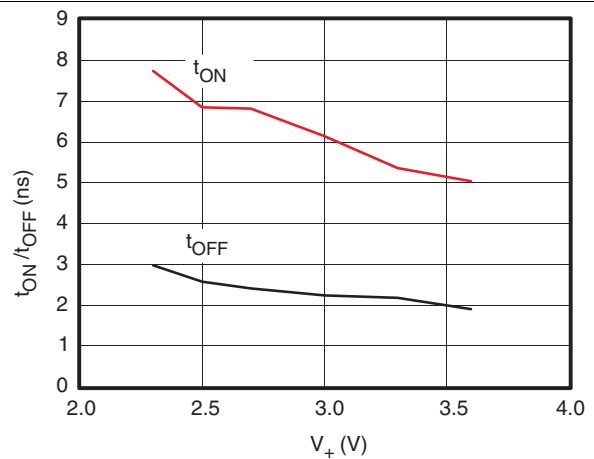


Figure 6. t_{ON} and t_{OFF} vs Supply Voltage

Typical Characteristics (continued)

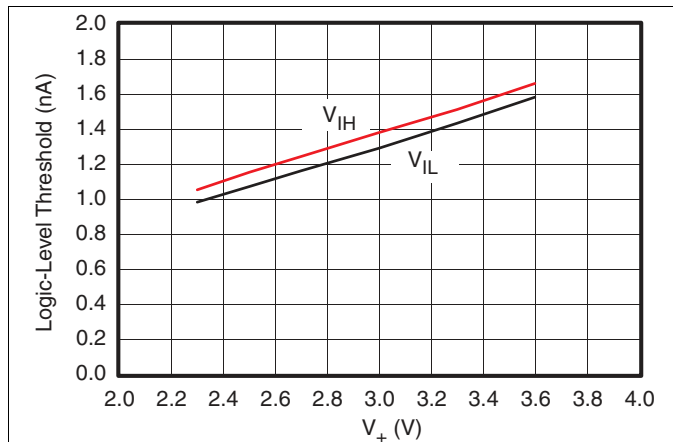


Figure 7. Logic-Level Threshold vs V_+

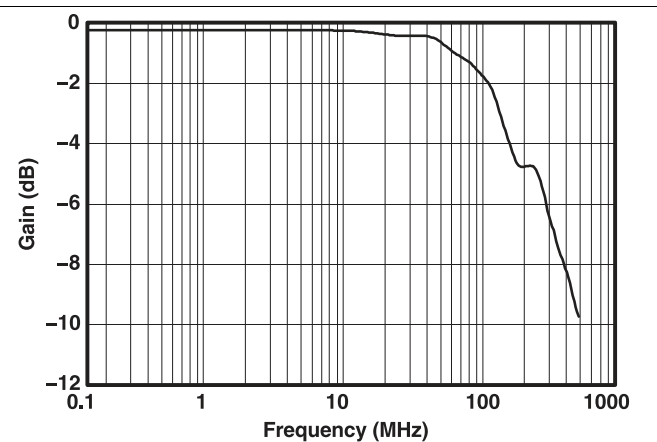


Figure 8. Bandwidth (Gain vs Frequency) ($V_+ = 3.3$ V)

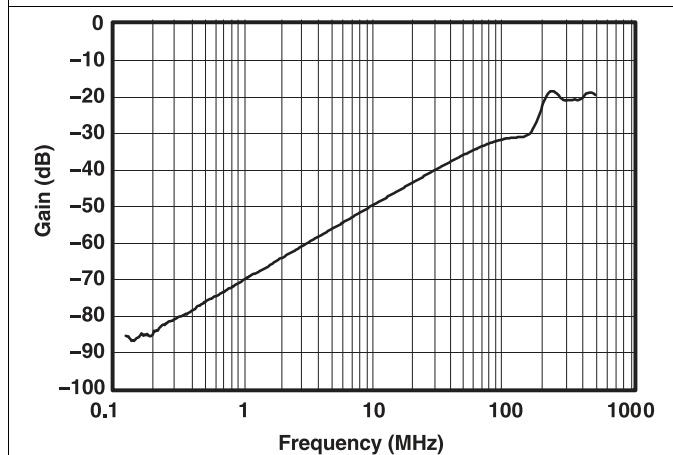


Figure 9. OFF Isolation and Crosstalk vs Frequency ($V_+ = 3.3$ V)

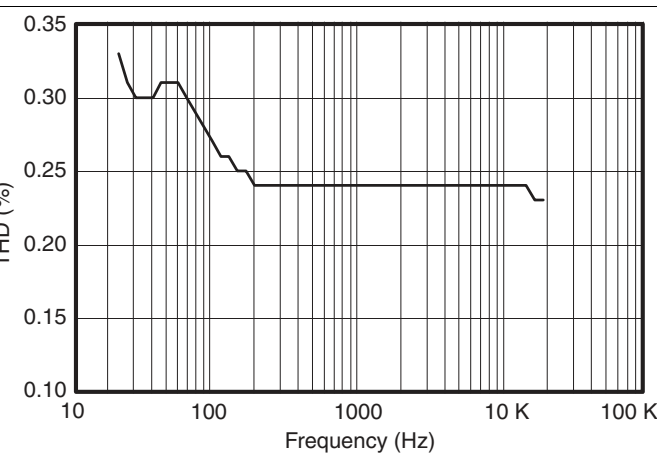


Figure 10. Total Harmonic Distortion vs Frequency

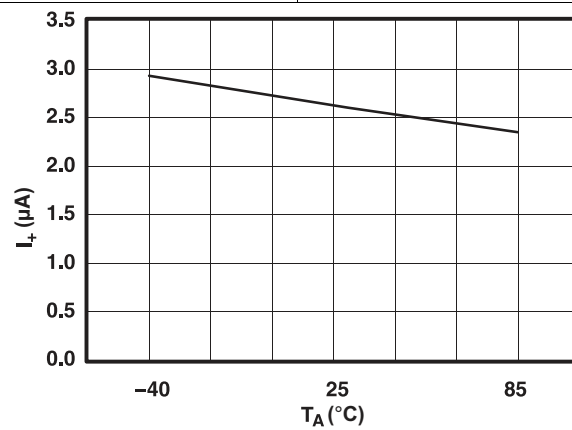


Figure 11. Power-Supply Current vs Temperature ($V_+ = 3.6$ V)

7 Parameter Measurement Information

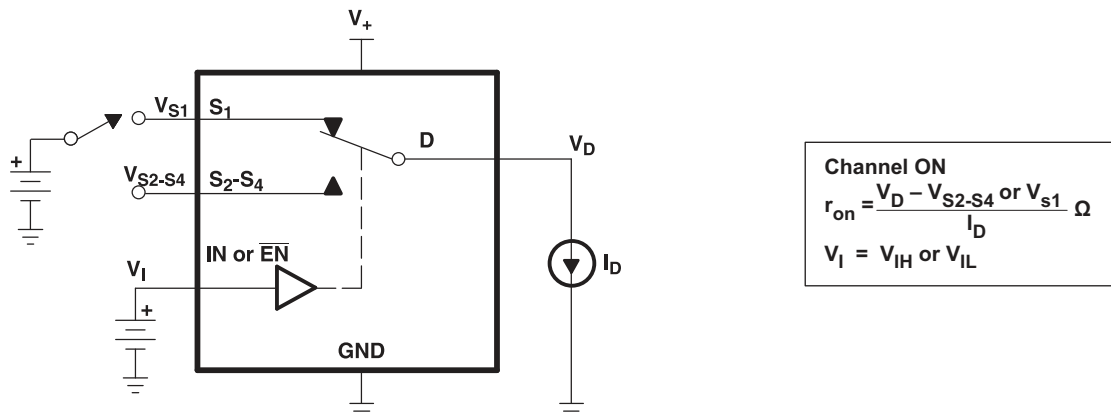


Figure 12. ON-State Resistance (r_{on})

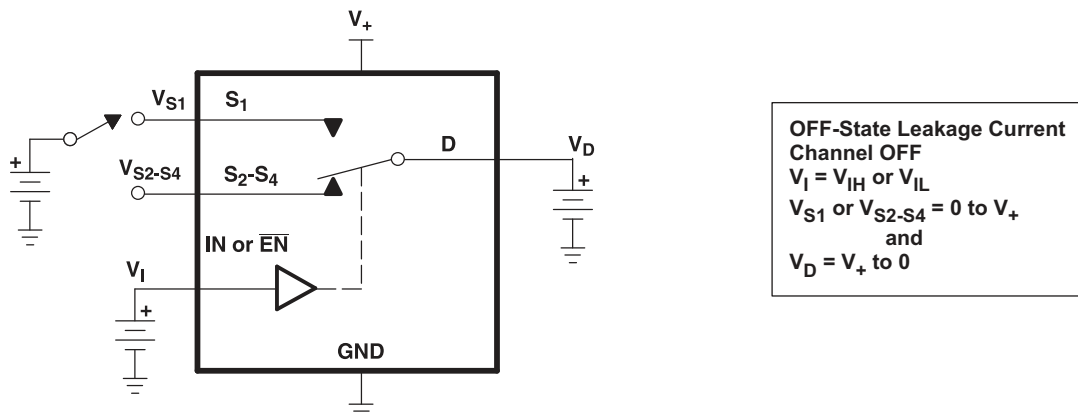


Figure 13. OFF-State Leakage Current ($I_{D(OFF)}$, $I_{S(OFF)}$)

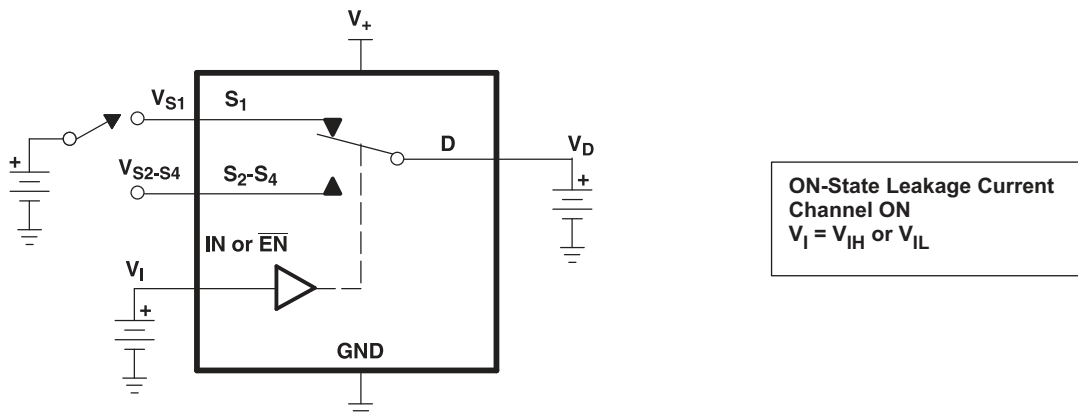


Figure 14. ON-State Leakage Current ($I_{D(ON)}$, $I_{S(ON)}$)

Parameter Measurement Information (continued)

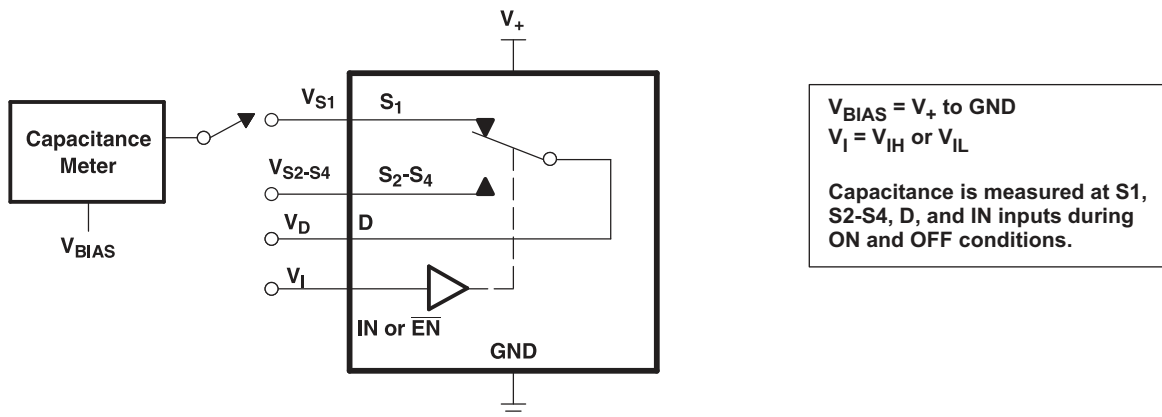


Figure 15. Capacitance (C_I , $C_{D(OFF)}$, $C_{D(ON)}$, $C_{S(OFF)}$, $C_{S(ON)}$)

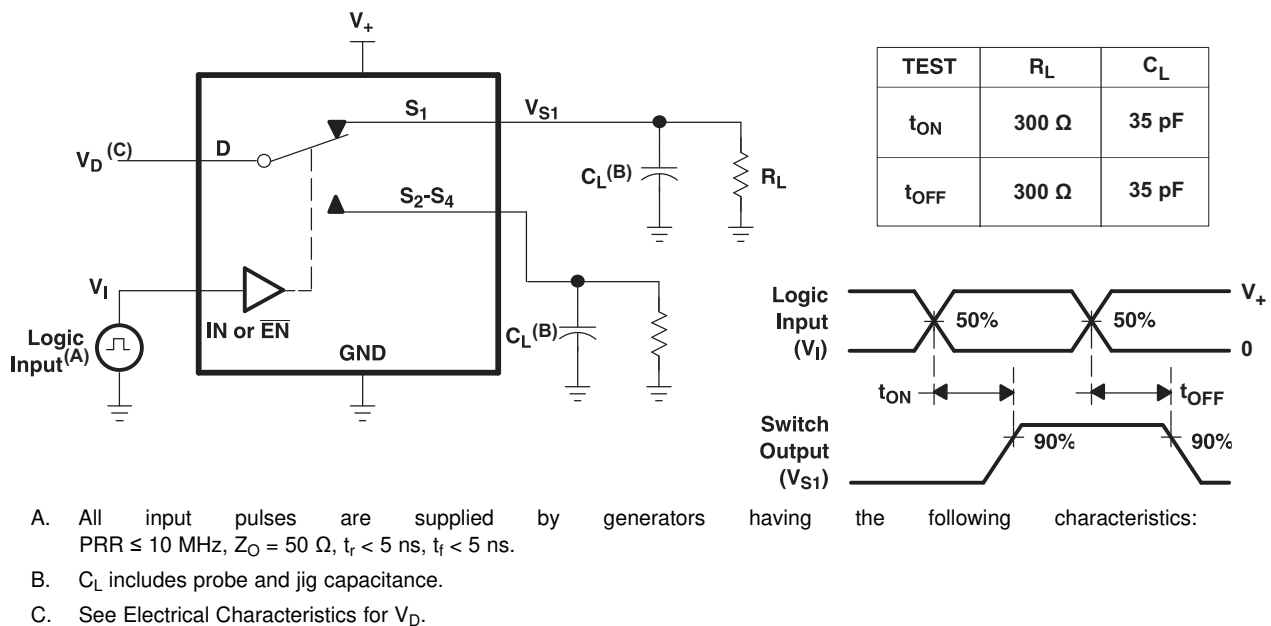


Figure 16. Turnon (t_{ON}) and Turnoff Time (t_{OFF})

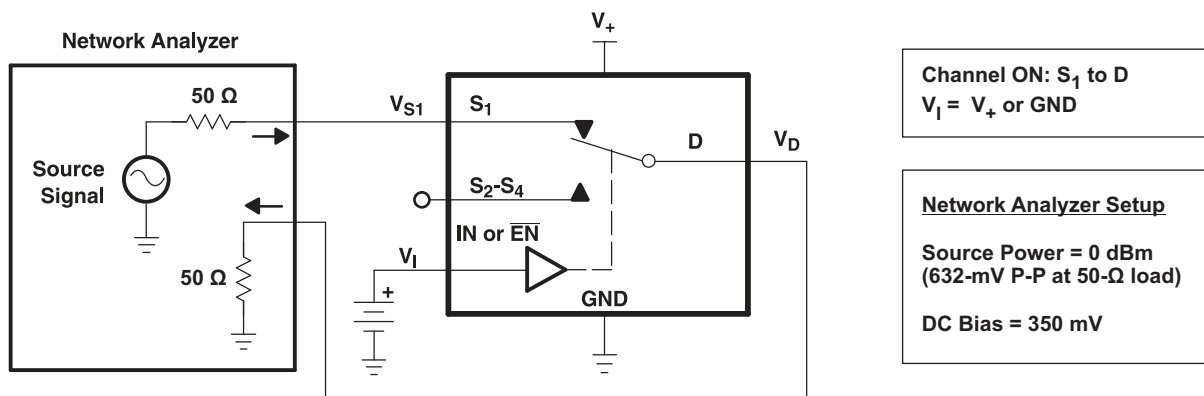


Figure 17. Bandwidth (BW)

Parameter Measurement Information (continued)

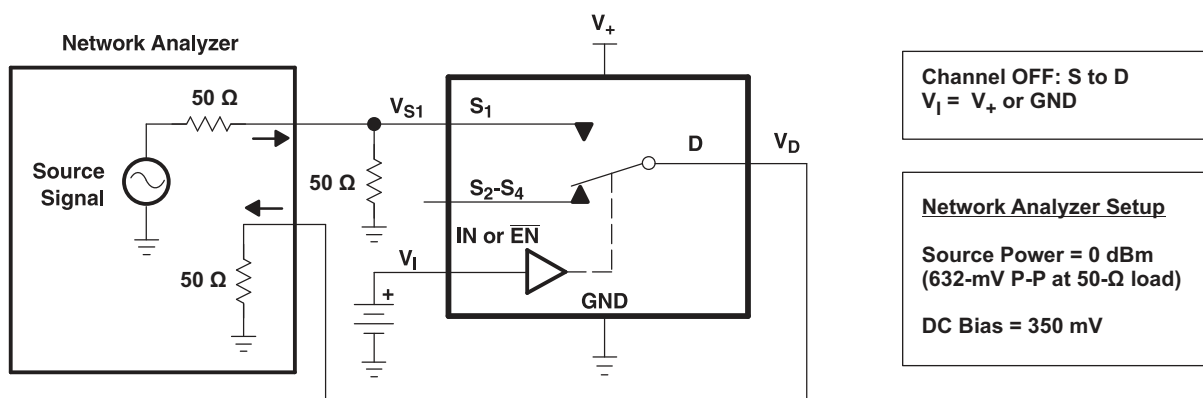


Figure 18. OFF Isolation (O_{ISO})

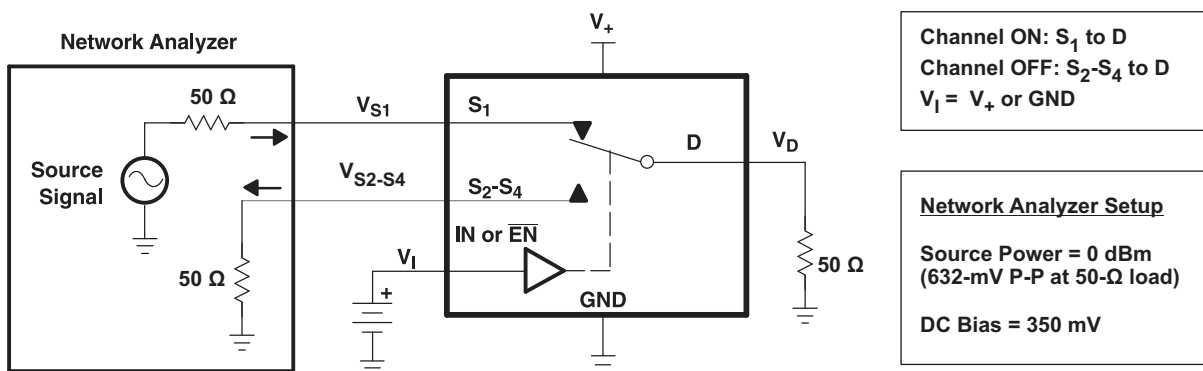


Figure 19. Crosstalk (X_{TALK})

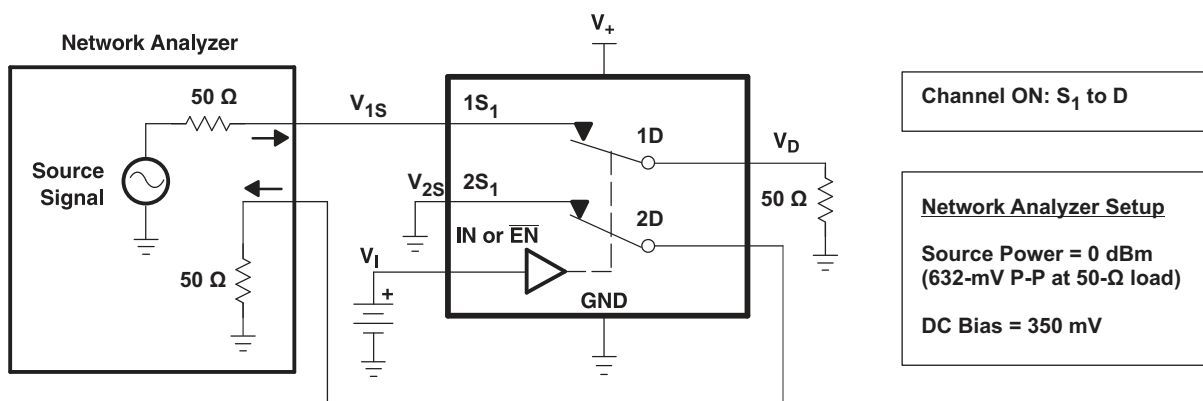
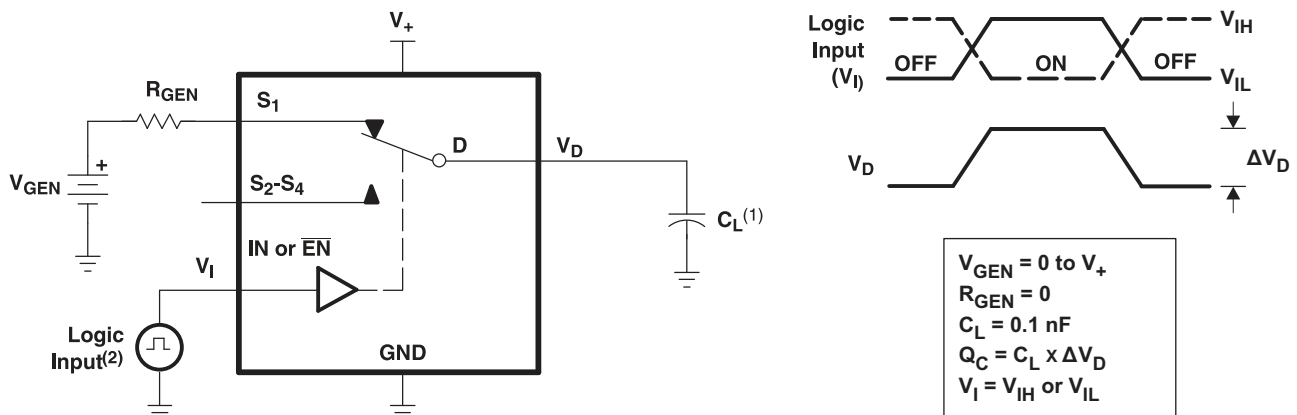


Figure 20. Adjacent Crosstalk (X_{TALK})

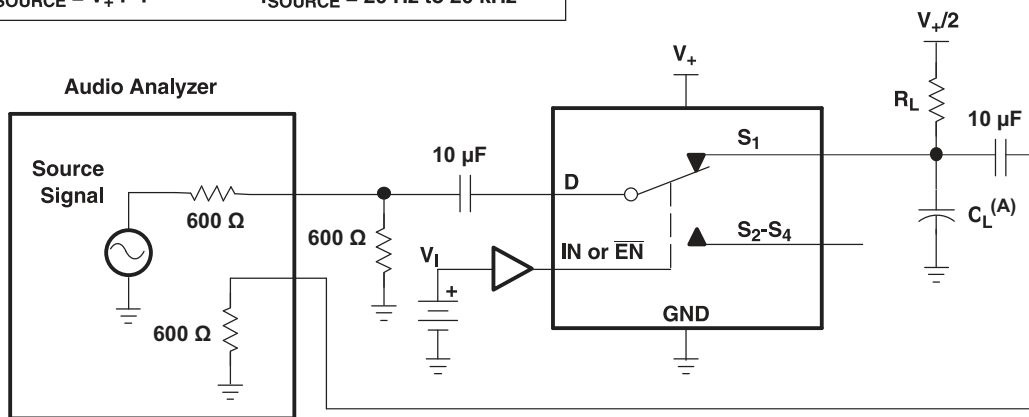
Parameter Measurement Information (continued)



- A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.
- B. C_L includes probe and jig capacitance.

Figure 21. Charge Injection (Q_C)

Channel ON: D to S	V _I = V _{IH} or V _{IL}
V _{SOURCE} = V ₊ P-P	f _{SOURCE} = 20 Hz to 20 kHz



- A. C_L includes probe and jig capacitance.

Figure 22. Total Harmonic Distortion (THD)

8 Detailed Description

8.1 Overview

The TS3A5017-Q1 is a dual Single-Pole-4-Throw (SP4T) solid-state analog switch. The TS3A5017-Q1, like all analog switches, is bidirectional. Each D pin connects to its four respective S pins, with the switch connection dependent on the status of $\overline{\text{EN}}$, IN2, and IN1. See [Table 1](#) for the switch configuration truth table.

8.2 Functional Block Diagram

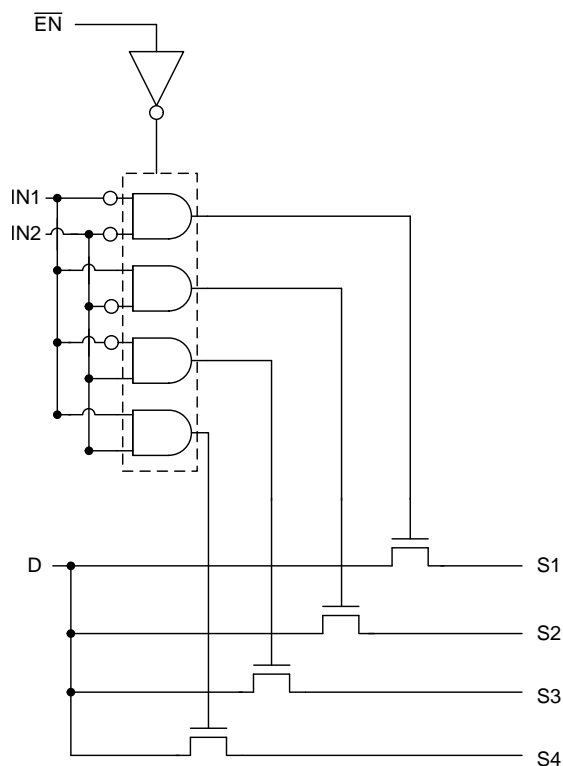


Figure 23. Functional Block Diagram (Each Switch)

8.3 Feature Description

Isolation in powered-down mode allows signals to be present at the inputs while the switch is powered off without causing damage to the device. The low ON-state resistance and low charge injection give the TS3A5017-Q1 better performance at higher speeds.

8.4 Device Functional Modes

Table 1. Function Table

$\overline{\text{EN}}$	IN2	IN1	D TO S, S TO D
L	L	L	D = S ₁
L	L	H	D = S ₂
L	H	L	D = S ₃
L	H	H	D = S ₄
H	X	X	OFF

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TS3A5017-Q1 can be used in a variety of customer systems. The TS3A5017-Q1 can be used anywhere multiple analog or digital signals must be selected to pass across a single line.

9.2 Typical Application

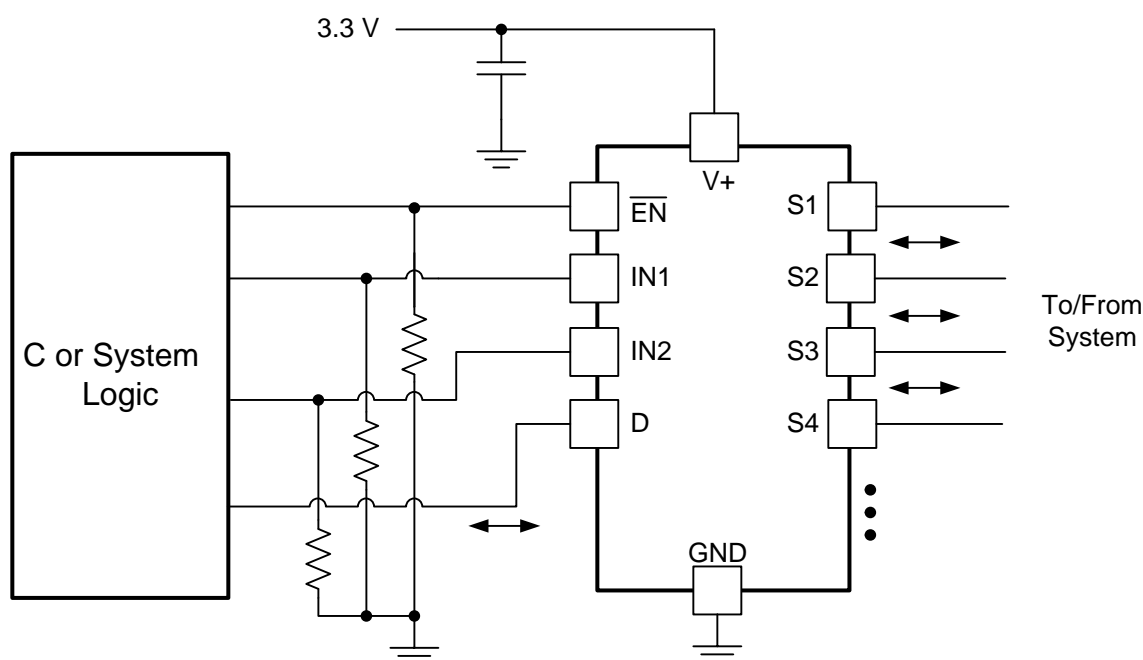


Figure 24. System Schematic for TS3A5017-Q1

9.2.1 Design Requirements

In this particular application, $V+$ was 3.3 V, although $V+$ is allowed to be any voltage specified in *Recommended Operating Conditions*. A decoupling capacitor is recommended on the $V+$ pin. See [Power Supply Recommendations](#) for more details.

9.2.2 Detailed Design Procedure

In this application, \overline{EN} , IN1, and IN2 are, by default, pulled low to GND. Choose these resistor sizes based on the current driving strength of the GPIO, the desired power consumption, and the switching frequency (if applicable). If the GPIO is open-drain, use pullup resistors instead.

Typical Application (continued)

9.2.3 Application Curve

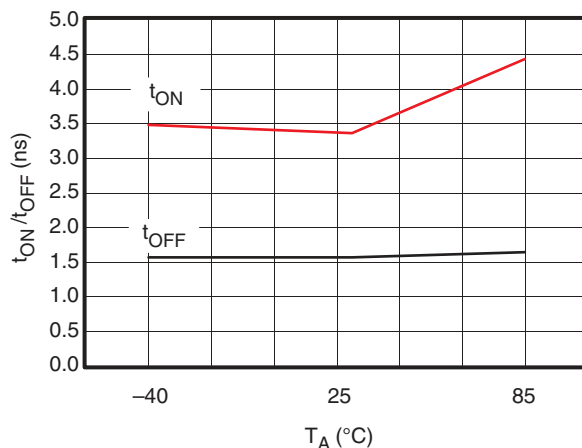


Figure 25. t_{ON} and t_{OFF} vs Temperature (V₊ = 3.3 V)

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operation Conditions*.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-μF bypass capacitor is recommended. If there are multiple pins labeled V_{CC}, then a 0.01-μF or 0.022-μF capacitor is recommended for each V_{CC} because the V_{CC} pins will be tied together internally. For devices with dual-supply pins operating at different voltages, for example V_{CC} and V_{DD}, a 0.1-μF bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self-inductance of the trace — resulting in the reflection. It is a given that not all PCB traces can be straight, and the traces will turn corners. [Figure 26](#) shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

Unused switch I/Os, such as NO, NC, and COM, can be left floating or tied to GND. However, the IN1, IN2, and $\overline{\text{EN}}$ pins must be driven high or low. Due to partial transistor turnon when control inputs are at threshold levels, floating control inputs can cause increased I_{CC} or unknown switch selection states. See *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#) for more details.

11.2 Layout Example

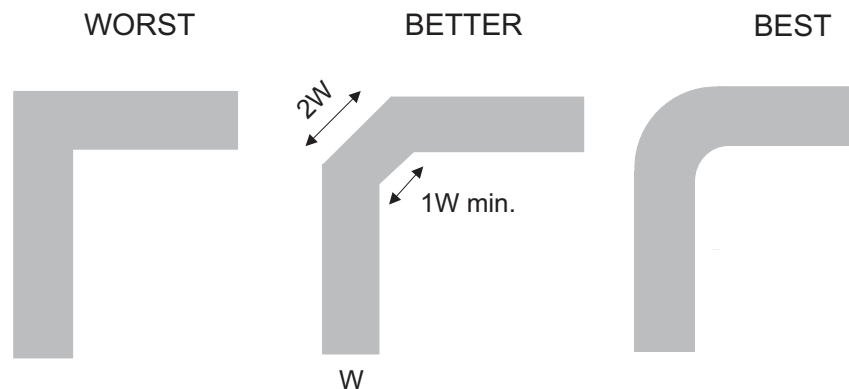


Figure 26. Trace Example

12 Device and Documentation Support

12.1 Device Support

12.1.1 Device Nomenclature

Table 2. Parameter Description

SYMBOL	DESCRIPTION
V_{COM}	Voltage at COM
V_{NC}	Voltage at NC
V_{NO}	Voltage at NO
r_{on}	Resistance between COM and NC or NO ports when the channel is ON
Δr_{on}	Difference of r_{on} between channels in a specific device
$r_{on(flat)}$	Difference between the maximum and minimum value of r_{on} in a channel over the specified range of conditions
$I_{NC(OFF)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the OFF state
$I_{NC(ON)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the ON state and the output (COM) open
$I_{NO(OFF)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state
$I_{NO(ON)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) open
$I_{COM(OFF)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NC or NO) in the OFF state
$I_{COM(ON)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NC or NO) in the ON state and the output (NC or NO) open
V_{IH}	Minimum input voltage for logic high for the control input (IN, \overline{EN})
V_{IL}	Maximum input voltage for logic low for the control input (IN, \overline{EN})
V_I	Voltage at the control input (IN, \overline{EN})
I_{IH}, I_{IL}	Leakage current measured at the control input (IN, \overline{EN})
t_{ON}	Turnon time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (NC or NO) signal when the switch is turning ON.
t_{OFF}	Turnoff time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (NC or NO) signal when the switch is turning OFF.
Q_C	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NC or NO) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_C = C_L \times \Delta V_{COM}$, C_L is the load capacitance and ΔV_{COM} is the change in analog output voltage.
$C_{NC(OFF)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is OFF
$C_{NC(ON)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is ON
$C_{NO(OFF)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is OFF
$C_{NO(ON)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is ON
$C_{COM(OFF)}$	Capacitance at the COM port when the corresponding channel (COM to NC) is OFF
$C_{COM(ON)}$	Capacitance at the COM port when the corresponding channel (COM to NC) is ON
C_I	Capacitance of control input (IN, \overline{EN})
O_{ISO}	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NC to COM) in the OFF state.
X_{TALK}	Crosstalk is a measurement of unwanted signal coupling from an ON channel to an OFF channel (NC1 to NO1). Adjacent crosstalk is a measure of unwanted signal coupling from an ON channel to an adjacent ON channel (NC1 to NC2). This is measured in a specific frequency and in dB.
BW	Bandwidth of the switch. This is the frequency in which the gain of an ON channel is –3 dB below the DC gain.
THD	Total harmonic distortion describes the signal distortion caused by the analog switch. This is defined as the ratio of root mean square (RMS) value of the second, third, and higher harmonic to the absolute magnitude of the fundamental harmonic.
I_+	Static power-supply current with the control (IN) pin at V_+ or GND

12.2 Documentation Support

12.2.1 Related Documentation

- *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#)

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.

12.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS3A5017QRGYRQ1	ACTIVE	VQFN	RGY	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	5017Q	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TS3A5017-Q1 :

- Catalog: [TS3A5017](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3A5017QRGYRQ1	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

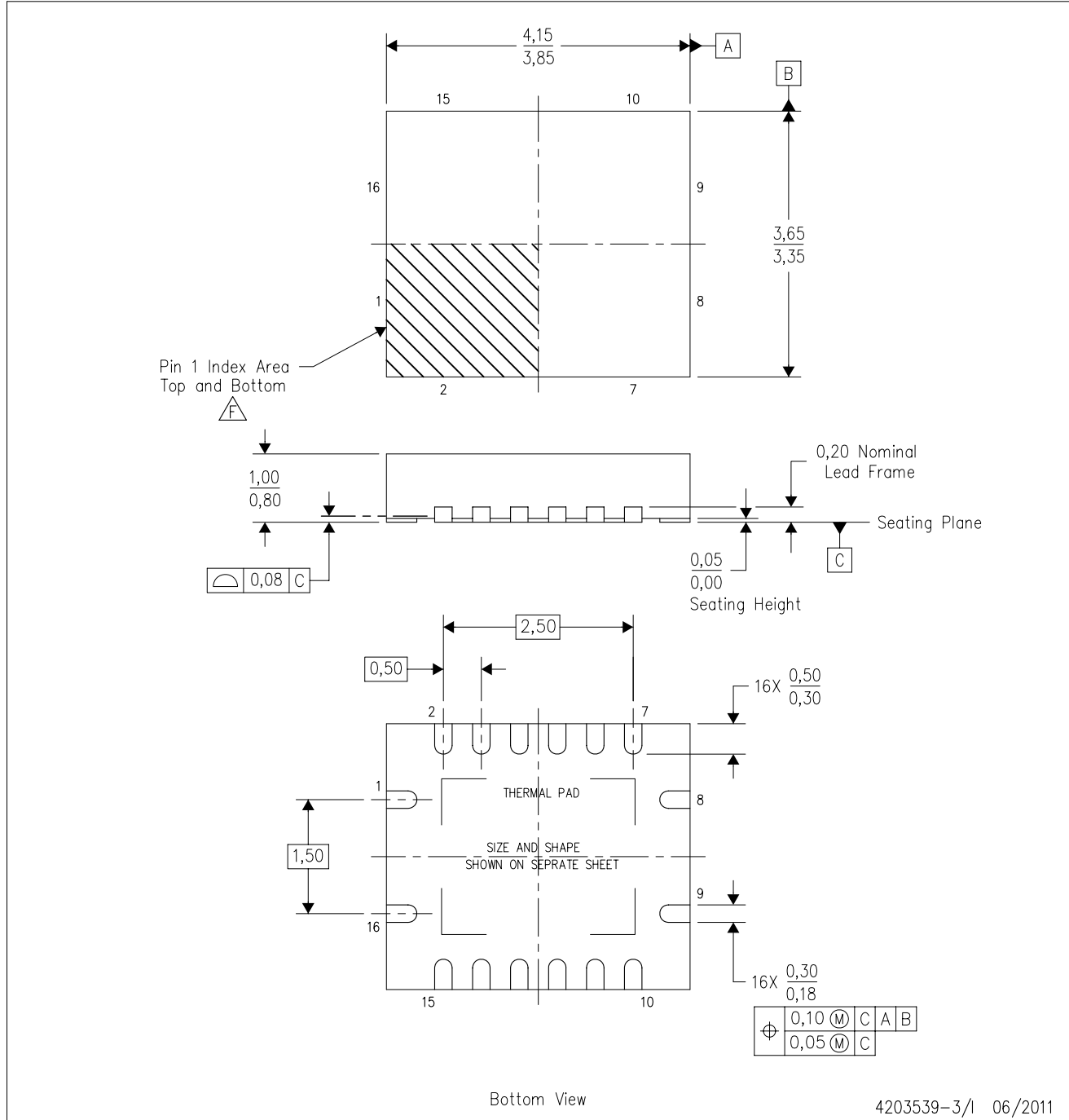
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3A5017QRGYRQ1	VQFN	RGY	16	3000	367.0	367.0	35.0

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
 - G. Package complies to JEDEC MO-241 variation BA.

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