TC4421M/TC4422M

9A High-Speed MOSFET Drivers

Features

- High Peak Output Current: 9A
- Wide Input Supply Voltage Operating Range:
  - 4.5V to 18V
- High Continuous Output Current: 2A Max
- Fast Rise and Fall Times:
  - 30 ns with 4,700 pF Load
  - 180 ns with 47,000 pF Load
- Short Propagation Delays: 30 ns (typ)
- Low Supply Current:
  - With Logic '1' Input – 200 µA (typ)
  - With Logic '0' Input – 55 µA (typ)
- Low Output Impedance: 1.4Ω (typ)
- Latch-Up Protected: Will Withstand 1.5A Output Reverse Current
- Input: Will Withstand Negative Inputs Up To 5V
- Pin-Compatible with the TC4420M/TC4429M 6A MOSFET Driver
- Wide Operating Temperature Range:
  - -55°C to +125°C
- See TC4421/TC4422 Data Sheet (DS21420) for additional temperature range and package offerings

Applications

- Line Drivers for Extra Heavily-Loaded Lines
- Pulse Generators
- Driving the Largest MOSFETs and IGBTs
- Local Power ON/OFF Switch
- Motor and Solenoid Driver

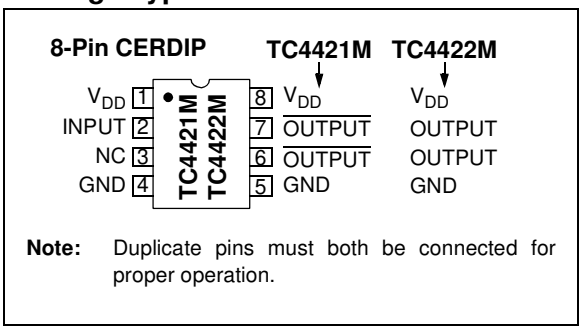
General Description

The TC4421M/TC4422M are high-current buffer/drivers capable of driving large MOSFETs and IGBTs.

They are essentially immune to any form of upset, except direct overvoltage or over-dissipation. They cannot be latched, under any conditions, within their power and voltage ratings. These parts are not subject to damage or improper operation when up to 5V of ground bounce is present on their ground terminals. They can accept, without damage or logic upset, more than 1A inductive current of either polarity being forced back into their outputs. In addition, all terminals are fully protected against up to 4 kV of electrostatic discharge.

The TC4421M/TC4422M inputs may be driven directly from either TTL or CMOS (3V to 18V). In addition, 300 mV of hysteresis is built into the input, providing noise immunity and allowing the device to be driven from slowly rising or falling waveforms.

Package Types



Note: Duplicate pins must both be connected for proper operation.

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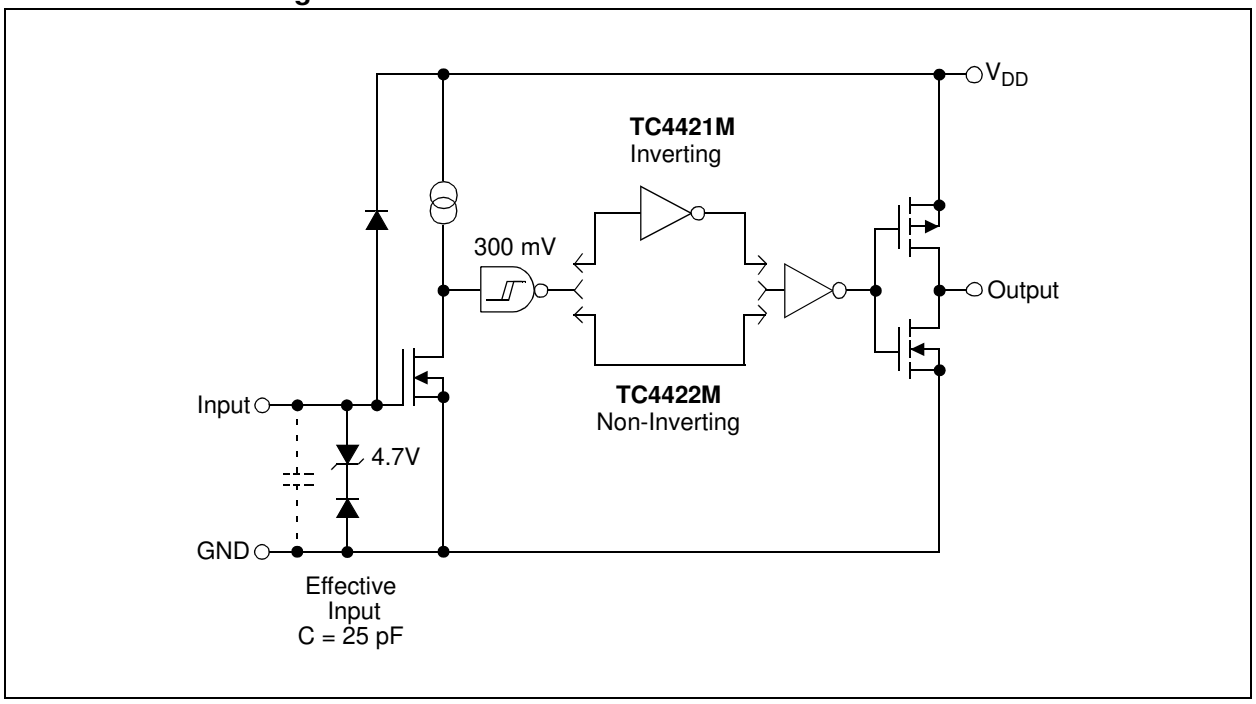
Functional Block Diagram



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Supply Voltage ..... +20V
Input Voltage ..... (V_{DD} + 0.3V) to (GND – 5V)
Input Current (V_{IN} > V_{DD}) ..... 50 mA

† Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, T_A = +25°C with 4.5V ≤ V_{DD} ≤ 18V.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input						
Logic '1', High Input Voltage	V_{IH}	2.4	1.8	—	V	
Logic '0', Low Input Voltage	V_{IL}	—	1.3	0.8	V	
Input Current	I_{IN}	-10	—	+10	µA	0V ≤ V_{IN} ≤ V_{DD}
Output						
High Output Voltage	V_{OH}	V_{DD} – 0.025	—	—	V	DC TEST
Low Output Voltage	V_{OL}	—	—	0.025	V	DC TEST
Output Resistance, High	R_{OH}	—	1.4	—	Ω	I_{OUT} = 10 mA, V_{DD} = 18V
Output Resistance, Low	R_{OL}	—	0.9	1.7	Ω	I_{OUT} = 10 mA, V_{DD} = 18V
Peak Output Current	I_{PK}	—	9.0	—	A	V_{DD} = 18V
Latch-Up Protection Withstand Reverse Current	I_{REV}	—	>1.5	—	A	Duty cycle ≤ 2%, t ≤ 300 µsec
Switching Time (Note 1)						
Rise Time	t_R	—	60	75	ns	**Figure 4-1**, C_L = 10,000 pF
Fall Time	t_F	—	60	75	ns	**Figure 4-1**, C_L = 10,000 pF
Delay Time	t_{D1}	—	30	60	ns	**Figure 4-1**
Delay Time	t_{D2}	—	33	60	ns	**Figure 4-1**
Power Supply						
Power Supply Current	I_S	— —	0.2 55	1.5 150	mA µA	V_{IN} = 3V V_{IN} = 0V
Operating Input Voltage	V_{DD}	4.5	—	18	V	

Note 1: Switching times ensured by design.

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DC CHARACTERISTICS (OVER OPERATING TEMPERATURE RANGE)

Electrical Specifications: Unless otherwise noted, over operating temperature range with 4.5V ≤ V_{DD} ≤ 18V.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Input						
Logic '1', High Input Voltage	V_{IH}	2.4	—	—	V	
Logic '0', Low Input Voltage	V_{IL}	—	—	0.8	V	
Input Current	I_{IN}	-10	—	+10	µA	0V ≤ V_{IN} ≤ V_{DD}
Output						
High Output Voltage	V_{OH}	V_{DD} – 0.025	—	—	V	DC TEST
Low Output Voltage	V_{OL}	—	—	0.025	V	DC TEST
Output Resistance, High	R_{OH}	—	2.4	3.6	Ω	I_{OUT} = 10 mA, V_{DD} = 18V
Output Resistance, Low	R_{OL}	—	1.8	2.7	Ω	I_{OUT} = 10 mA, V_{DD} = 18V
Switching Time (Note 1)						
Rise Time	t_R	—	60	120	ns	**Figure 4-1**, C_L = 10,000 pF
Fall Time	t_F	—	60	120	ns	**Figure 4-1**, C_L = 10,000 pF
Delay Time	t_{D1}	—	50	80	ns	**Figure 4-1**
Delay Time	t_{D2}	—	65	80	ns	**Figure 4-1**
Power Supply						
Power Supply Current	I_S	— —	— —	3 0.2	mA	V_{IN} = 3V V_{IN} = 0V
Operating Input Voltage	V_{DD}	4.5	—	18	V	

Note 1: Switching times ensured by design.

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, all parameters apply with 4.5V ≤ V_{DD} ≤ 18V.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range (M)	T_A	-55	—	+125	°C	
Maximum Junction Temperature	T_J	—	—	+150	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Package Thermal Resistances						
Thermal Resistance, 8L-CERDIP	θ_{JA}	—	150	—	°C/W	

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2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C with 4.5V ≤ V_{DD} ≤ 18V.

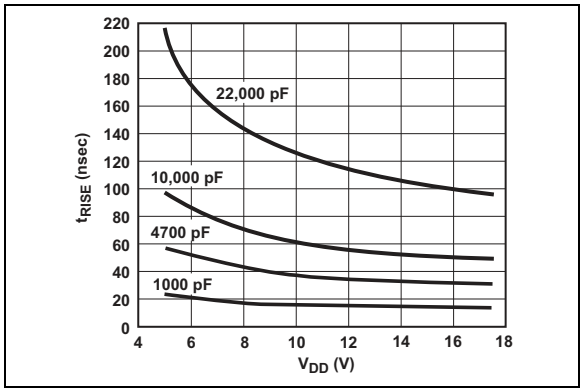

FIGURE 2-1: *Rise Time vs. Supply Voltage.*

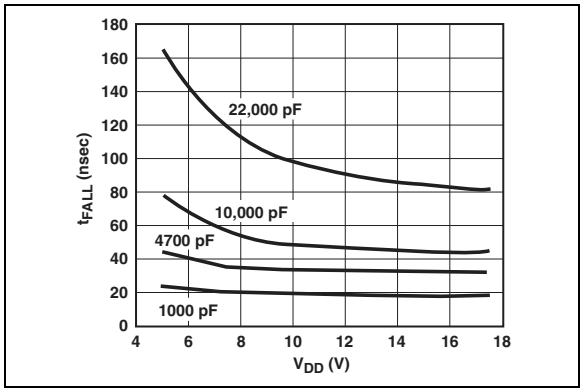

FIGURE 2-4: *Fall Time vs. Supply Voltage.*

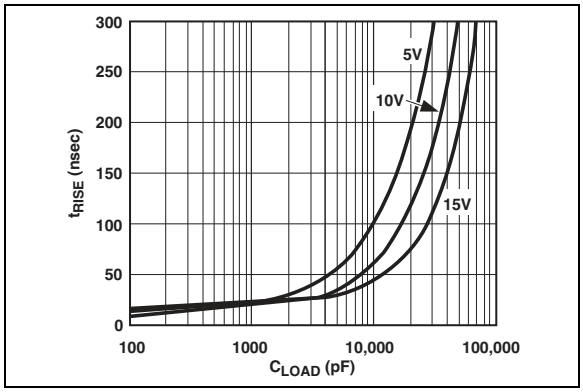

FIGURE 2-2: *Rise Time vs. Capacitive Load.*

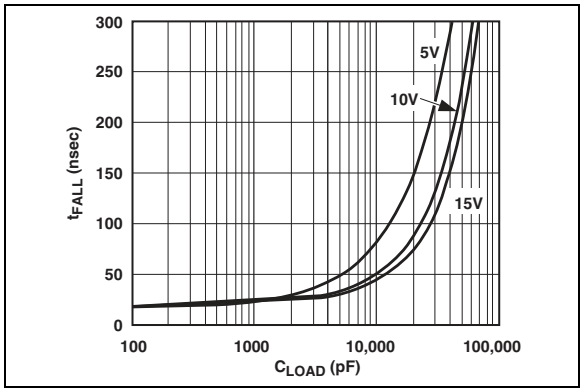

FIGURE 2-5: *Fall Time vs. Capacitive Load.*

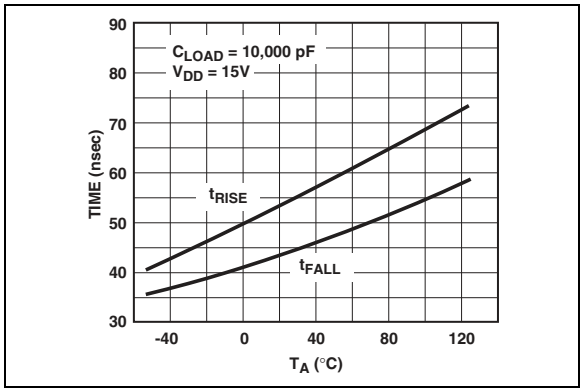

FIGURE 2-3: *Rise and Fall Times vs. Temperature.*

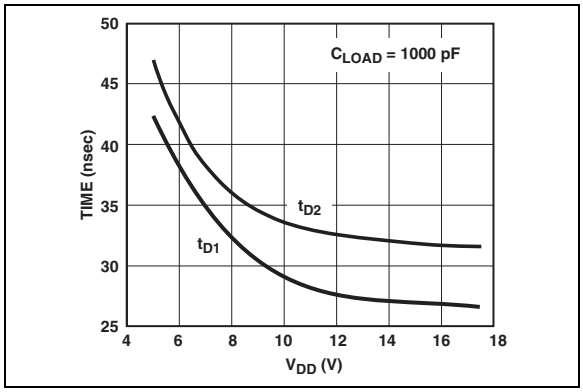

FIGURE 2-6: *Propagation Delay vs. Supply Voltage.*

Note: Unless otherwise indicated, T_A = +25°C with 4.5V ≤ V_{DD} ≤ 18V.

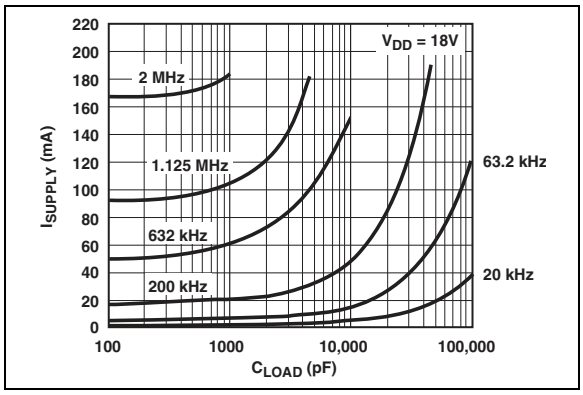

FIGURE 2-7: *Supply Current vs. Capacitive Load (V_{DD} = 18V).*

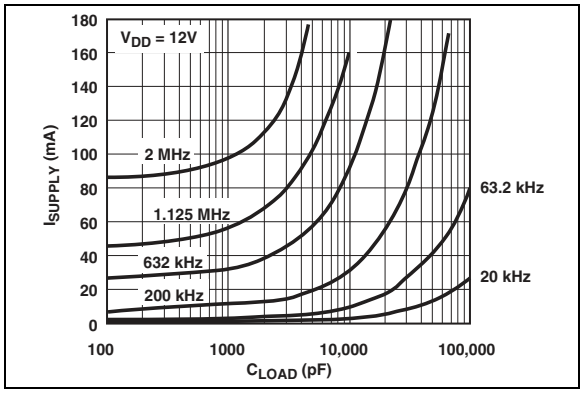

FIGURE 2-8: *Supply Current vs. Capacitive Load (V_{DD} = 12V).*

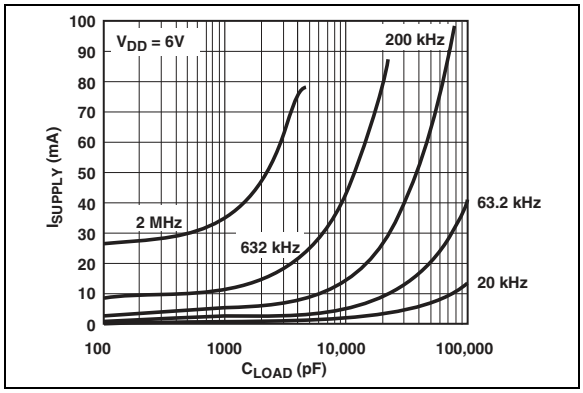

FIGURE 2-9: *Supply Current vs. Capactive Load (V_{DD} = 6V).*

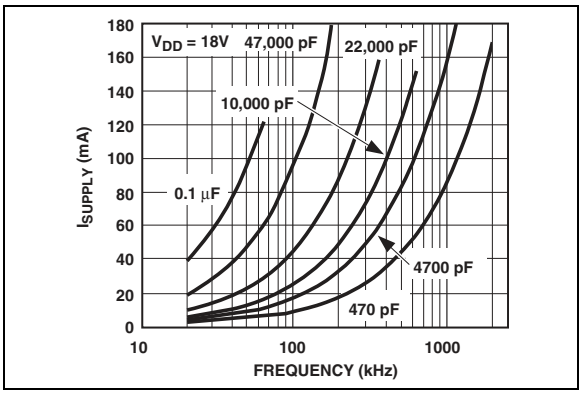

FIGURE 2-10: *Supply Current vs. Frequency (V_{DD} = 18V).*

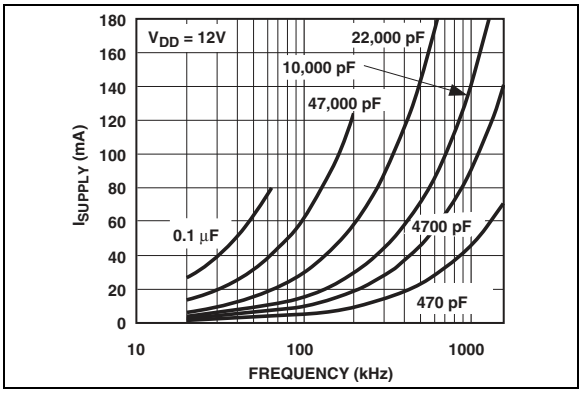

FIGURE 2-11: *Supply Current vs. Frequency (V_{DD} = 12V).*

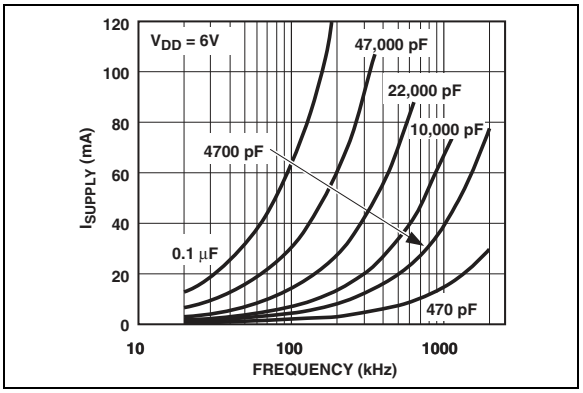

FIGURE 2-12: *Supply Current vs. Frequency (V_{DD} = 6V).*

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Note: Unless otherwise indicated, T_A = +25°C with 4.5V ≤ V_{DD} ≤ 18V.

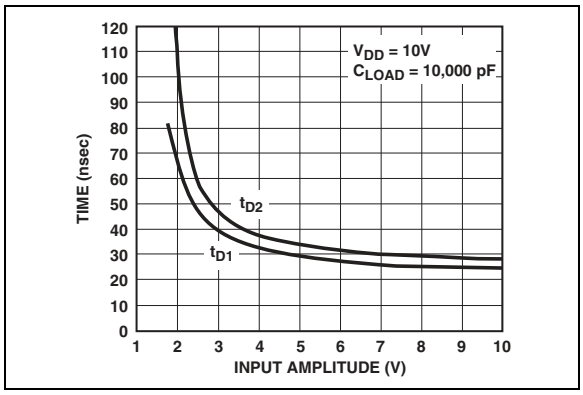

FIGURE 2-13: *Propagation Delay vs. Input Amplitude.*

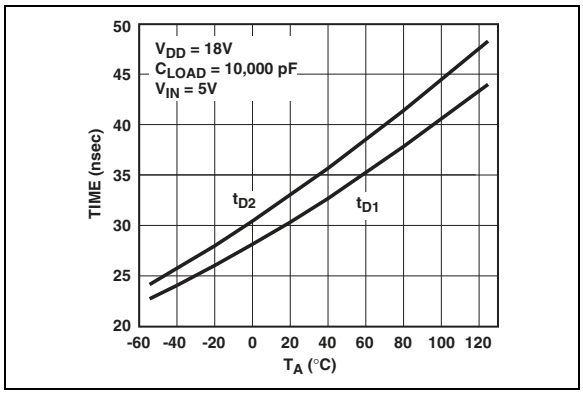

FIGURE 2-16: *Propagation Delay vs. Temperature.*

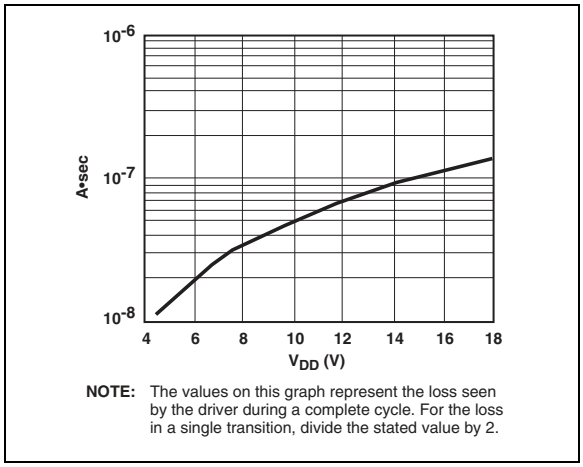

FIGURE 2-14: *Crossover Energy vs. Supply Voltage.*

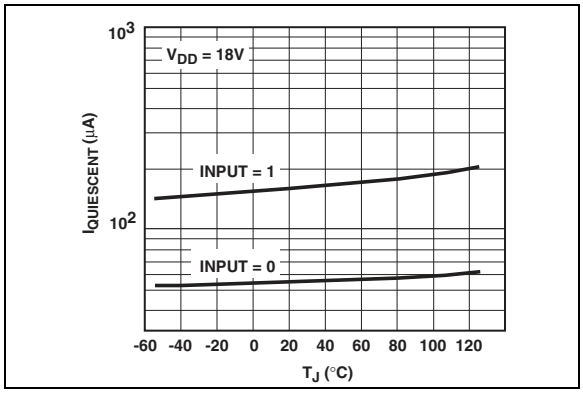

FIGURE 2-17: *Quiescent Supply Current vs. Temperature.*

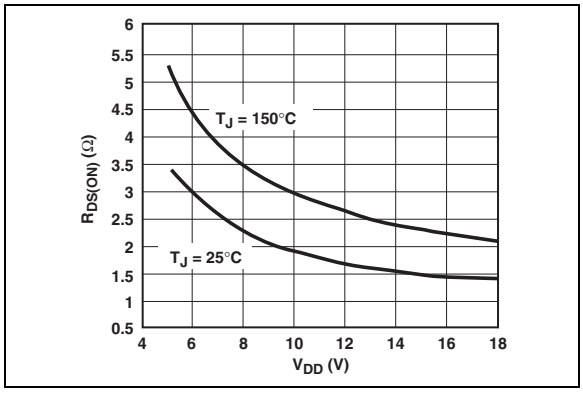

FIGURE 2-15: *High-State Output Resistance vs. Supply Voltage.*

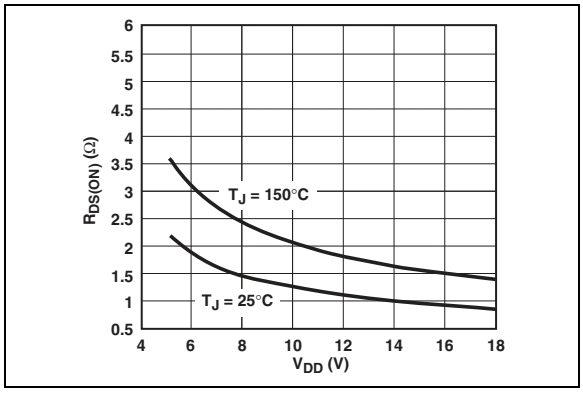

FIGURE 2-18: *Low-State Output Resistance vs. Supply Voltage.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin No. 8-Pin CERDIP	Symbol	Description
1	V_{DD}	Supply input, 4.5V to 18V
2	INPUT	Control input, TTL/CMOS-compatible input
3	NC	No connection
4	GND	Ground
5	GND	Ground
6	OUTPUT	CMOS push-pull output
7	OUTPUT	CMOS push-pull output
8	V_{DD}	Supply input, 4.5V to 18V

3.1 Supply Input (V_{DD})

The V_{DD} input is the bias supply for the MOSFET driver and is rated for 4.5V to 18V with respect to the ground pin. The V_{DD} input should be bypassed to ground with a local ceramic capacitor. The value of the capacitor should be chosen based on the capacitive load that is being driven. A minimum value of 1.0 µF is suggested.

3.2 Control Input

The MOSFET driver input is a high-impedance, TTL/CMOS-compatible input. The input also has 300 mV of hysteresis between the high and low thresholds that prevents output glitching even when the rise and fall time of the input signal is very slow.

3.3 CMOS Push-Pull Output

The MOSFET driver output is a low-impedance, CMOS, push-pull style output capable of driving a capacitive load with 9.0A peak currents. The MOSFET driver output is capable of withstanding 1.5A peak reverse currents of either polarity.

3.4 Ground

The ground pins are the return path for the bias current and for the high peak currents that discharge the load capacitor. The ground pins should be tied into a ground plane or have very short traces to the bias supply source return.

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4.0 APPLICATIONS INFORMATION

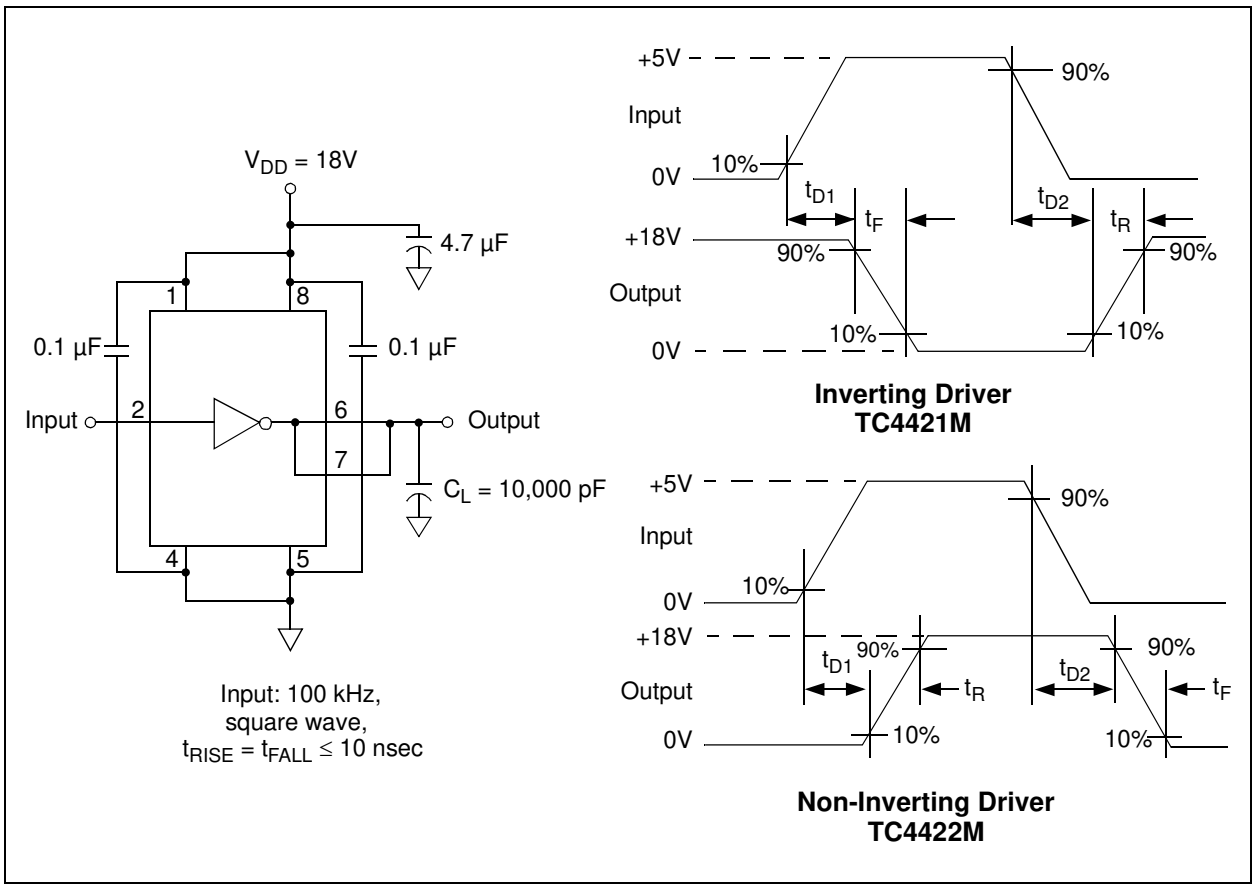
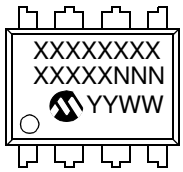


FIGURE 4-1: *Switching Time Test Circuits.*

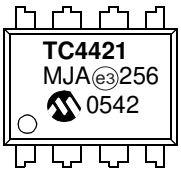
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

8-Lead CERDIP (300 mil)



Example:



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

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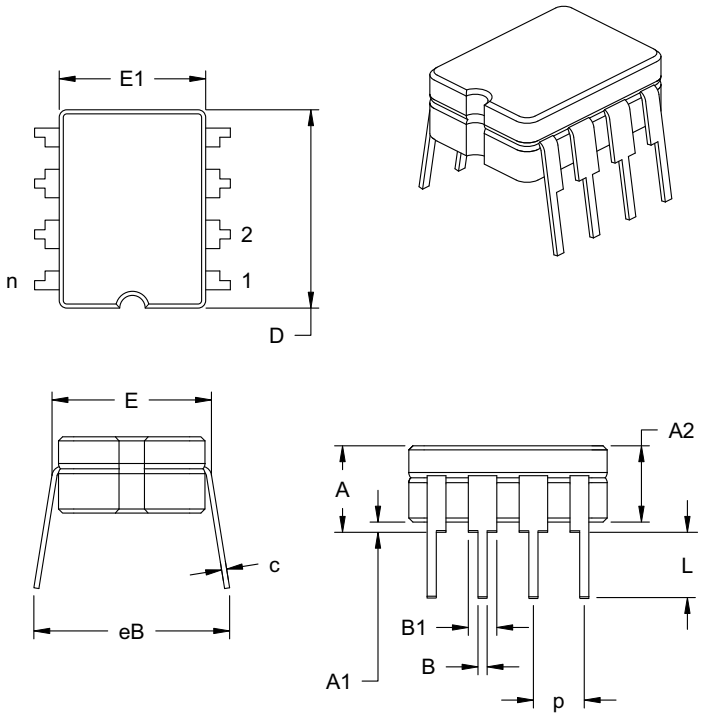
8-Lead Ceramic Dual In-line – 300 mil (CERDIP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.160	.180	.200	4.06	4.57	5.08
Standoff §	A1	.020	.030	.040	0.51	0.77	1.02
Shoulder to Shoulder Width	E	.290	.305	.320	7.37	7.75	8.13
Ceramic Pkg. Width	E1	.230	.265	.300	5.84	6.73	7.62
Overall Length	D	.370	.385	.400	9.40	9.78	10.16
Tip to Seating Plane	L	.125	.163	.200	3.18	4.13	5.08
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.055	.065	1.14	1.40	1.65
Lower Lead Width	B	.016	.018	.020	0.41	0.46	0.51
Overall Row Spacing	eB	.320	.360	.400	8.13	9.15	10.16

*Controlling Parameter

JEDEC Equivalent: MS-030

Drawing No. C04-010

NOTES:

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APPENDIX A: REVISION HISTORY

Revision A (February 2005)

- Original Release of this Document.

Revision B (January 2013)

Added a note to each package outline drawing.

NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	XX
Device and Temperature Range	Package

Device and Temperature Range:	TC4421M: 9A High-Speed MOSFET Driver, Inverting, -55°C to +125°C TC4422M: 9A High-Speed MOSFET Driver, Non-Inverting, -55°C to +125°C
Package:	JA = Ceramic Dual In-Line (300 mil Body), 8-lead

Examples:

a) TC4421MJA: 9A High-Speed MOSFET Driver, Inverting, 8LD CERDIP package.

a) TC4422MJA: 9A High-Speed MOSFET Driver, Non-Inverting, 8LD CERDIP package.

NOTES:

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