High-performance Regulator IC Series for PCs

Termination Regulators for DDR-SDRAMs

BD3533F/FVM/EKN(1A),BD3531F(1.5A),BD3532F/EFV/KN(3A)

●Description

BD3533/31/32 is a termination regulator compatible with JEDEC DDR-SDRAM, which functions as a linear power supply incorporating an N-channel MOSFET and provides a sink/source current capability up to 1A, 1.5A, and 3A respectively. A built-in high-speed OP-AMP specially designed offers an excellent transient response. Requires 3.3 volts or 5.0 volts as a bias power supply to drive the N-channel MOSFET. Has an independent reference voltage input pin (VDDQ) and an independent feedback pin (VTTS) to maintain the accuracy in voltage required by JEDEC, and offers an excellent output voltage accuracy and load regulation. Also has a reference power supply output pin (VREF) for DDR-SDRAM or a memory controller. When EN pin turns to “Low”, VTT output becomes “Hi-Z” while VREF output is kept unchanged, compatible with “Self Refresh” state of DDR-SDRAM.

●Features

1) Incorporates a push-pull power supply for termination (VTT)
2) Incorporates a reference voltage circuit (VREF)
3) Incorporates an enabler
4) Incorporates an undervoltage lockout (UVLO)
5). Employs SOP8 package
6) Employs MSOP8 package
7) Employs HQFN20V package
8) Employs HTSSOP-B20 package
9) Employs VQFN28V package
10) Incorporates a thermal shutdown protector (TSD)
11) Operates with input voltage from 2.7 to 5.5 volts
12) Compatible with Dual Channel (DDR-II)

●Use

Power supply for DDR I/II - SDRAM

●Line up

Parameter	BD3533F/FVM/EKN	BD3531F	BD3532F/EFV/KN
Output Current	±1.0A	±1.5A	±3A
Vcc Range	2.7V～5.5V	4.5V～5.5V	4.3～5.5V
Soft Start Function	○	×	○
Temperature	-20～100℃	-10～100℃	-40～100℃
Package	SOP8/MSOP8/HQFN20V	SOP8	SOP8/HTSSOP-B20/VQFN28

Oct. 2008

●ABSOLUTE MAXIMUM RATINGS

◎BD3533F/FVM/EKN

Parameter	Symbol	BD3533F	BD3533FVM	BD3533EKN	Unit
Input Voltage	VCC	7 *1*2	7 *1*2	7 *1*2	V
Enable Input Voltage	VEN	7 *1*2	7 *1*2	7 *1*2	V
Termination Input Voltage	VTT_IN	7 *1*2	7 *1*2	7 *1*2	V
VDDQ Reference Voltage	VDDQ	7 *1*2	7 *1*2	7 *1*2	V
Output Current	ITT	3	1	3	A
Power Dissipation1	Pd1	560 *3	437.5 *5	500 *6	mW
Power Dissipation2	Pd2	690 *4	-	750 *7	mW
Power Dissipation3	Pd3	-	-	1750 *8	mW
Power Dissipation4	Pd4	-	-	2000 *9	mW
Operating Temperature Range	Topr	-20～+100	-20～+100	-20～+100	℃
Storage Temperature Range	Tstg	-55～+150	-55～+150	-55～+150	℃
Maximum Junction Temperature	Tjmax	+150	+150	+150	℃

*1 Should not exceed Pd.
*2 Instantaneous surge voltage, back electromotive force and voltage under less than 10% duty cycle.
*3 Reduced by 4.48mW for each increase in Ta of 1℃ over 25℃(With no heat sink).
*4 Reduced by 5.52mW for each increase in Ta of 1℃ over 25℃(When mounted on a board 70mm×70mm×1.6mm Glass-epoxyPCB).
*5 Reduced by 3.5mW for each increase in Ta of 1℃ over 25℃(With no heat sink).
*6 Ta≧25℃(no heat sink)4mW/℃ increase.
*7 Ta≧25℃(when mounted on 70mm x 70mm x 1.6mm Glass-epoxy PCB which does not have copper on the back side).
*8 Ta≧25℃(when mounted on 70mm x 70mm x 1.6mm Glass-epoxy PCB which has 1 layer (60mm x 60mm) of copper on the back side)14mW/℃ increase.
*9 Ta≧25℃(When mounted on board 70mm x 70mm x 1.6mm Glass-epoxy PCB which has 2 layers (60mm x 60mm) of copper on the back side)16mW/℃ increase.

◎BD3531F

Parameter	Symbol	Limit	Unit
Input Voltage	VCC	7 *1	V
EN Input Voltage	VEN	7 *1	V
Termination Input Voltage	VTT_IN	7 *1	V
VDDQ Reference Voltage	VDDQ	7 *1	V
Output Current	ITT	3	A
Power Dissipation1	Pd1	560 *2	mW
Power Dissipation2	Pd2	690 *3	mW
Operating Temperature Range	Topr	-10～	℃
Storage Temperature Range	Tstg	-55～	℃
Maximum Junction Temperature	Tjmax	+150	℃

*1 Should not exceed Pd.
*2 Reduced by 4.48mW for each increase in Ta of 1℃ over 25℃(With no heat sink).
*3 Reduced by 5.52mW for each increase in Ta of 1℃ over 25℃(When mounted on a board 70mm×70mm×1.6mm Glass-epoxyPCB).

◎BD3532F/EFV/KN

Parameter	Symbol	BD3532F	BD3532EFV	BD3532KN	Unit
Input Voltage	VCC	7 *1	7 *1	7 *1	V
Enable Input Voltage	VEN	7 *1	7 *1	7 *1	V
Termination Input Voltage	VTT_IN	7 *1	7 *1	7 *1	V
VDDQ Reference Voltage	VDDQ	7 *1	7 *1	7 *1	V
Output Current	ITT	3	3	3	A
Power Dissipation1	Pd1	560 *2	-	460 *5	mW
Power Dissipation2	Pd2	690 *3	1000 *4	725 *6	mW
Operating Temperature Range	Topr	-40～+100	-40～+100	-40～+100	℃
Storage Temperature Range	Tstg	-55～+150	-55～+150	-55～+150	℃
Maximum Junction Temperature	Tjmax	+150	+150	+150	℃

*1 Should not exceed Pd.
*2 Reduced by 4.48mW for each increase in Ta of 1℃ over 25℃(With no heat sink).
*3 Reduced by 5.52mW for each increase in Ta of 1℃ over 25℃(When mounted on a board 70mm×70mm×1.6mm Glass-epoxyPCB).
*4 Reduced by 8.0mW for each increase in Ta of 1℃ over 25℃(When mounted on a board 70mm×70mm×1.6mm Glass-epoxyPCB).
*5 Reduced by 3.68mW for each increase in Ta of 1℃ over 25℃(With no heat sink).
*6 Reduced by 5.80mW for each increase in Ta of 1℃ over 25℃(When mounted on a board 70mm×70mm×1.6mm Glass-epoxyPCB).

●RECOMMENDED OPERATING CONDITIONS

◎BD3533F/FVM/EKN(Ta=25℃)

Parameter	Symbol	MIN	MAX	Unit
Input Voltage	VCC	2.7	5.5	V
Termination Input Voltage	VTT_IN	1.0	5.5	V
VDDQ Reference Voltage	VDDQ	1.0	2.75	V
Enable Input Voltage	VEN	-0.3	5.5	V

◎BD3531F(Ta=25℃)

Parameter	Symbol	MIN	MAX	Unit
Input Voltage	VCC	4.5	5.5	V
Termination Input Voltage	VTT_IN	1.0	5.5	V
EN Input Voltage	VEN	-0.3	5.5	V

◎BD3532F/EFV/KN(Ta=25℃)

Parameter	Symbol	MIN	MAX	Unit
Input Voltage	VCC	4.3	5.5	V
Termination Input Voltage	VTT_IN	1.0	5.5	V
EN Input Voltage	VEN	-0.3	5.5	V

★ No radiation-resistant design is adopted for the present product.

●ELECTRICAL CHARACTERISTICS

◎BD3533F/FVM/EKN

ELECTRICAL CHARACTERISTICS(unless otherwise noted, Ta=25℃ VCC=3.3V VEN=3V VDDQ=1.8V VTT_IN=1.8V)

Parameter	Symbol	Standard Value			Unit	Condition
		MIN	TYP	MAX		
Standby Current	IST	-	0.8	1.6	mA	VEN=0V
Bias Current	ICC	-	2	4	mA	VEN=3V
[Enable]						
High Level Enable Input Voltage	VENHIGH	2.3	-	5.5	V	
Low Level Enable Input Voltage	VENLOW	-0.3	-	0.8	V	
Enable Pin Input Current	IEN	-	7	10	uA	VEN=3V
[Termination]						
Termination Output Voltage 1	VTT1	VREF -30m	VREF	VREF +30m	V	ITT=-1.0A to 1.0A Ta=0℃ to 100℃ *7
Termination Output Voltage 2	VTT2	VREF -30m	VREF	VREF +30m	V	VCC=5V, VDDQ=2.5V VTT_IN=2.5V ITT=-1.0A to 1.0A Ta=0℃ to 100℃ *7
Source Current	ITT+	1.0	-	-	A	
Sink Current	ITT-	-	-	-1.0	A	
Load Regulation	⊿VTT	-	-	50	mV	ITT=-1.0A to 1.0A
Line Regulation	Reg.l	-	20	40	mV	
Upper Side ON Resistance 1	HRON1	-	0.45	0.9	Ω	
Lower Side ON Resistance 1	LRON1	-	0.45	0.9	Ω	
Upper Side ON Resistance 2	HRON2	-	0.4	0.8	Ω	VCC=5V, VDDQ=2.5V VTT_IN=2.5V
Lower Side ON Resistance 2	LRON2	-	0.4	0.8	Ω	VCC=5V, VDDQ=2.5V VTT_IN=2.5V

*7 Design Guarantee

●ELECTRICAL CHARACTERISTICS

◎BD3533F/FVM/EKN

ELECTRICAL CHARACTERISTICS(unless otherwise noted, Ta=25℃ VCC=3.3V VEN=3V VDDQ=1.8V VTT_IN=1.8V)

Parameter	Symbol	Standard Value			Unit	Condition
		MIN	TYP	MAX		
[Input of Reference Voltage]						
Input Impedance	ZVDDQ	70	100	130	kΩ	
Output Voltage1	VREF1	1/2×VDDQ -18m	1/2×VDDQ	1/2×VDDQ +18m	V	IREF=-5mA to 5mA Ta=0℃ to 100℃*7
Output Voltage2	VREF2	1/2×VDDQ -40m	1/2×VDDQ	1/2×VDDQ +40m	V	IREF=-10mA to 10mA Ta=0℃ to 100℃*7
Output Voltage3	VREF3	1/2×VDDQ -25m	1/2×VDDQ	1/2×VDDQ +25m	V	VCC=5V, VDDQ=VTT_IN=2.5V IREF=-5mA to 5mA Ta=0℃ to 100℃*7
Output Voltage4	VREF4	1/2×VDDQ -40m	1/2×VDDQ	1/2×VDDQ +40m	V	VCC=5V, VDDQ=VTT_IN=2.5V IREF=-10mA to 10mA Ta=0℃ to 100℃*7
[Reference voltage]						
Source Current	IREF+	20	-	-	mA	
Sink Current	IREF-	-	-	-20	mA	
[UVLO]						
UVLO OFF Voltage	VUVLO	2.40	2.55	2.70	V	VCC : sweep up
Hysteresis Voltage	⊿VUVLO	100	160	220	mV	VCC : sweep down

*7 Design Guarantee

◎BD3531F

ELECTRICAL CHARACTERISTICS(unless otherwise noted, Ta=25℃ VCC=5V VEN=3V VDDQ=2.5V VTT_IN=2.5V)

Parameter	Symbol	Standard Value			Unit	Condition
		MIN	TYP	MAX		
Standby Current	IST	-	0.8	1.6	mA	VEN=0V
Bias Current	ICC	-	2	4	mA	
[Enable]						
Hi Level Enable Input Voltage	VENHI	2	-	5.5	V	
Low Level Enable Input Voltage	VENLOW	-0.3	-	0.8	V	
Enable Pin Input Current	IEN	-	7	10	uA	VEN=3V
[Termination]						
Termination Output Voltage	VTT	VREF -30mV	VREF	VREF +30mV	V	Io=-1.5A to 1.5A Ta=0℃ to 100℃ *8
Source Current	ITT+	1.5	-	-	A	
Sink Current	ITT-	-	-	-1.5	A	
Load Regulation	⊿VTT	-	-	40	mV	Io=-1.5A to 1.5A
Line Regulation	Reg.l	-	20	40	mV	VCC=4.5V to 5.5V
Upper Side ON Resistance	HRON	-	0.4	0.8	Ω	
Lower Side ON Resistance	LRON	-	0.4	0.8	Ω	
[Input of Reference Voltage]						
Input Impedance	ZVDDQ	-	100	-	kΩ	
[Reference voltage]						
Output Voltage1	VREF1	1/2×VDDQ-30m	1/2×VDDQ	1/2×VDDQ+30m	V	IREF=0mA
Output Voltage2	VREF2	1/2×VDDQ -40m	1/2×VDDQ	1/2×VDDQ +40m	V	IREF=-10mA to 10mA Ta=0℃ to 100℃ *8
Source Current	IREF+	10	20	-	mA	
Sink Current	IREF-	-	-20	-10	mA	
[UVLO]						
UVLO OFF Voltage	VUVLO	4.2	4.35	4.5	V	VCC : Sweep up
Hysteresis Voltage	⊿VUVLO	100	160	220	mV	VCC : Sweep down

*8 Design Guarantee

◎BD3532F/EFV/KN

ELECTRICAL CHARACTERISTICS(unless otherwise noted, Ta=25℃ VCC=5V VEN=3V VDDQ=2.5V VTT_IN=2.5V)

Parameter	Symbol	Standard Value			Unit	Condition
		MIN	TYP	MAX		
Standby Current	IST	-	0.8	1.6	mA	VEN=0V
Bias Current	ICC	-	2	4	mA	
[Enable]						
Hi Level Enable Input Voltage	VENHI	2.3	-	5.5	V	VCC=4.3V to 5.5V Ta=0℃ to 100℃ *9
Low Level Enable Input Voltage	VENLOW	-0.3	-	0.8	V	VCC=4.3V to 5.5V Ta=0℃ to 100℃ *9
Enable Pin Input Current	IEN	-	7	10	uA	VEN=3V
[Termination]						
Termination Output Voltage	VTT	VREF -30mV	VREF	VREF +30mV	V	Io=-3A to 3A Ta=0℃ to 100℃ *9
Source Current	ITT+	3	-	-	A	
Sink Current	ITT-	-	-	-3	A	
Load Regulation	⊿VTT	-	-	40	mV	Io=-3A to 3A
Line Regulation	Reg.I	-	20	40	mV	VCC=4.3V to 5.5V
Upper Side ON Resistance	HRON	-	0.2	0.4	Ω	
Lower Side ON Resistance	LRON	-	0.2	0.4	Ω	
[Input of Reference Voltage]						
Input Impedance	ZVDDQ	70	100	130	kΩ	
Output Voltage1	VREF1	1/2×VDDQ -30mV	1/2×VDDQ	1/2×VDDQ +30mV	V	IREF=0mA
Output Voltage2	VREF2	1/2×VDDQ -40mV	1/2×VDDQ	1/2×VDDQ +40mV	V	IREF=-10mA to 10mA Ta=0℃ to 100℃ *9
Output Voltage1'	VREF1'	1/2×VDDQ -30mV	1/2×VDDQ	1/2×VDDQ +30mV	V	VDDQ=VTT_IN1=VTT_IN2=1.8V IREF=0mA
Output Voltage2'	VREF2'	1/2×VDDQ -40mV	1/2×VDDQ	1/2×VDDQ +40mV	V	VDDQ=VTT_IN1=VTT_IN2=1.8V IREF=-10mA to 10mA Ta=0℃ to 100℃ *9
Source Current1	IREF1+	20	-	-	mA	
Sink Current1	IREF1-	-	-	-20	mA	
Source Current2	IREF2+	20	-	-	mA	VDDQ=VTT_IN1=VTT_IN2=1.8V
Sink Current2	IREF2-	-	-	-20	mA	VDDQ=VTT_IN1=VTT_IN2=1.8V
[UVLO]						
UVLO OFF Voltage	VUVLO	4.0	4.15	4.3	V	VCC : sweep up
Hysteresis Voltage	⊿VUVLO	100	160	220	mV	VCC : sweep down

*9 Design Guarantee

●Reference Data

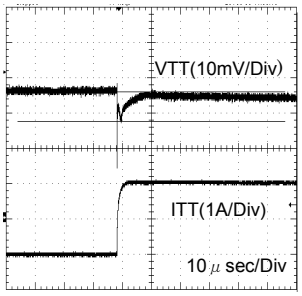


Fig.1 DDR Ⅰ(-1A→1A) BD3531

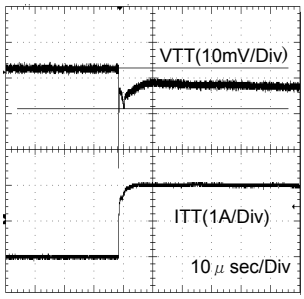


Fig.2 DDR Ⅰ(-1A→1A) BD3532

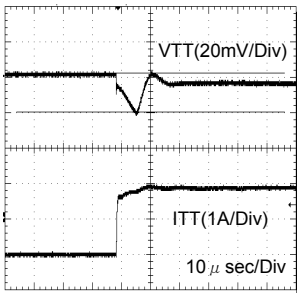


Fig.3 DDR Ⅰ(-1A→1A) BD3533

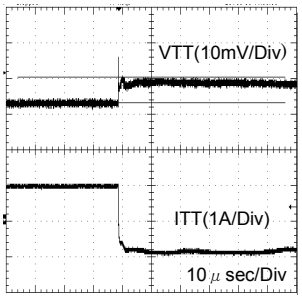


Fig.4 DDR Ⅰ(1A→-1A) BD3531

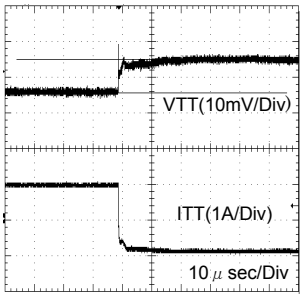


Fig.5 DDR Ⅰ(1A→-1A) BD3532

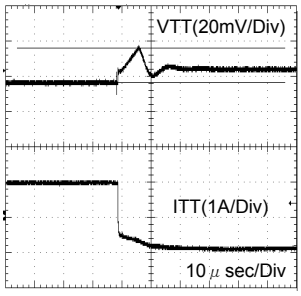


Fig.6 DDR Ⅰ(1A→-1A) BD3533

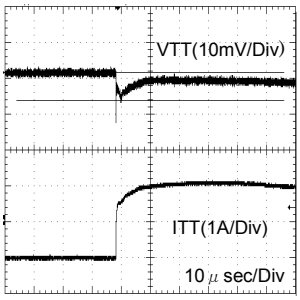


Fig.7 DDRⅡ(-1A→1A) BD3531

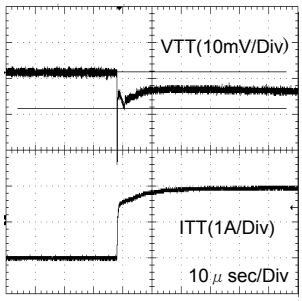


Fig.8 DDRⅡ(-1A→1A) BD3532

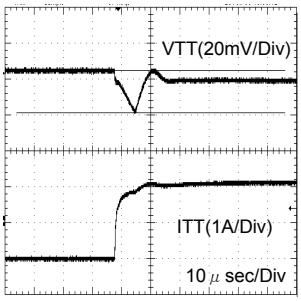


Fig.9 DDRⅡ(-1A→1A) BD3533

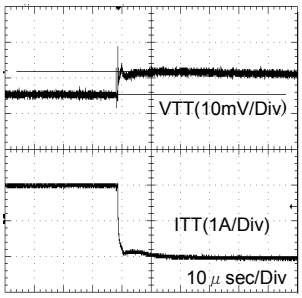


Fig.10 DDRⅡ(1A→-1A) BD3531

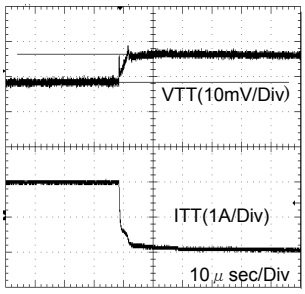


Fig.11 DDRⅡ(1A→-1A) BD3532

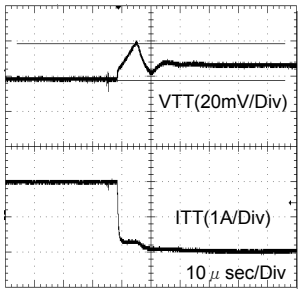


Fig.12 DDRⅡ(1A→-1A) BD3533

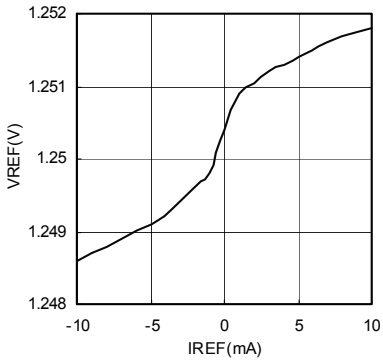


Fig.13 IREF-VREF (DDR-Ⅰ)

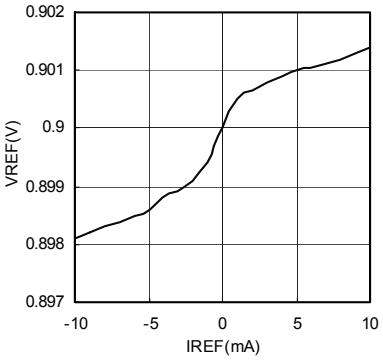


Fig.14 IREF-VREF (DDR-Ⅱ)

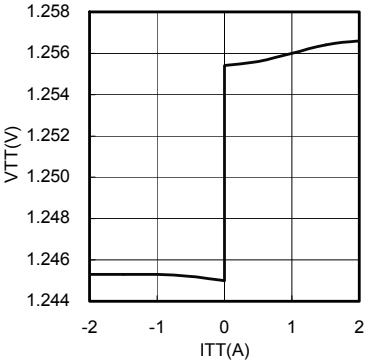


Fig.15 ITT-VTT (DDR-Ⅰ)

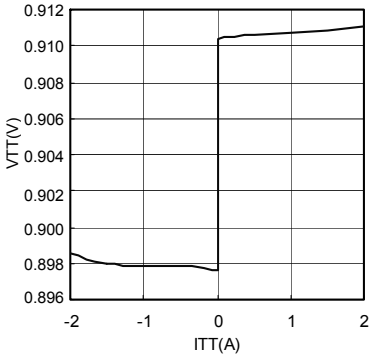


Fig.16 ITT-VTT (DDR-Ⅱ)

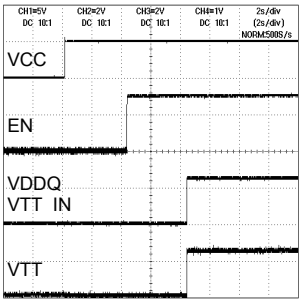


Fig.17 Input Sequence 1

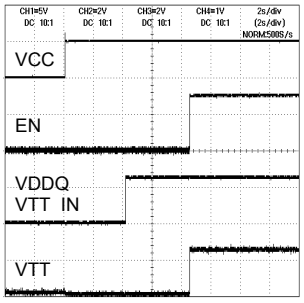


Fig.18 Input Sequence 2

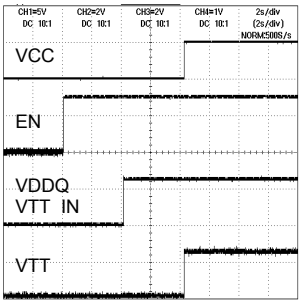


Fig.19 Input Sequence 3

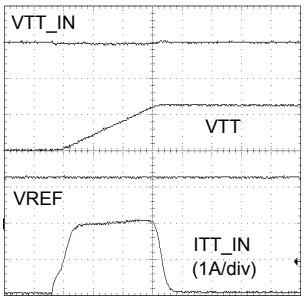
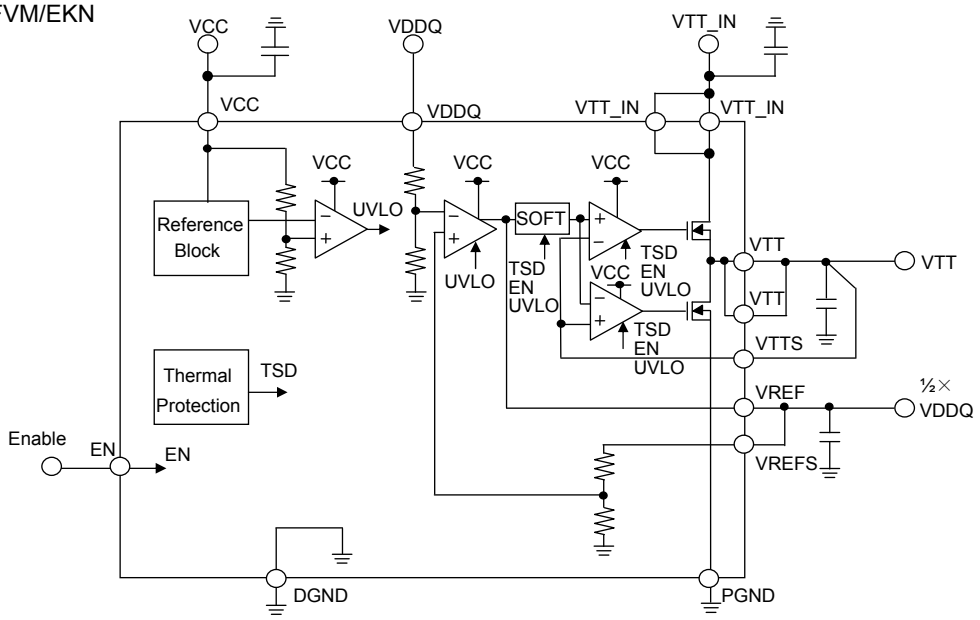


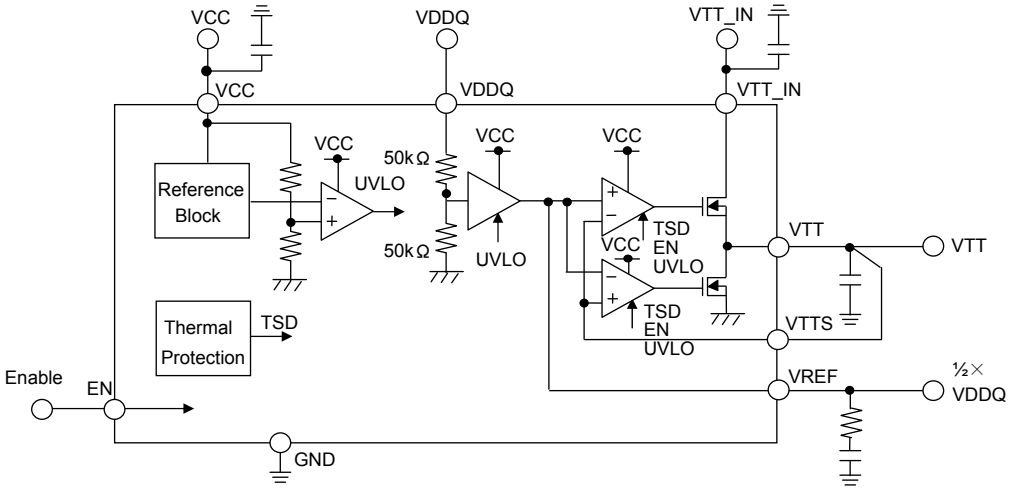
Fig.20 Start up Wave Form

●BLOCK DIAGRAM

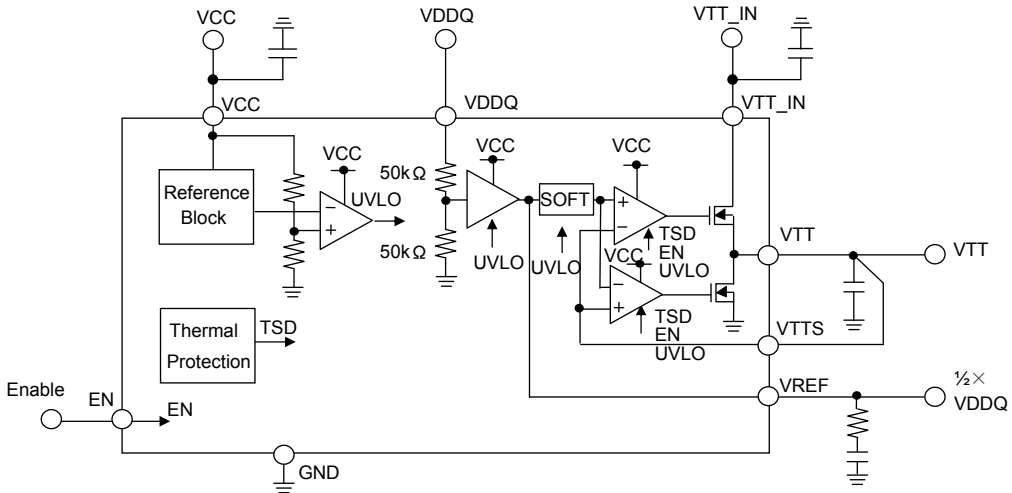
◎BD3533F/FVM/EKN



◎BD3531F

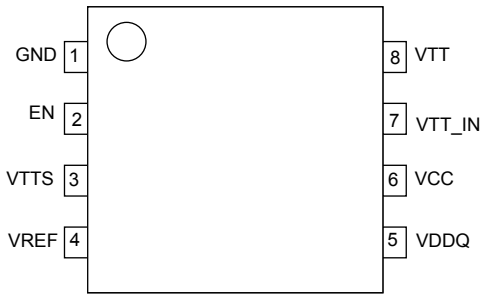


◎BD3532F/FVM/EKN



◎BD3533F/BD3533FVM/BD3531F/BD3532F

●PIN CONFIGRATION

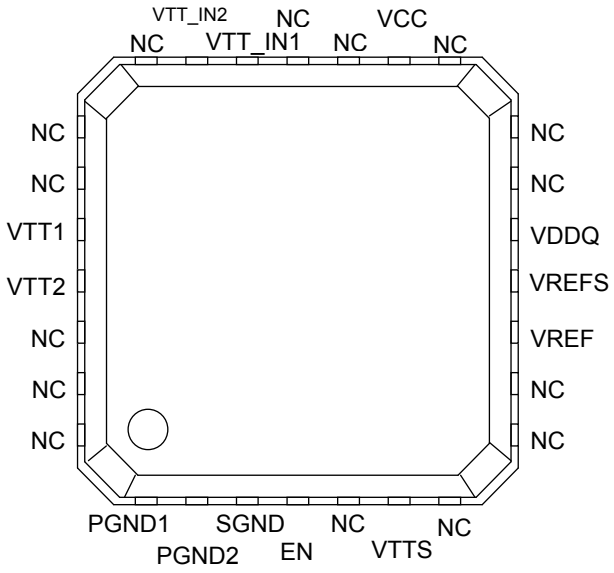


●PIN FUNCTION

PIN No.	PIN NAME	PIN FUNCTION
1	GND	GND Pin
2	EN	Enable Input Pin
3	VTTS	Detector Pin for Termination Voltage
4	VREF	Reference Voltage Output Pin
5	VDDQ	Reference Voltage Input Pin
6	VCC	VCC Pin
7	VTT_IN	Termination Input Pin
8	VTT	Termination Output Pin

◎BD3532KN

●PIN CONFIGRATION

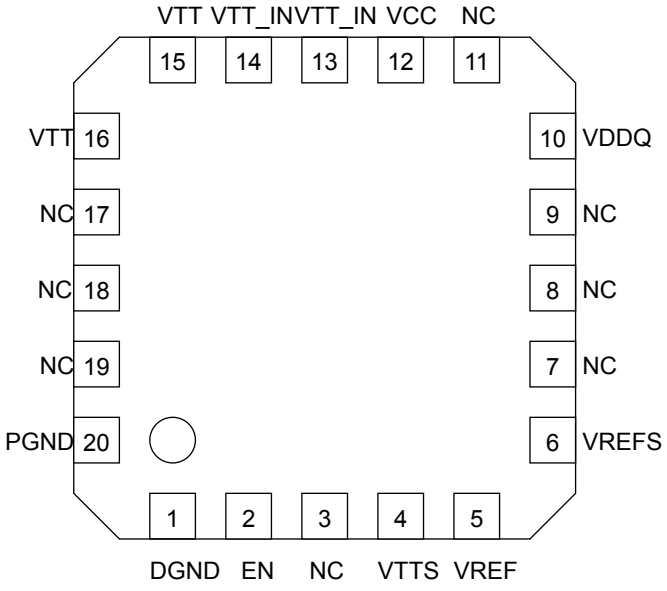


●PIN FUNCTION

PIN No.	PIN NAME	PIN FUNCTION
1	PGND1	Power Ground Pin 1
2	PGND2	Power Ground Pin 2
3	SGND	Ground Pin for Reference Voltage
4	EN	Enable Input Pin
5	N.C.	Non Connection
6	VTTS	Detector Pin for Termination Voltage
7	N.C.	Non Connection
8	N.C.	Non Connection
9	N.C.	Non Connection
10	VREF	Reference Voltage Output Pin
11	VREFS	Detector Pin for Reference Voltage
12	VDDQ	Reference Voltage Input Pin
13	N.C.	Non Connection
14	N.C.	Non Connection
15	N.C.	Non Connection
16	VCC	VCC Pin
17	N.C.	Non Connection
18	N.C.	Non Connection
19	VTT_IN1	Termination Input Pin 1
20	VTT_IN2	Termination Input Pin 2
21	N.C.	Non Connection
22	N.C.	Non Connection
23	N.C.	Non Connection
24	VTT1	Termination Output Pin 1
25	VTT2	Termination Output Pin 2
26	N.C.	Non Connection
27	N.C.	Non Connection
28	N.C.	Non Connection

◎BD3533EKN

●PIN CONFIGRATION

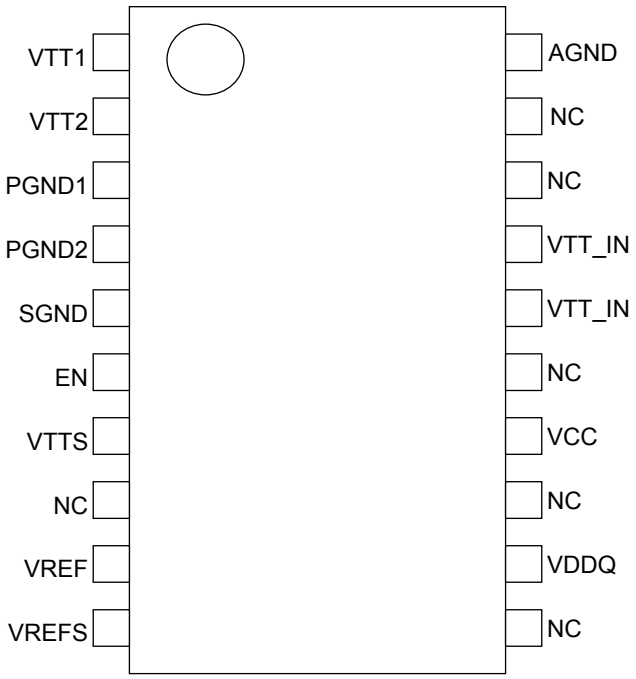


●PIN FUNCTION

PIN No.	PIN NAME	PIN FUNCTION
1	DGND	Digital Ground Pin
2	EN	Enable Input Pin
3	NC	Non Connection
4	VTTS	Detector Pin for Termination Voltage
5	VREF	Reference Voltage Output Pin
6	VREFS	Detector Pin for Reference Voltage
7	NC	Non Connection
8	NC	Non Connection
9	NC	Non Connection
10	VDDQ	Reference Voltage Input Pin
11	NC	Non Connection
12	VCC	VCC Pin
13	VTT_IN	Termination Input Pin
14	VTT_IN	Termination Input Pin
15	VTT	Termination Output Pin
16	VTT	Termination Output Pin
17	NC	Non Connection
18	NC	Non Connection
19	NC	Non Connection
20	PGND	Power Ground Pin

◎BD3532EFV

●PIN CONFIGRATION



●PIN FUNCTION

PIN No.	PIN NAME	PIN FUNCTION
1	VTT1	Termination Output Pin 1
2	VTT2	Termination Output Pin 2
3	PGND1	Power Ground Pin 1
4	PGND2	Power Ground Pin 2
5	SGND	Ground Pin for Reference Voltage
6	EN	Enable Input Pin
7	VTTS	Detector Pin for Termination Voltage
8	N.C.	Non Connection
9	VREF	Reference Voltage Output Pin
10	VREFS	Detector Pin for Reference Voltage
11	N.C.	Non Connection
12	VDDQ	Reference Voltage Input Pin
13	N.C.	Non Connection
14	VCC	VCC Pin
15	N.C.	Non Connection
16	VTT_IN1	Termination Input Pin 1
17	VTT_IN2	Termination Input Pin 2
18	N.C.	Non Connection
19	N.C.	Non Connection
20	AGND	Ground Pin for Analog Ground
-	FIN	Substrate (Connected to AGND)

●Description of operations

・VCC

In BD3533/31/32, an independent power input pin is provided for an internal circuit operation of the IC. This is used to drive the amplifier circuit of the IC, and its maximum current rating is 4 mA. The power supply voltage is 3.3 to 5.5 volts (BD3533) or 5 volts (BD3531/32). It is recommended to connect a bypass capacitor of 1 μF or so to VCC.

・VDDQ

Reference input pin for the output voltage, that may be used to satisfy the JEDEC requirement for DDR-SDRAM (VTT = 1/2VDDQ) by dividing the voltage inside the IC with two 50 kΩ voltage-divider resistors

For BD3533, care must be taken to an input noise to VDDQ pin because this IC also cuts such noise input into half and provides it with the voltage output divided in half. Such noise may be reduced with an RC filter consisting of such resistance and capacitance (220 Ω and 2.2 μF, for instance) that may not give significant effect to voltage dividing inside the IC.

・VTT_IN

VTT_IN is a power supply input pin for VTT output. Voltage in the range between 1.0 and 5.5 volts may be supplied to this VTT_IN terminal, but care must be taken to the current limitation due to on-resistance of the IC and the change in allowable loss due to input/output voltage difference.

Generally, the following voltages are supplied:

・ DDR I VTT_IN=2.5V

・ DDRII VTT_IN=1.8V

Higher impedance of the voltage input at VTT_IN may result in oscillation or degradation in ripple rejection, which must be noted. To VTT_IN terminal, it is recommended to use a 10 μF capacitor characterized with less change in capacitance. But it may depend on the characteristics of the power supply input and the impedance of the pc board wiring, which must be carefully checked before use.

・VREF

In BD3533/31/32, a reference voltage output pin independent from VTT output is given to provide a reference input for a memory controller and a DRAM. Even if EN pin turns to “Low” level, VREF output is kept unchanged, compatible with “Self Refresh” state of DRAM. The maximum current capability of VREF is 20 mA, and a suitable capacitor is needed to stabilize the output voltage. It is recommended to use a combination of a 1.0 to 2.2 μF ceramic capacitor characterized with less change in capacitance and a 0.5 to 2.2 Ω phase compensator resistor, or a 10μF ceramic or tantalum capacitor instead. For an application where VREF current is low, a capacitor of lower capacitance may be used. If VREF current is 1 mA or less, it is possible to secure a phase margin with a ceramic capacitor of 1 μF more or less.

・VTTS

An independent pin provided to improve load regulation of VTT output. In case that longer wiring is needed to the load at VTT output, connecting VTTS from the load side may improve the load regulation.

・VTT

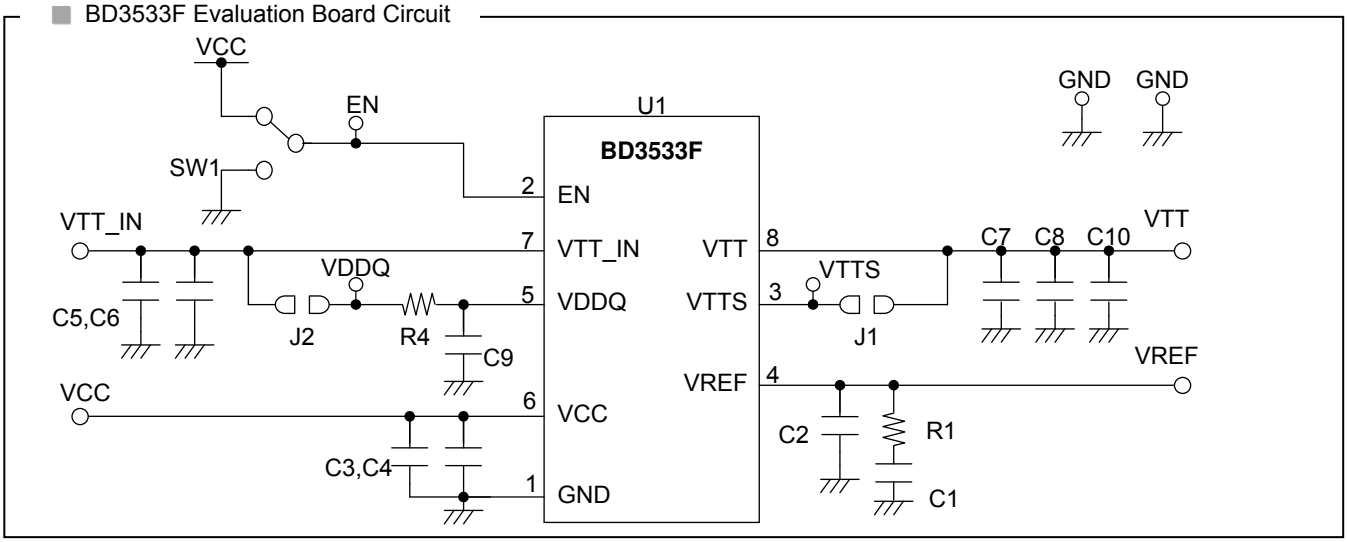
A DDR memory termination output pin. BD3533/31/32 has a sink/source current capability of ±1.0A/±1.5A/±3.0A respectively. The output voltage tracks the voltage divided in half at VDDQ pin. VTT output is turned to OFF when VCC UVLO or thermal shutdown protector is activated with EN pin level turned to “Low”. Do not fail to connect a capacitor to VTT output pin for a loop gain phase compensation and a reduction in output voltage variation in the event of sudden change in load. Insufficient capacitance may cause an oscillation. High ESR (Equivalent Series Resistance) of the capacitor may result in increase in output voltage variation in the event of sudden change in load. It is recommended to use a 220 μF functional polymer capacitor (OS-CON, POS-CAP, NEO-CAP), though it depends on ambient temperature and other conditions. A low ESR ceramic capacitor may reduce a loop gain phase margin and may cause an oscillation, which may be improved by connecting a resistor in series with the capacitor.

・EN

With an input of 2.3 volts or higher, the level at EN pin turns to “High” to provide VTT output. If the input is lowered to 0.8 volts or less, the level at EN pin turns to “Low” and VTT status turns to Hi-Z. But if VCC and VDDQ are established, VREF output is maintained.

●Evaluation Board

■ BD3533F Evaluation Board Circuit



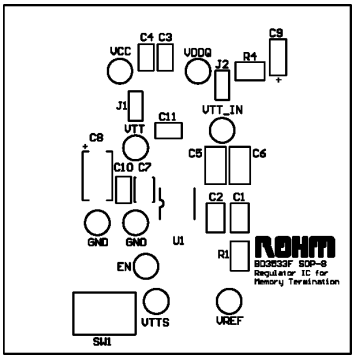
■ BD3533F Evaluation Board Application Components

Part No	Value	Company	Parts Name
U1	-	ROHM	BD3533F
R1	-	-	-
R4	220Ω	ROHM	MCR032200
J1	0Ω	-	-
J2	0Ω	-	-
C1	-	-	-
C2	10uF	KYOCERA	CM21B106M06A
C3	1uF	KYOCERA	CM105B105K06A

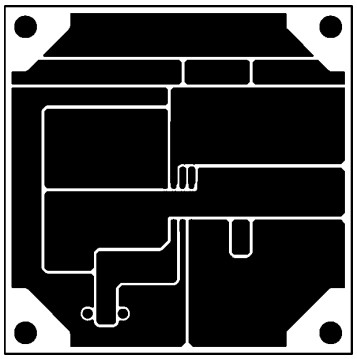
Part No	Value	Company	Parts Name
C4	-	-	-
C5	10uF	KYOCERA	CM21B106M06A
C6	-	-	-
C7	-	-	-
C8	-	-	-
C9	2.2uF	KYOCERA	CM105B225K06A
C10	220uF	SANYO	2R5TPE220MF

■ BD3533F（SOP8） Evaluation Board Layout

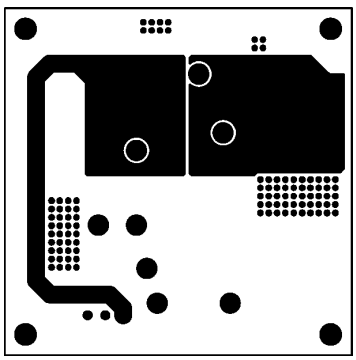
Silk Screen



TOP Layer



Bottom Layer



Versions for MSOP8 and HQFN20V packages are also available.
In addition, BD3533F/FVM/EKN(1A), BD3531F(1.5A), and BD3532F/EFV/KN(3A) are available.

● Heat loss

Thermal design must be conducted with the operation under the conditions listed below (which are the guaranteed temperature range requiring consideration on appropriate margins etc.):

1. Ambient temperature Ta: 100°C or lower
2. Chip junction temperature Tj: 150°C or lower

The chip junction temperature Tj can be considered as follows. See Page 14/16 for θja.

Most of heat loss in BD3533/31/32 occurs at the output N-channel FET. The power lost is determined by multiplying the voltage between VIN and Vo by the output current. As this IC employs the power PKG, the thermal derating characteristics significantly depends on the pc board conditions. When designing, care must be taken to the size of a pc board to be used.

Power dissipation (W) = {Input voltage (V_{TT_IN}) – Output voltage (V_{TT}=1/2VDDQ)}×Io (Ave)

If VTT_IN = 1.8 volts, VDDQ=1.8 volts, and Io (Ave)=0.5 A, for instance, the power dissipation is determined as follows:
Power dissipation (W) = {1.8 (V) – 0.9 (V)} × 0.5 (A) = 0.4 (W)

●NOTE FOR USE

1.Absolute maximum ratings

For the present product, thoroughgoing quality control is carried out, but in the event that applied voltage, working temperature range, and other absolute maximum rating are exceeded, the present product may be destroyed. Because it is unable to identify the short mode, open mode, etc., if any special mode is assumed, which exceeds the absolute maximum rating, physical safety measures are requested to be taken, such as fuses, etc.

2.GND potential

Bring the GND terminal potential to the minimum potential in any operating condition.

3.Thermal design

Consider allowable loss (Pd) under actual working condition and carry out thermal design with sufficient margin provided.

4.Terminal-to-terminal short-circuit and erroneous mounting

When the present IC is mounted to a printed circuit board, take utmost care to direction of IC and displacement. In the event that the IC is mounted erroneously, IC may be destroyed. In the event of short-circuit caused by foreign matter that enters in a clearance between outputs or output and power-GND, the IC may be destroyed.

5.Operation in strong electromagnetic field

The use of the present IC in the strong electromagnetic field may result in maloperation, to which care must be taken.

6.Built-in thermal shutdown protection circuit

The present IC incorporates a thermal shutdown protection circuit (TSD circuit). The working temperature is 175°C (standard value) and has a -15°C (standard value) hysteresis width. When the IC chip temperature rises and the TSD circuit operates, the output terminal is brought to the OFF state. The built-in thermal shutdown protection circuit (TSD circuit) is first and foremost intended for interrupt IC from thermal runaway, and is not intended to protect and warrant the IC. Consequently, never attempt to continuously use the IC after this circuit is activated or to use the circuit with the activation of the circuit premised.

7.Capacitor across output and GND

In the event a large capacitor is connected across output and GND, when Vcc and VIN are short-circuited with 0V or GND for some kind of reasons, current charged in the capacitor flows into the output and may destroy the IC. Use a capacitor smaller than 1000 μF between output and GND.

8.Inspection by set substrate

In the event a capacitor is connected to a pin with low impedance at the time of inspection with a set substrate, there is a fear of applying stress to the IC. Therefore, be sure to discharge electricity for every process. As electrostatic measures, provide grounding in the assembly process, and take utmost care in transportation and storage. Furthermore, when the set substrate is connected to a jig in the inspection process, be sure to turn OFF power supply to connect the jig and be sure to turn OFF power supply to remove the jig.

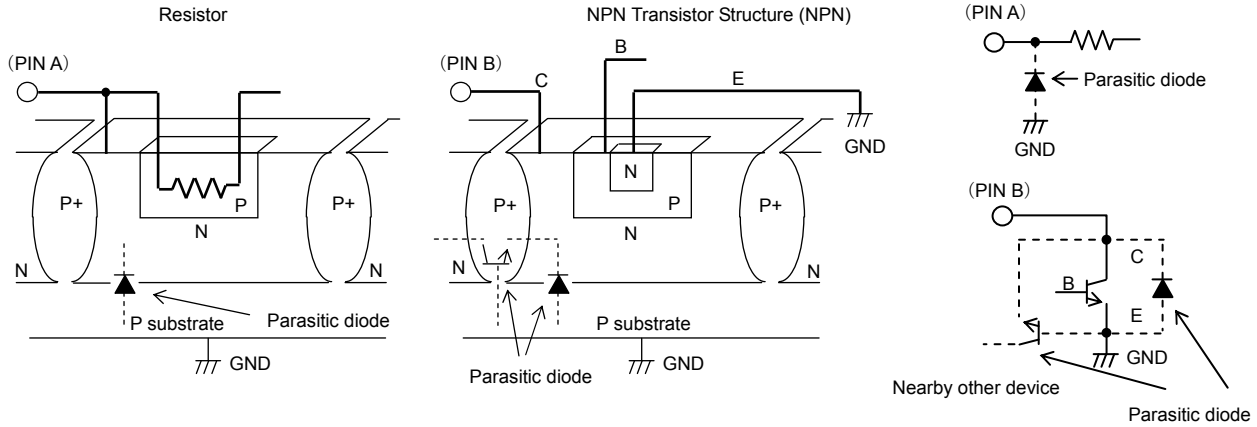
9. Inputs to IC terminals

This device is a monolithic IC with P^+ isolation between P-substrate and each element as illustrated below. This P-layer and the N-layer of each element form a PN junction which works as:

・a diode if the electric potentials at the terminals satisfy the following relationship; GND>Terminal A>Terminal B, or

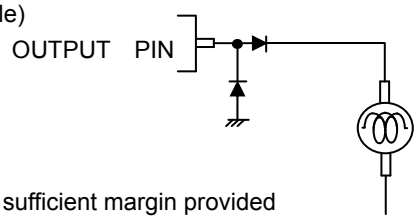
・a parasitic transistor if the electric potentials at the terminals satisfy the following relationship; Terminal B>GND Terminal A.

The structure of the IC inevitably forms parasitic elements, the activation of which may cause interference among circuits, and/or malfunctions contributing to breakdown. It is therefore requested to take care not to use the device in such manner that the voltage lower than GND (at P-substrate) may be applied to the input terminal, which may result in activation of parasitic elements.



10. GND wiring pattern
When both a small-signal GND and high current GND are present, single-point grounding (at the set standard point) is recommended, in order to separate the small-signal and high current patterns, and to be sure the voltage change stemming from the wiring resistance and high current does not cause any voltage change in the small-signal GND. In the same way, care must be taken to avoid wiring pattern fluctuations in any connected external component GND.
11. Output capacitor (C1)
Do not fail to connect a output capacitor to VREF output terminal for stabilization of output voltage. The capacitor connected to VREF output terminal works as a loop gain phase compensator. Insufficient capacitance may cause an oscillation. It is recommended to use a low temperature coefficient 1-10 μF ceramic capacitor, though it depends on ambient temperature and load conditions. It is therefore requested to carefully check under the actual temperature and load conditions to be applied.
12. Output capacitor (C4)
Do not fail to connect a capacitor to VTT output pin for stabilization of output voltage. This output capacitor works as a loop gain phase compensator and an output voltage variation reducer in the event of sudden change in load. Insufficient capacitance may cause an oscillation. And if the equivalent series resistance (ESR) of this capacitor is high, the variation in output voltage increases in the event of sudden change in load. It is recommended to use a 47-220 μF functional polymer capacitor, though it depends on ambient temperature and load conditions. Using a low ESR ceramic capacitor may reduce a loop gain phase margin and cause an oscillation, which may be improved by connecting a resistor in series with the capacitor. It is therefore requested to carefully check under the actual temperature and load conditions to be applied.
13. Input capacitors (C2 and C3)
These input capacitors are used to reduce the output impedance of power supply to be connected to the input terminals (VCC and VTT_IN). Increase in the power supply output impedance may result in oscillation or degradation in ripple rejecting characteristics. It is recommended to use a low temperature coefficient 1μF (for VCC) and 10μF (for VTT_IN) capacitor, but it depends on the characteristics of the power supply input, and the capacitance and impedance of the pc board wiring pattern. It is therefore requested to carefully check under the actual temperature and load conditions to be applied.
14. Input terminals (VCC, VDDQ, VTT_IN and EN)
VCC, VDDQ, VTT_IN and EN terminals of this IC are made up independent one another. To VCC terminal, the UVLO function is provided for malfunction protection. Irrespective of the input order of the inputs terminals, VTT output is activated to provide the output voltage when UVLO and EN voltages reach the threshold voltage while VREF output is activated when UVLO voltage reaches the threshold. If VDDQ and VTT_IN terminals have equal potential and common impedance, any change in current at VTT_IN terminal may result in variation of VTT_IN voltage, which affects VDDQ terminal and may cause variation in the output voltage. It is therefore required to perform wiring in such manner that VDDQ and VTT_IN terminals may not have common impedance. If impossible, take appropriate corrective measures including suitable CR filter to be inserted between VDDQ and VTT_IN terminals.
15. VTTS terminal
A terminal used to improve load regulation of VTT output. Connection with VTT terminal must be done not to have common impedance with high current line, which may offer better load regulation of VTT output.
16. Operating range
Within the operating range, the operation and function of the circuits are generally guaranteed at an ambient temperature within the range specified. The values specified for electrical characteristics may not be guaranteed, but drastic change may not occur to such characteristics within the operating range.
17. Allowable loss Pd
For the allowable loss, the thermal derating characteristics are shown in the Exhibit, which should be used as a guide. Any uses that exceed the allowable loss may result in degradation in the functions inherent to IC including a decrease in current capability due to chip temperature increase. Use within the allowable loss.
18. Built-in thermal shutdown protection circuit
Thermal shutdown protection circuit is built-in to prevent thermal breakdown. Turns VTT output to OFF when the thermal shutdown protection circuit activates. This thermal shutdown protection circuit is originally intended to protect the IC itself. It is therefore requested to conduct a thermal design not to exceed the temperature under which the thermal shutdown protection circuit can work.
19. The use in the strong electromagnetic field may sometimes cause malfunction, to which care must be taken.
In the event that load containing a large inductance component is connected to the output terminal, and generation of back-EMF at the start-up and when output is turned OFF is assumed, it is requested to insert a protection diode.
20. In the event that load containing a large inductance component is connected to the output terminal, and generation of back-EMF at the start-up and when output is turned OFF is assumed, it is requested to insert a protection diode.

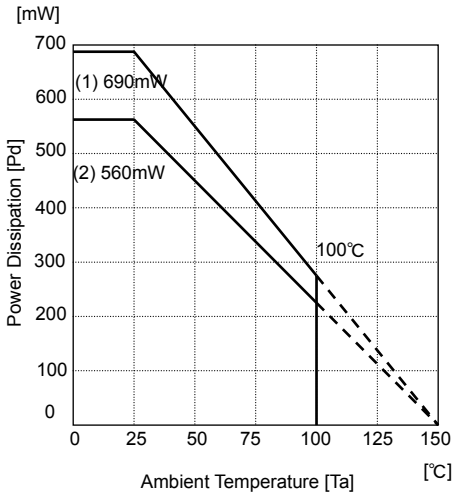
(Example)



21. We are certain that examples of applied circuit diagrams are recommendable, but you are requested to thoroughly confirm the characteristics before using the IC.
In addition, when the IC is used with the external circuit changed, decide the IC with sufficient margin provided while consideration is being given not only to static characteristics but also variations of external parts and our IC including transient characteristics.

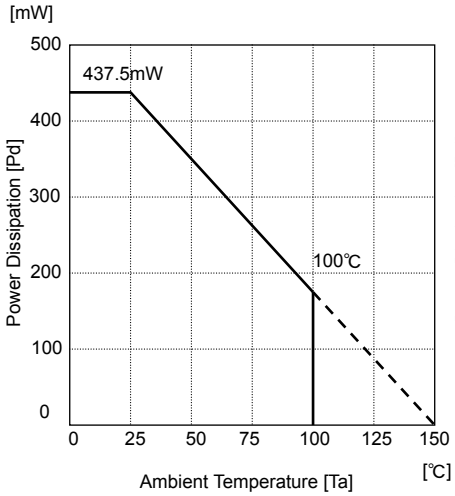
●POWER DISSIPATION

◎SOP8(BD3533F/31F/32F)



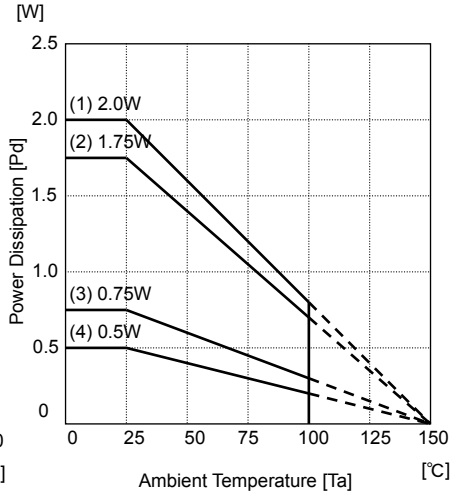
(1) 70mm×70mm×1.6mm Glass-epoxy PCB
θj-c=181℃/W
(2) With no heat sink
θj-a=222℃/W

◎MSOP8(BD3533FVM)



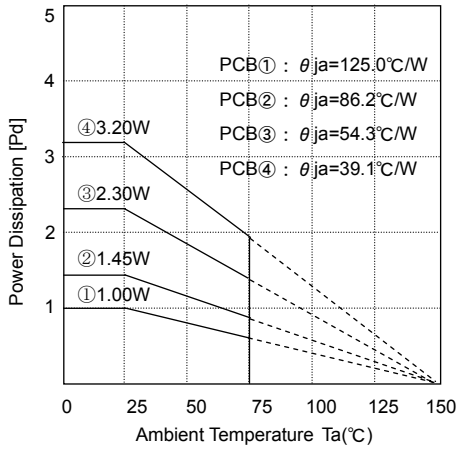
With no heat sink
θj-a=286℃/W

◎HQFN20V(BD3533EKN)



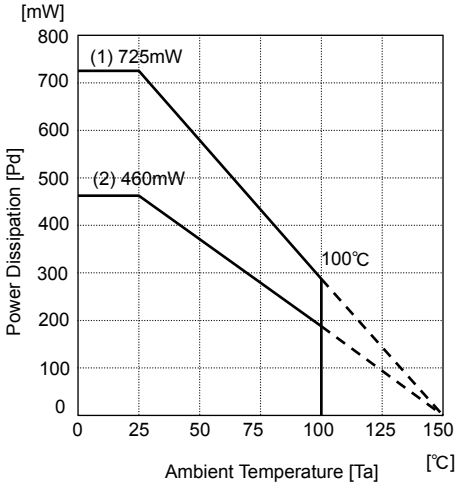
(1) With no heat sink
θj-a=250℃/W
(2) PCB (substrate surface copper foil area : None)
θj-a=166.7℃/W
(3) PCB Single-layer substrate
(substrate surface copper foil area : 15mm×15mm)
θj-a=71.4℃/W
(4) PCB Double-layer substrate
(substrate surface copper foil area : 60mm×60mm)
θj-a=62.5℃/W

◎HTSSOP-B20(BD3532EFV)



measure : TH-156 (Kuwano Denki)
measure condition : Rohm Standard Board
PCB size : 70mm×70mm×1.6mmt
(Thermal vias in the board) Connect the board with the exposed area at the bottom surface of the package by soldering.
PCB① : Single-layer substrate
PCB② : Double-layer substrate (substrate surface copper foil area : 15mm×15mm)
PCB③ : Double-layer substrate (substrate surface copper foil area : 70mm×70mm)

◎VQFN28(BD3532KN)



(2) 70mm×70mm×1.6mm Glass-epoxy PCB
θj-c=172℃/W
(2) With no heat sink
θj-a=270℃/W

●Ordering part number

B	D	3	5	3	3	F	V	M	-	T	R

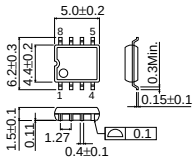
Part Number
- **BD3533**
- **BD3531**
- **BD3532**

Package Type
- **F : SOP8**
- **FVM : MSOP8**
- **HFV : HTSSOP-B20**
- **KN : VQFN28**
- **EKN : HQFN20V**

TR Emboss tape reel opposite draw-out side: 1 pin
E2 Emboss tape reel opposite draw-out side: 1 pin

SOP8

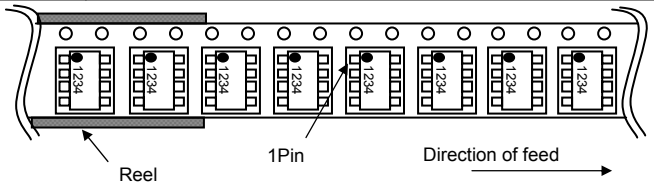
<Dimension>



(Unit:mm)

<Tape and Reel information>

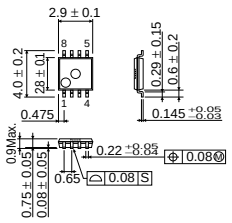
Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



※When you order , please order in times the amount of package quantity.

MSOP8

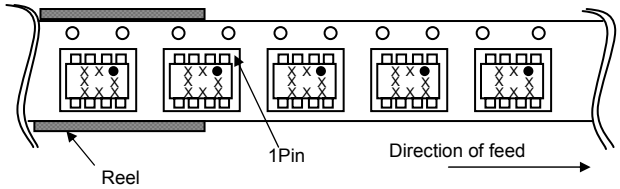
<Dimension>



(Unit:mm)

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper light when you hold reel on the left hand and you pull out the tape on the right hand)



※When you order , please order in times the amount of package quantity.

HTSSOP-B20

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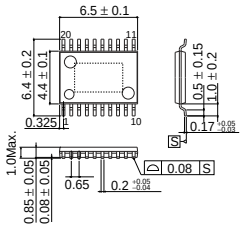
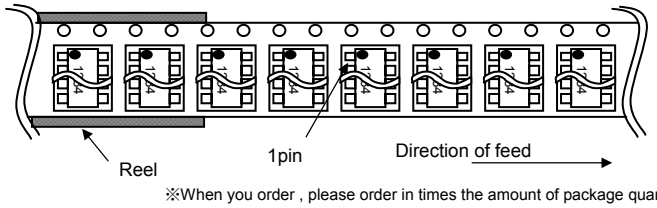


(Unit:mm)

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



※When you order , please order in times the amount of package quantity.

VQFN28

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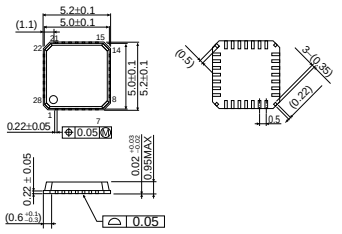
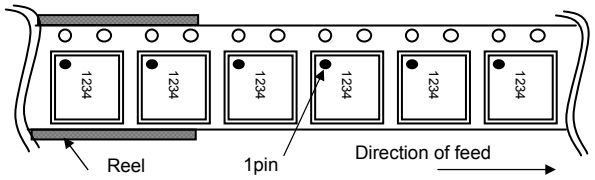


(Unit:mm)

<Tape and Reel information>

Tape	Embossed carrier tape(with dry pack)
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



※When you order , please order in times the amount of package quantity.

HQFN20V

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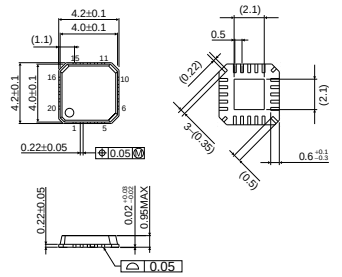
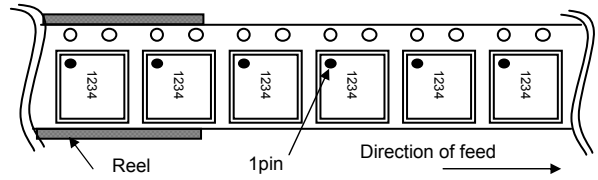


(Unit:mm)

<Tape and Reel information>

Tape	Embossed carrier tape(with dry pack)
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



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