

Dual 5 A High Speed Low-Side MOSFET Drivers with Enable



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NCP81071

NCP81071 is a high speed dual low-side MOSFETs driver. It is capable of providing large peak currents into capacitive loads. This driver can deliver 5 A peak current at the Miller plateau region to help reduce the Miller effect during MOSFETs switching transition. This driver also provides enable functions to give users better control capability in different applications. ENA and ENB are implemented on pin 1 and pin 8 which were previously unused in the industry standard pin-out. They are internally pulled up to driver's input voltage for active high logic and can be left open for standard operations. This part is available in MSOP8-EP package, SOIC8 package and WDFN8 3 mm x 3 mm package.

Features

- High Current Drive Capability ± 5 A
- TTL/CMOS Compatible Inputs Independent of Supply Voltage
- Industry Standard Pin-out
- High Reverse Current Capability (6 A) Peak
- Enable Functions for Each Driver
- 8 ns Typical Rise and 8 ns Typical Fall Times with 1.8 nF Load
- Typical Propagation Delay Times of 20 ns with Input Falling and 20 ns with Input Rising
- Input Voltage from 4.5 V to 20 V
- Dual Outputs can be Paralleled for Higher Drive Current
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

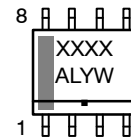
Applications

- Server Power
- Telecommunication, Datacenter Power
- Synchronous Rectifier
- Switch Mode Power Supply
- DC/DC Converter
- Power Factor Correction
- Motor Drive
- Renewable Energy, Solar Inverter

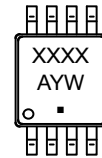
MARKING DIAGRAMS



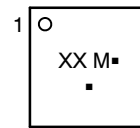
SOIC-8
D SUFFIX
CASE 751



MSOP-8
Z SUFFIX
CASE 846AM



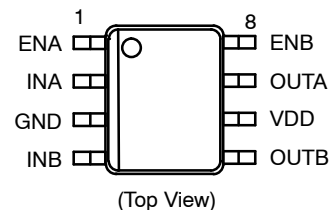
WDFN8
MN SUFFIX
CASE 511CD



XX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

NCP81071

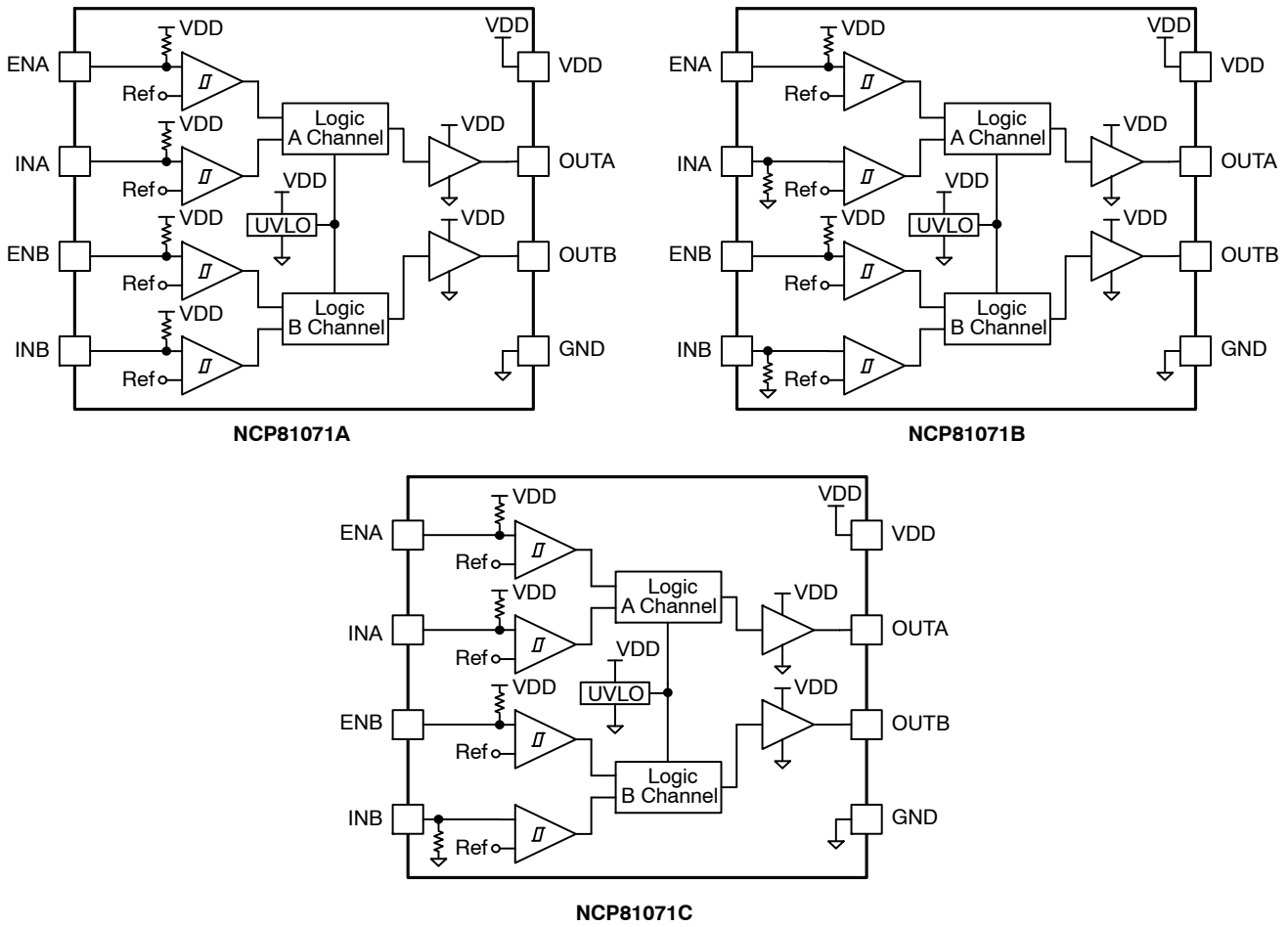


Figure 1. NCP81071 Block Diagram

Table 1. PIN DESCRIPTION

| Pin No. | Symbol | Description |
|---------|--------|---|
| 1 | ENA | Enable input for the driver channel A with logic compatible threshold and hysteresis. This pin is used to enable and disable the driver output. It is internally pulled up to VDD with a 200 kΩ resistor for active high operation. The output of the pin when the device is disabled will be always low. |
| 2 | INA | Input of driver channel A which has logic compatible threshold and hysteresis. If not used, this pin should be connected to either VDD or GND. It should not be left unconnected. |
| 3 | GND | Common ground. This ground should be connected very closely to the source of the power MOSFET. |
| 4 | INB | Input of driver channel B which has logic compatible threshold and hysteresis. If not used, this pin should be connected to either VDD or GND. It should not be left unconnected. |
| 5 | OUTB | Output of driver channel B. The driver is able to provide 5 A drive current to the gate of the power MOSFET. |
| 6 | VDD | Supply voltage. Use this pin to connect the input power for the driver device. |
| 7 | OUTA | Output of driver channel A. The driver is able to provide 5 A drive current to the gate of the power MOSFET. |
| 8 | ENB | Enable input for the driver channel B with logic compatible threshold and hysteresis. This pin is used to enable and disable the driver output. It is internally pulled up to VDD with a 200 kΩ resistor for active high operation. The output of the pin when the device is disabled will be always low. |

NCP81071

TYPICAL APPLICATION CIRCUIT

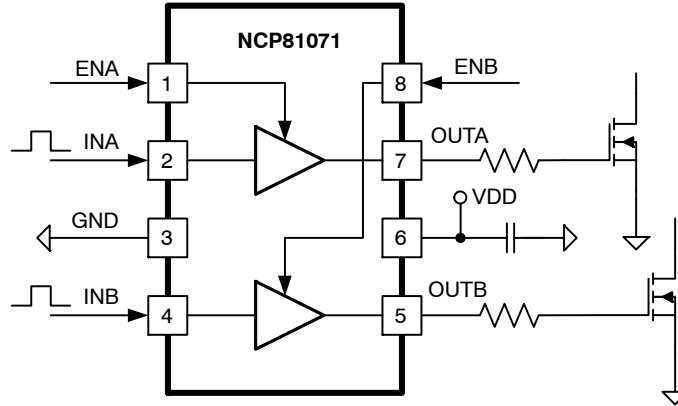


Table 2. ABSOLUTE MAXIMUM RATINGS

| | | Value | | Unit |
|---------------------------------|--------------------------|-------|---------|------|
| | | Min | Max | |
| Supply Voltage | VDD | -0.3 | 24 | V |
| Output Current (DC) | I _{out_dc} | 0.3 | | A |
| Reverse Current (Pulse < 1 μs) | | | 6.0 | A |
| Output Current (Pulse < 0.5 μs) | I _{out_pulse} | 6.0 | | A |
| Input Voltage | INA, INB | -6.0 | VDD+0.3 | V |
| Enable Voltage | ENA, ENB | -0.3 | VDD+0.3 | V |
| Output Voltage | OUTA, OUTB | -0.3 | VDD+0.3 | V |
| Output Voltage (Pulse < 0.5 μs) | OUTA, OUTB | -3.0 | VDD+3.0 | V |
| Junction Operation Temperature | T _J | -40 | 150 | °C |
| Storage Temperature | T _{stg} | -65 | 160 | °C |
| Electrostatic Discharge | Human body model, HBM | 4000 | | V |
| | Charge device model, CDM | 1000 | | V |
| OUTA OUTB Latch-up Protection | | 500 | | mA |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 3. RECOMMENDED OPERATING CONDITIONS

| Parameter | Rating | Unit |
|----------------------------|-------------|------|
| VDD supply Voltage | 4.5 to 20 | V |
| INA, INB input voltage | -5.0 to VDD | V |
| ENA, ENB input voltage | 0 to VDD | V |
| Junction Temperature Range | -40 to +140 | °C |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 4. THERMAL INFORMATION

| Package | θ _{JA} (°C/W) | θ _{JC} (°C/W) | Ψ _{JT} (°C/W) (Note 1) |
|-----------|------------------------|------------------------|---------------------------------|
| SOIC-8 | 115 | 50 | |
| MSOP-8 EP | 39 | 4.7 | 11 |
| WDFN8 3x3 | 39 | 4.7 | |

1. Ψ_{JT}: approximate thermal impedance, junction-to-case top.

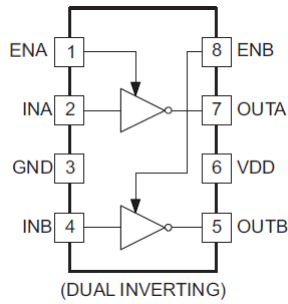
NCP81071

Table 5. INPUT/OUTPUT TABLE

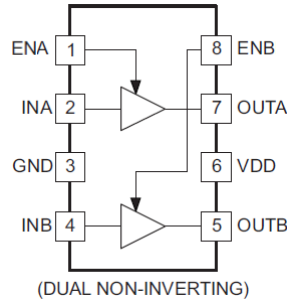
| ENA | ENB | INA | INB | NCP81071A | | NCP81071B | | NCP81071C | |
|------------|------------|------------|------------|-----------|------|-----------|------|-----------|------|
| | | | | OUTA | OUTB | OUTA | OUTB | OUTA | OUTB |
| H | H | L | L | H | H | L | L | H | L |
| H | H | L | H | H | L | L | H | H | H |
| H | H | H | L | L | H | H | L | L | L |
| H | H | H | H | L | L | H | H | L | H |
| L | L | Any | Any | L | L | L | L | L | L |
| Any | Any | x (Note 2) | x (Note 2) | L | L | L | L | L | L |
| x (Note 2) | x (Note 2) | L | L | H | H | L | L | H | L |
| x (Note 2) | x (Note 2) | L | H | H | L | L | H | H | H |
| x (Note 2) | x (Note 2) | H | L | L | H | H | L | L | L |
| x (Note 2) | x (Note 2) | H | H | L | L | H | H | L | H |

2. Floating condition, internal resistive pull up or pull down configures output condition

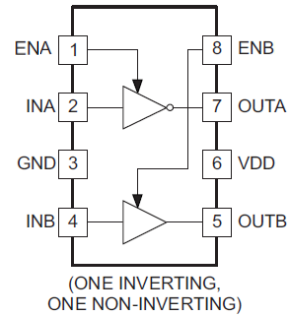
PRODUCT MATRIX



NCP81071A



NCP81071B



NCP81071C

NCP81071

Table 6. ELECTRICAL CHARACTERISTICS

(Typical values: $V_{DD} = 12\text{ V}$, $1\ \mu\text{F}$ from V_{DD} to GND, $T_A = T_J = -40^\circ\text{C}$ to 140°C , typical at $T_{AMB} = 25^\circ\text{C}$, unless otherwise specified)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|--|-----------|--|-----|-----|-----|---------------|
| SUPPLY VOLTAGE | | | | | | |
| VDD Under Voltage Lockout (rising) | V_{CCR} | VDD rising | 3.5 | 4.0 | 4.5 | V |
| VDD Under Voltage Lockout (hysteresis) | V_{CCH} | | | 400 | | mV |
| Operating Current (no switching) | I_{DD} | INA = 0, INB = 5 V, ENA = ENB = 0 INA = 5 V, INB = 0, ENA = ENB = 0 INA = 0, INB = 5 V, ENA = ENB = 5 V INA = 5 V, INB = 0, ENA = ENB = 5 V | | 1.4 | 3 | mA |
| VDD Under Voltage Lockout to Output Delay (Note 3) | | VDD rising | | 10 | | μs |

INPUTS

| | | | | | | |
|-------------------------------|-----------|--------------------------------------|-----|-----|-----|------------|
| High Threshold | V_{thH} | Input rising from logic low | 1.8 | 2.0 | 2.2 | V |
| Low Threshold | V_{thL} | Input falling from logic high | 0.8 | 1.0 | 1.2 | V |
| INA, INB Pull-Up Resistance | | OUTA = OUTB = Inverter Configuration | | 200 | | k Ω |
| INA, INB Pull-Down Resistance | | OUTA = OUTB = Buffer Configuration | | 200 | | k Ω |

OUTPUTS

| | | | | | | |
|--|--------------|-----------------------------------|--|-----|---|----------|
| Output Resistance High | R_{OH} | IOU _T = -10 mA | | 0.8 | 2 | Ω |
| Output Resistance Low | R_{OL} | IOU _T = +10 mA | | 0.8 | 2 | Ω |
| Peak Source Current (Note 4) | I_{Source} | OUTA/OUTB = GND 200 ns Pulse | | 5 | | A |
| Miller Plateau Source Current (Note 4) | I_{Source} | OUTA/OUTB = 5.0 V 200 ns Pulse | | 4.5 | | A |
| Peak Sink Current (Note 4) | I_{Sink} | OUTA/OUTB = VDD 200 ns Pulse | | 5 | | A |
| Miller Plateau Sink Current (Note 4) | I_{Sink} | OUTA/OUTB = 5.0 V 200 ns Pulse | | 3.5 | | A |

ENABLE

| | | | | | | |
|---|-------------|----------------------------|-----|-----|-----|------------|
| High-Level Input Voltage | V_{IN_H} | Low to High Transition | 1.8 | 2.0 | 2.2 | V |
| Low-Level Input Voltage | V_{IN_L} | High to Low Transition | 0.8 | 1.0 | 1.2 | V |
| ENA, ENB pull-up resistance | | | | 200 | | k Ω |
| Propagation Delay Time (EN to OUT) (Notes 3, 5) | t_{d3} | $C_{Load} = 1.8\text{ nF}$ | 16 | 20 | 29 | ns |
| Propagation Delay Time (EN to OUT) (Notes 3, 5) | t_{d4} | $C_{Load} = 1.8\text{ nF}$ | 16 | 20 | 29 | ns |

SWITCHING CHARACTERISTICS

| | | | | | | |
|---|----------|--|----|----|----|----|
| Propagation Delay Time Low to High, IN Rising (IN to OUT) (Notes 3, 5) | t_{d1} | $C_{Load} = 1.8\text{ nF}$ | 16 | 20 | 29 | ns |
| Propagation Delay Time High to Low, IN Falling (IN to OUT) (Notes 3, 5) | t_{d2} | $C_{Load} = 1.8\text{ nF}$ | 16 | 20 | 29 | ns |
| Rise Time (Note 5) | t_r | $C_{Load} = 1.8\text{ nF}$ | | 8 | 15 | ns |
| Fall Time (Note 5) | t_f | $C_{Load} = 1.8\text{ nF}$ | | 8 | 15 | ns |
| Delay Matching between 2 Channels (Note 6) | t_m | INA = INB, OUTA and OUTB at 50% Transition Point | | 1 | 4 | ns |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Guaranteed by design.

4. Not production tested, guaranteed by design and statistical analysis.

5. See timing diagrams in Figure 2, Figure 3, Figure 4 and Figure 5.

6. Guaranteed by characterization.

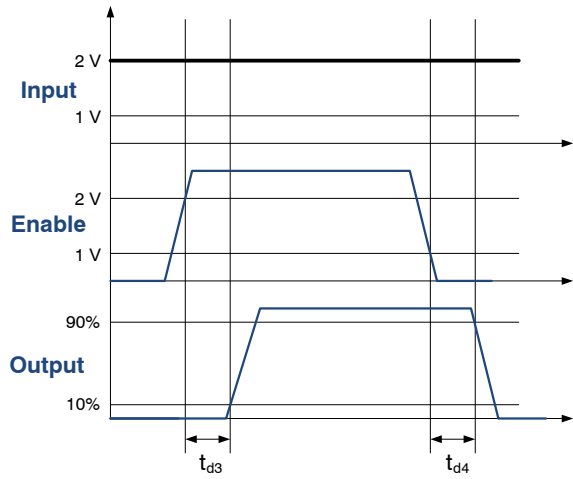


Figure 2. Enable Function for Non-inverting Input Driver Operation

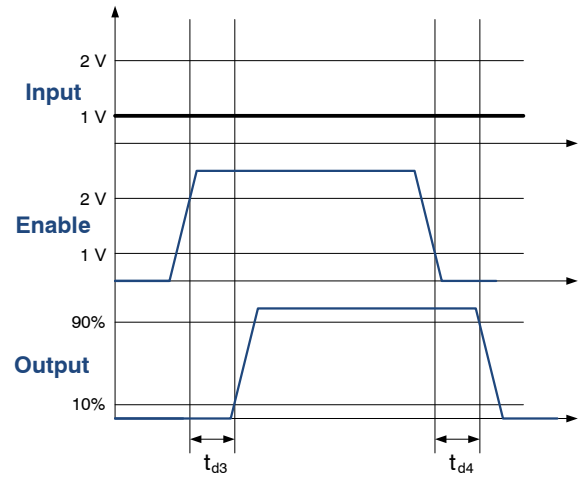


Figure 3. Enable Function for Inverting Input Driver Operation

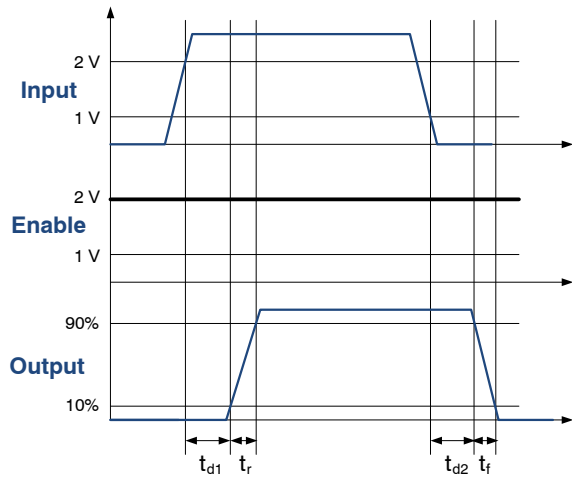


Figure 4. Non-inverting Input Driver Operation

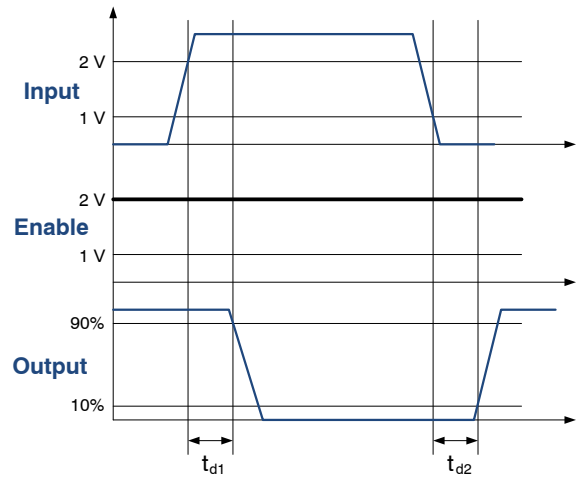


Figure 5. Inverting Input Driver Operation

TYPICAL CHARACTERISTICS

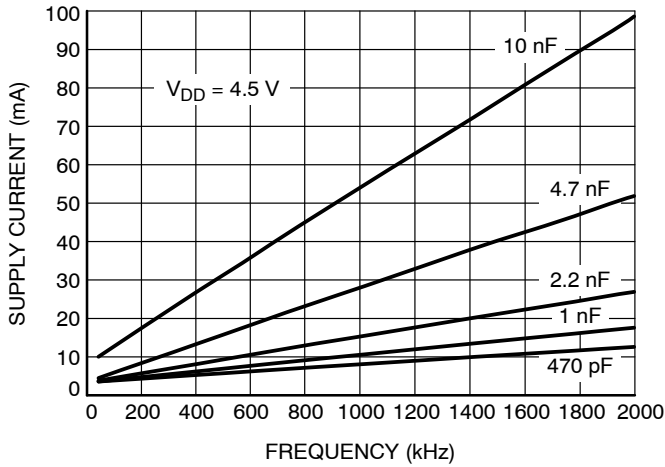


Figure 6. Supply Current vs. Switching Frequency ($V_{DD} = 4.5\text{ V}$)

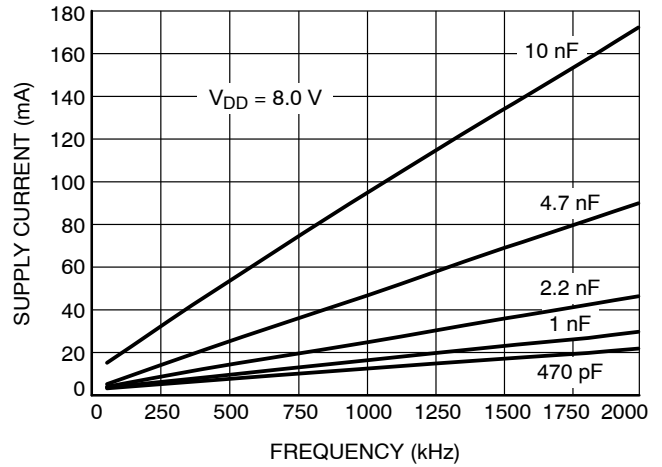


Figure 7. Supply Current vs. Switching Frequency ($V_{DD} = 8.0\text{ V}$)

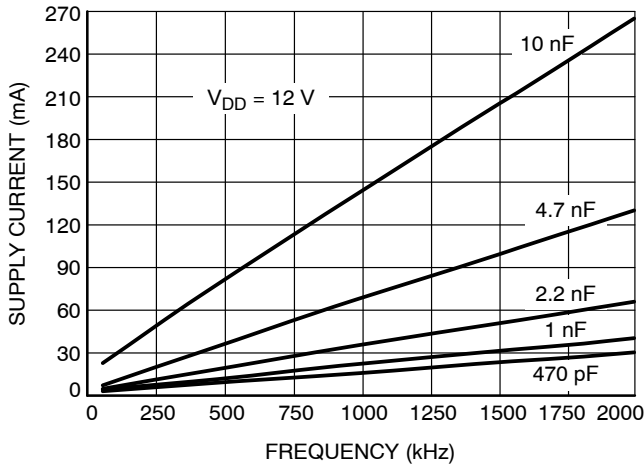


Figure 8. Supply Current vs. Switching Frequency ($V_{DD} = 12\text{ V}$)

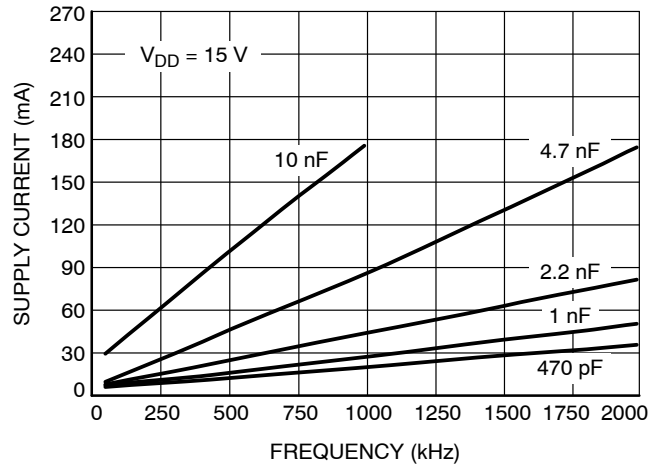


Figure 9. Supply Current vs. Switching Frequency ($V_{DD} = 15\text{ V}$)

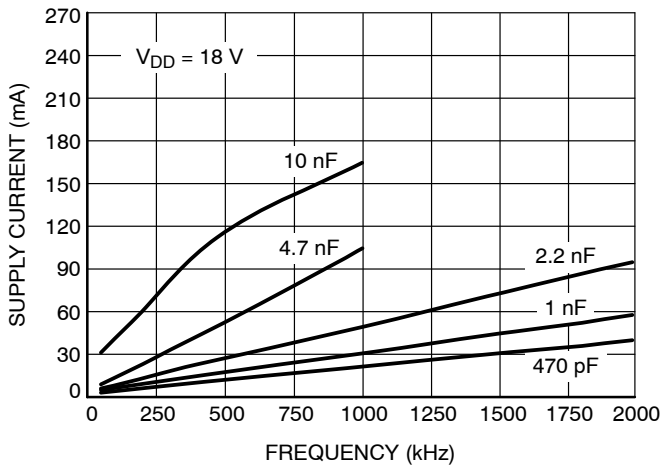


Figure 10. Supply Current vs. Switching Frequency ($V_{DD} = 18\text{ V}$)

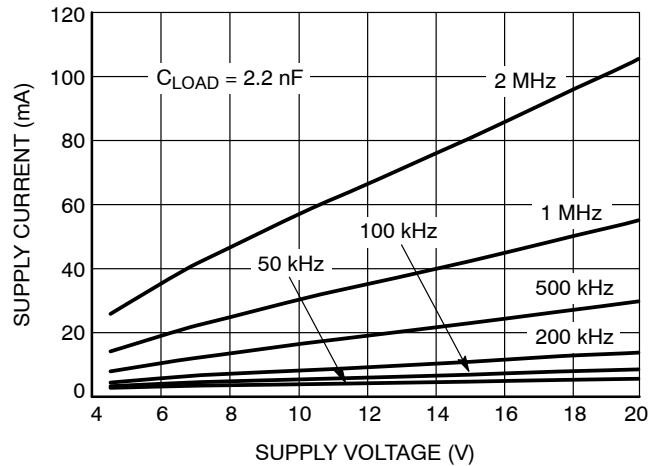


Figure 11. Supply Current vs. Supply Voltage ($C_{LOAD} = 2.2\text{ nF}$)

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TYPICAL CHARACTERISTICS

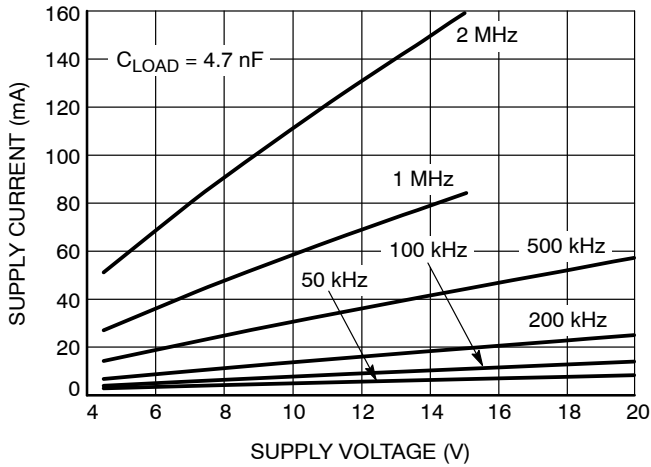


Figure 12. Supply Current vs. Supply Voltage ($C_{LOAD} = 4.7$ nF)

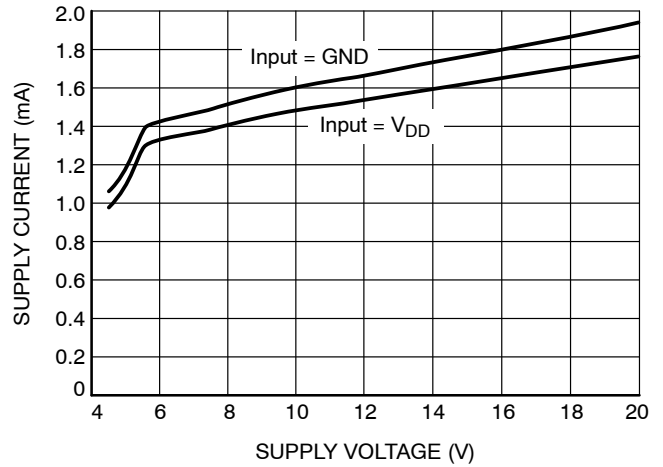


Figure 13. Supply Current vs. Supply Voltage (NCP81071A)

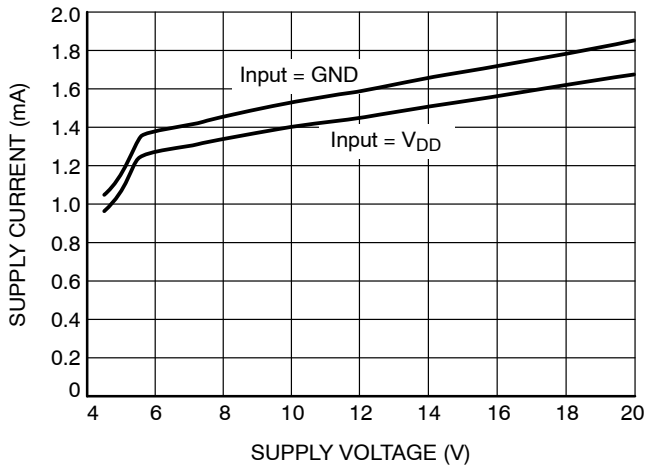


Figure 14. Supply Current vs. Supply Voltage (NCP81071B)

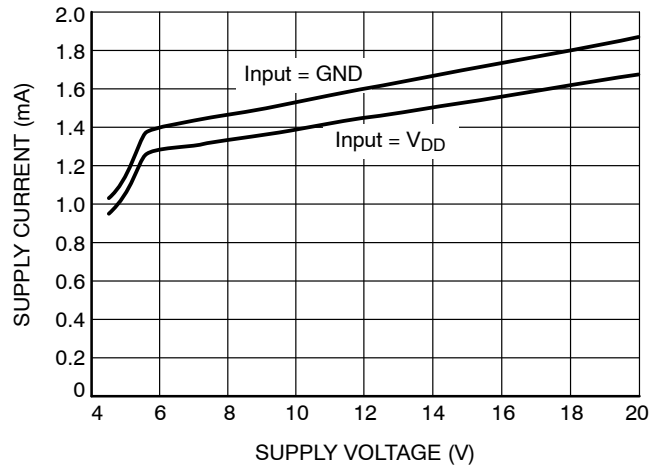


Figure 15. Supply Current vs. Supply Voltage (NCP81071C)

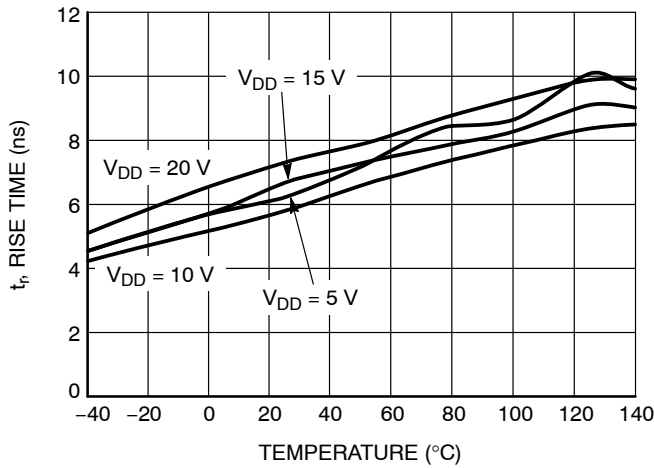


Figure 16. Rise Time vs. Temperature

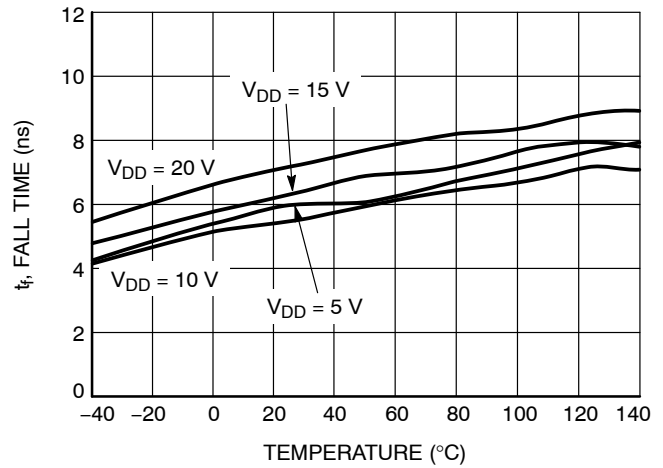


Figure 17. Fall Time vs. Temperature

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TYPICAL CHARACTERISTICS

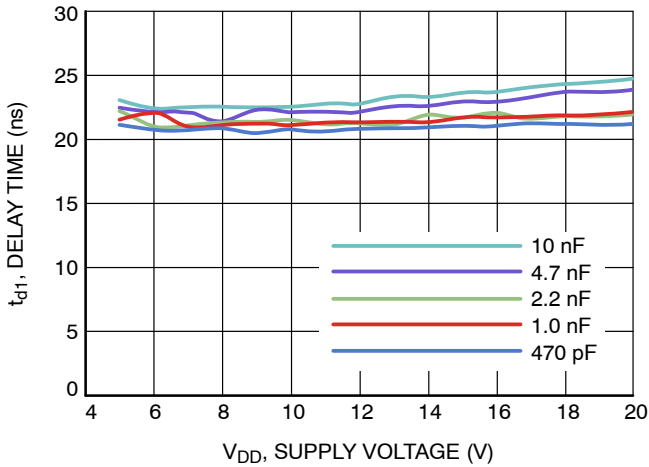


Figure 18. Propagation Delay t_{d1} vs. Supply Voltage

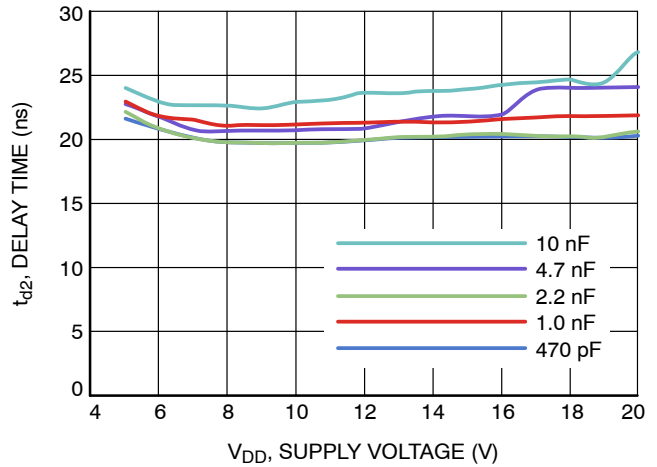


Figure 19. Propagation Delay t_{d2} vs. Supply Voltage

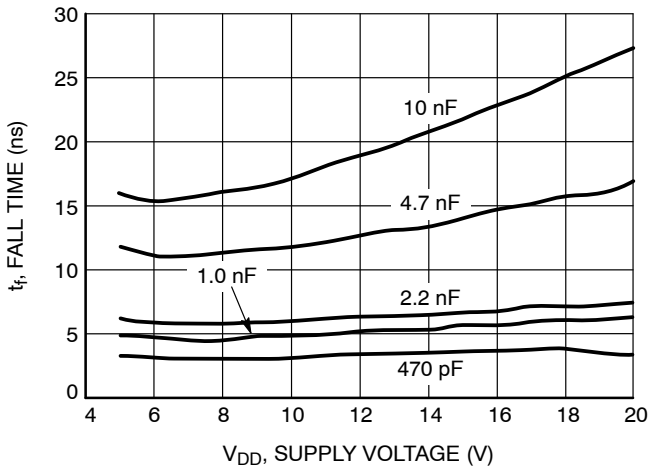


Figure 20. Fall Time t_f vs. Supply Voltage

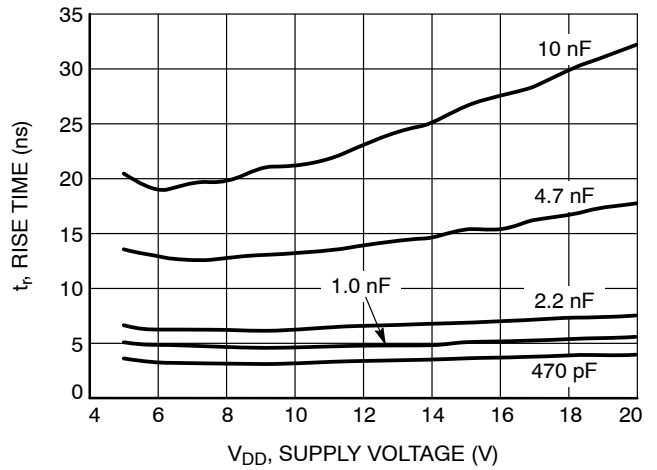


Figure 21. Rise Time t_r vs. Supply Voltage



Figure 22. Output Behavior vs. Supply Voltage NCP81071A (Inverting) 10 nF between Output and GND, INA = GND, ENA = VDD



Figure 23. Output Behavior vs. Supply Voltage NCP81071A (Inverting) 10 nF between Output and GND, INA = GND, ENA = VDD

NCP81071

TYPICAL CHARACTERISTICS

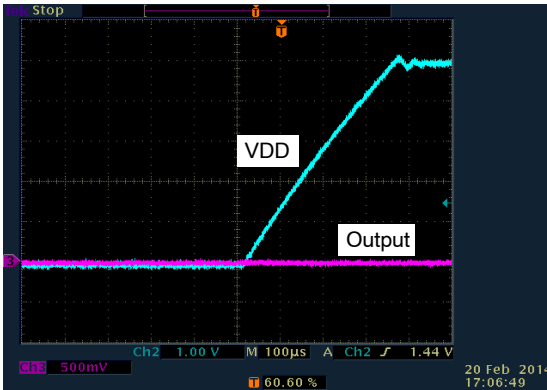


Figure 24. Output Behavior vs. Supply Voltage NCP81071A (Inverting) 10 nF between Output and GND, INA = VDD, ENA = VDD

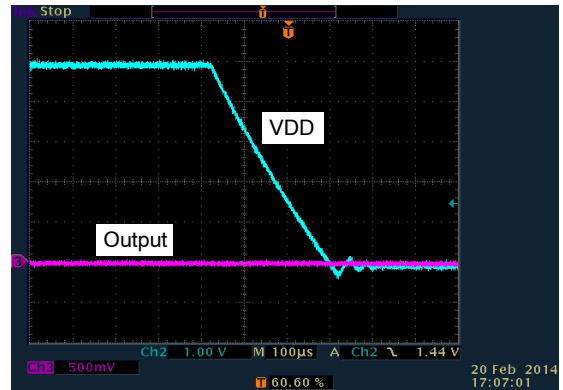


Figure 25. Output Behavior vs. Supply Voltage NCP81071A (Inverting) 10 nF between Output and GND, INA = VDD, ENA = VDD

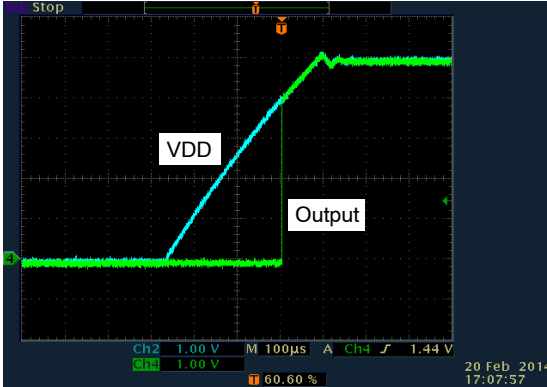


Figure 26. Output Behavior vs. Supply Voltage NCP81071B (Non-Inverting) 10 nF between Output and GND, INA = VDD, ENA = VDD

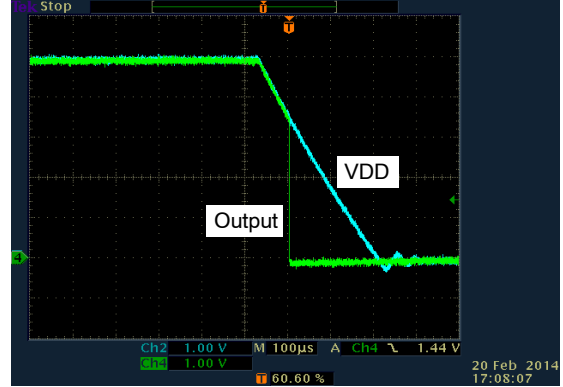


Figure 27. Output Behavior vs. Supply Voltage NCP81071B (Non-Inverting) 10 nF between Output and GND, INA = VDD, ENA = VDD

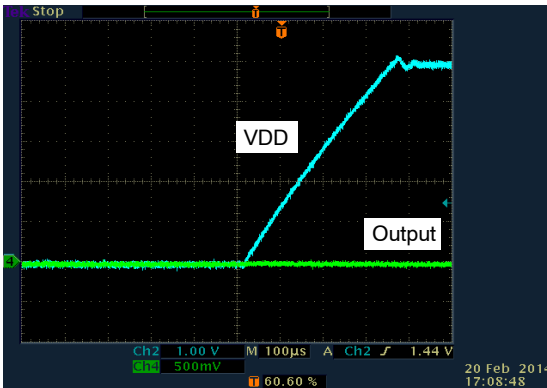


Figure 28. Output Behavior vs. Supply Voltage NCP81071B (Non-Inverting) 10 nF between Output and GND, INA = GND, ENA = VDD

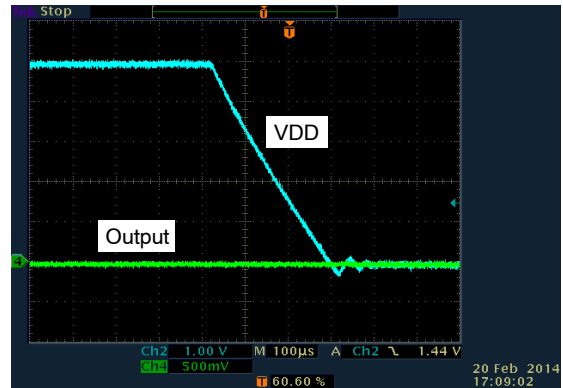


Figure 29. Output Behavior vs. Supply Voltage NCP81071B (Non-Inverting) 10 nF between Output and GND, INA = GND, ENA = VDD

NCP81071

LAYOUT GUIDELINES

The switching performance of NCP81071 highly depends on the design of PCB board. The following layout design guidelines are recommended when designing boards using these high speed drivers.

Place the driver as close as possible to the driven MOSFET.

Place the bypass capacitor between VDD and GND as close as possible to the driver to improve the noise filtering. It is preferred to use low inductance components such as chip capacitor and chip resistor. If vias are used, connect several paralleled vias to reduce the inductance of the vias.

Minimize the turn-on/sourcing current and turn-off/sinking current paths in order to minimize stray inductance. Otherwise high di/dt established in these loops with stray inductance can induce significant voltage spikes on the output of the driver and MOSFET Gate terminal.

Keep power loops as short as possible by paralleling the source and return traces (flux cancellation).

Keep low level signal lines away from high level power lines with a lot of switching noise.

Place a ground plane for better noise shielding. Beside noise shielding, ground plane is also useful for heat dissipation.

NCP81071 DFN and MSOP package have thermal pad for: 1) quiet GND for all the driver circuits; 2) heat sink for the driver. This pad must be connected to a ground plane and no switching currents from the driven MOSFET should pass through the ground plane under the driver. To maximize the heatsinking capability, it is recommended several ground layers are added to connect to the ground plane and thermal pad. A via array within the area of package can conduct the heat from the package to the ground layers and the whole PCB board. The number of vias and the size of ground plane are determined by the power dissipation of NCP81071 (VDD voltage, switching frequency and load condition), the air flow condition and its maximum junction temperature.

ORDERING INFORMATION

| Part Number | Output Configuration | Temperature Range (°C) | Package Type | Shipping† |
|----------------|------------------------------------|------------------------|-----------------------|--------------------|
| NCP81071ADR2G | dual inverting | -40 to +140 | SOIC-8 (Pb-Free) | 2500 / Tape & Reel |
| NCP81071BDR2G | dual non inverting | | | |
| NCP81071CDR2G | One inverting one non inverting | | | |
| NCP81071AZR2G | dual inverting | | MSOP8 EP (Pb-Free) | 3000 / Tape & Reel |
| NCP81071BZR2G | dual non inverting | | | |
| NCP81071CZR2G | One inverting one non inverting | | | |
| NCP81071AMNTXG | dual inverting | | WDFN8 (Pb-Free) | 3000 / Tape & Reel |
| NCP81071BMNTXG | dual non inverting | | | |
| NCP81071CMNTXG | One inverting one non inverting | | | |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

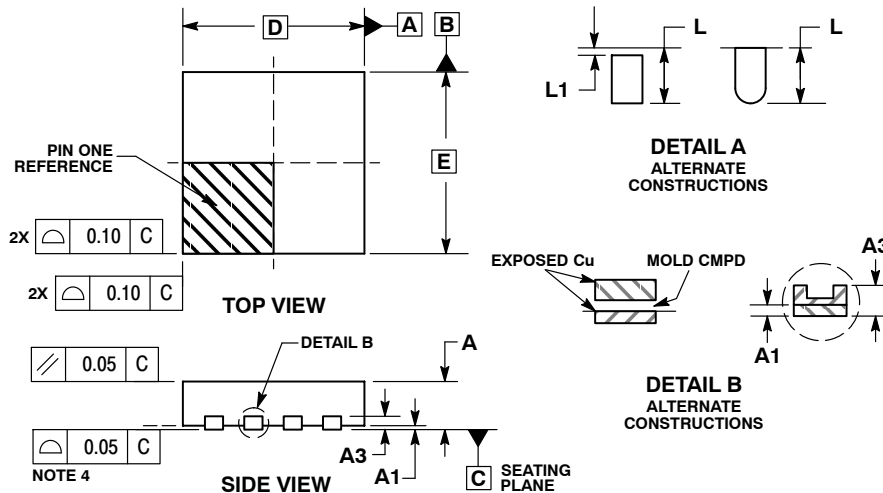
ON Semiconductor®



SCALE 2:1

WDFN8 3x3, 0.65P
CASE 511CD
ISSUE O

DATE 29 APR 2014

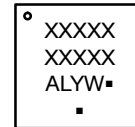


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| DIM | MILLIMETERS | |
|-----|-------------|------|
| | MIN | MAX |
| A | 0.70 | 0.80 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 REF | |
| b | 0.25 | 0.35 |
| D | 3.00 BSC | |
| D2 | 2.05 | 2.25 |
| E | 3.00 BSC | |
| E2 | 1.10 | 1.30 |
| e | 0.65 BSC | |
| K | 0.20 | --- |
| L | 0.30 | 0.50 |
| L1 | 0.00 | 0.15 |

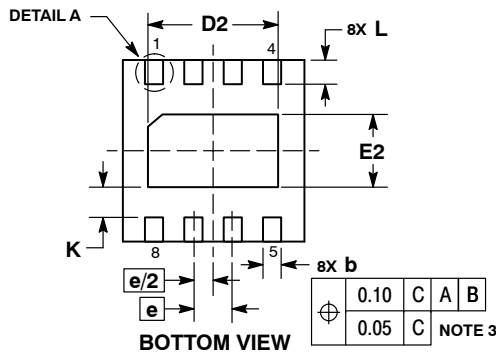
GENERIC MARKING DIAGRAM*



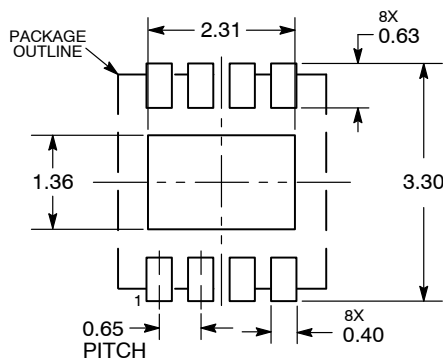
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.



RECOMMENDED SOLDERING FOOTPRINT*

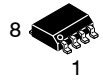


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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| DESCRIPTION: | WDFN8, 3X3, 0.65P | PAGE 1 OF 1 |

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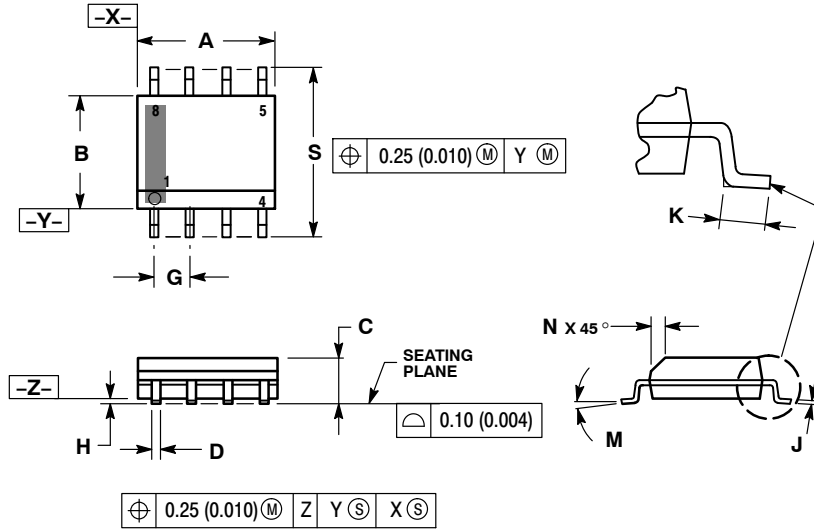
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-8 NB
CASE 751-07
ISSUE AK

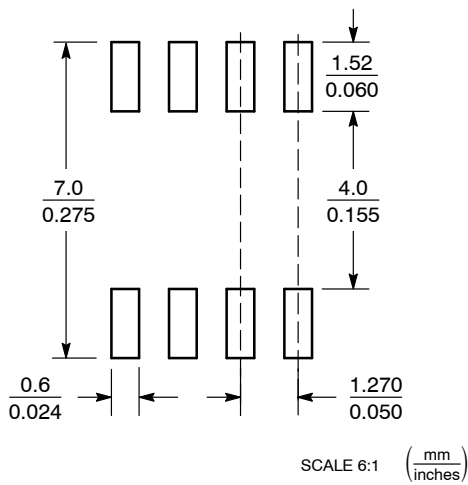
DATE 16 FEB 2011



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

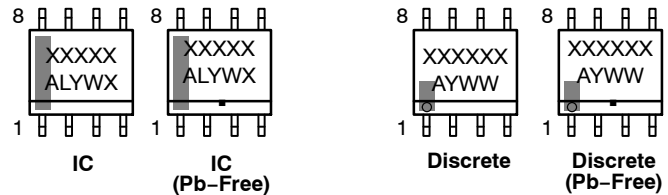
| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.80 | 5.00 | 0.189 | 0.197 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.053 | 0.069 |
| D | 0.33 | 0.51 | 0.013 | 0.020 |
| G | 1.27 BSC | | 0.050 BSC | |
| H | 0.10 | 0.25 | 0.004 | 0.010 |
| J | 0.19 | 0.25 | 0.007 | 0.010 |
| K | 0.40 | 1.27 | 0.016 | 0.050 |
| M | 0° | 8° | 0° | 8° |
| N | 0.25 | 0.50 | 0.010 | 0.020 |
| S | 5.80 | 6.20 | 0.228 | 0.244 |

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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SOIC-8 NB
CASE 751-07
ISSUE AK

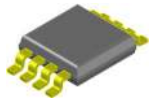
DATE 16 FEB 2011

- | | | | |
|---|--|--|--|
| <p>STYLE 1: PIN 1. EMITTER 2. COLLECTOR 3. COLLECTOR 4. EMITTER 5. EMITTER 6. BASE 7. BASE 8. EMITTER</p> | <p>STYLE 2: PIN 1. COLLECTOR, DIE, #1 2. COLLECTOR, #1 3. COLLECTOR, #2 4. COLLECTOR, #2 5. BASE, #2 6. EMITTER, #2 7. BASE, #1 8. EMITTER, #1</p> | <p>STYLE 3: PIN 1. DRAIN, DIE #1 2. DRAIN, #1 3. DRAIN, #2 4. DRAIN, #2 5. GATE, #2 6. SOURCE, #2 7. GATE, #1 8. SOURCE, #1</p> | <p>STYLE 4: PIN 1. ANODE 2. ANODE 3. ANODE 4. ANODE 5. ANODE 6. ANODE 7. ANODE 8. COMMON CATHODE</p> |
| <p>STYLE 5: PIN 1. DRAIN 2. DRAIN 3. DRAIN 4. DRAIN 5. GATE 6. GATE 7. SOURCE 8. SOURCE</p> | <p>STYLE 6: PIN 1. SOURCE 2. DRAIN 3. DRAIN 4. SOURCE 5. SOURCE 6. GATE 7. GATE 8. SOURCE</p> | <p>STYLE 7: PIN 1. INPUT 2. EXTERNAL BYPASS 3. THIRD STAGE SOURCE 4. GROUND 5. DRAIN 6. GATE 3 7. SECOND STAGE Vd 8. FIRST STAGE Vd</p> | <p>STYLE 8: PIN 1. COLLECTOR, DIE #1 2. BASE, #1 3. BASE, #2 4. COLLECTOR, #2 5. COLLECTOR, #2 6. EMITTER, #2 7. EMITTER, #1 8. COLLECTOR, #1</p> |
| <p>STYLE 9: PIN 1. EMITTER, COMMON 2. COLLECTOR, DIE #1 3. COLLECTOR, DIE #2 4. EMITTER, COMMON 5. EMITTER, COMMON 6. BASE, DIE #2 7. BASE, DIE #1 8. EMITTER, COMMON</p> | <p>STYLE 10: PIN 1. GROUND 2. BIAS 1 3. OUTPUT 4. GROUND 5. GROUND 6. BIAS 2 7. INPUT 8. GROUND</p> | <p>STYLE 11: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. DRAIN 2 7. DRAIN 1 8. DRAIN 1</p> | <p>STYLE 12: PIN 1. SOURCE 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN</p> |
| <p>STYLE 13: PIN 1. N.C. 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN</p> | <p>STYLE 14: PIN 1. N-SOURCE 2. N-GATE 3. P-SOURCE 4. P-GATE 5. P-DRAIN 6. P-DRAIN 7. N-DRAIN 8. N-DRAIN</p> | <p>STYLE 15: PIN 1. ANODE 1 2. ANODE 1 3. ANODE 1 4. ANODE 1 5. CATHODE, COMMON 6. CATHODE, COMMON 7. CATHODE, COMMON 8. CATHODE, COMMON</p> | <p>STYLE 16: PIN 1. EMITTER, DIE #1 2. BASE, DIE #1 3. EMITTER, DIE #2 4. BASE, DIE #2 5. COLLECTOR, DIE #2 6. COLLECTOR, DIE #2 7. COLLECTOR, DIE #1 8. COLLECTOR, DIE #1</p> |
| <p>STYLE 17: PIN 1. VCC 2. V2OUT 3. V1OUT 4. TXE 5. RXE 6. VEE 7. GND 8. ACC</p> | <p>STYLE 18: PIN 1. ANODE 2. ANODE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. CATHODE 8. CATHODE</p> | <p>STYLE 19: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. MIRROR 2 7. DRAIN 1 8. MIRROR 1</p> | <p>STYLE 20: PIN 1. SOURCE (N) 2. GATE (N) 3. SOURCE (P) 4. GATE (P) 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN</p> |
| <p>STYLE 21: PIN 1. CATHODE 1 2. CATHODE 2 3. CATHODE 3 4. CATHODE 4 5. CATHODE 5 6. COMMON ANODE 7. COMMON ANODE 8. CATHODE 6</p> | <p>STYLE 22: PIN 1. I/O LINE 1 2. COMMON CATHODE/VCC 3. COMMON CATHODE/VCC 4. I/O LINE 3 5. COMMON ANODE/GND 6. I/O LINE 4 7. I/O LINE 5 8. COMMON ANODE/GND</p> | <p>STYLE 23: PIN 1. LINE 1 IN 2. COMMON ANODE/GND 3. COMMON ANODE/GND 4. LINE 2 IN 5. LINE 2 OUT 6. COMMON ANODE/GND 7. COMMON ANODE/GND 8. LINE 1 OUT</p> | <p>STYLE 24: PIN 1. BASE 2. EMITTER 3. COLLECTOR/ANODE 4. COLLECTOR/ANODE 5. CATHODE 6. CATHODE 7. COLLECTOR/ANODE 8. COLLECTOR/ANODE</p> |
| <p>STYLE 25: PIN 1. VIN 2. N/C 3. REXT 4. GND 5. IOUT 6. IOUT 7. IOUT 8. IOUT</p> | <p>STYLE 26: PIN 1. GND 2. dv/dt 3. ENABLE 4. ILIMIT 5. SOURCE 6. SOURCE 7. SOURCE 8. VCC</p> | <p>STYLE 27: PIN 1. ILIMIT 2. OVLO 3. UVLO 4. INPUT+ 5. SOURCE 6. SOURCE 7. SOURCE 8. DRAIN</p> | <p>STYLE 28: PIN 1. SW_TO_GND 2. DASIC_OFF 3. DASIC_SW_DET 4. GND 5. V_MON 6. VBULK 7. VBULK 8. VIN</p> |
| <p>STYLE 29: PIN 1. BASE, DIE #1 2. EMITTER, #1 3. BASE, #2 4. EMITTER, #2 5. COLLECTOR, #2 6. COLLECTOR, #2 7. COLLECTOR, #1 8. COLLECTOR, #1</p> | <p>STYLE 30: PIN 1. DRAIN 1 2. DRAIN 1 3. GATE 2 4. SOURCE 2 5. SOURCE 1/DRAIN 2 6. SOURCE 1/DRAIN 2 7. SOURCE 1/DRAIN 2 8. GATE 1</p> | | |

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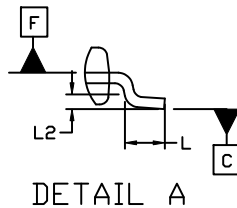
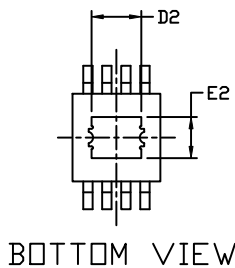
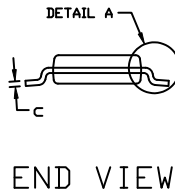
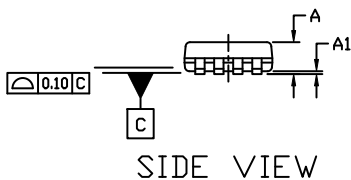
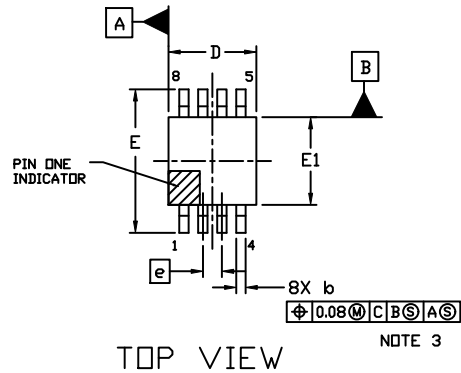
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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



MSOP8 EP, 3x3 CASE 846AM ISSUE B

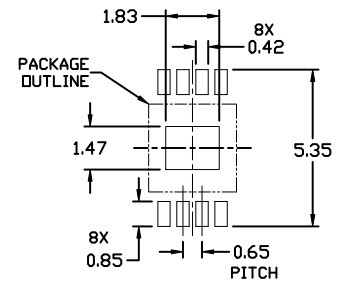
DATE 07 JAN 2022



NOTES:

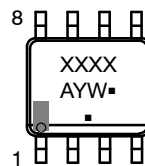
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION *b* DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSION *D* DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION *E* DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS *D* AND *E* ARE DETERMINED AT DATUM *F*.
5. DATUMS *A* AND *B* ARE TO BE DETERMINED AT DATUM *F*.
6. *A1* IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

| DIM | MILLIMETERS | |
|-----------|-------------|------|
| | MIN. | MAX. |
| A | --- | 1.10 |
| A1 | 0.05 | 0.15 |
| <i>b</i> | 0.25 | 0.40 |
| <i>c</i> | 0.13 | 0.23 |
| <i>D</i> | 2.90 | 3.10 |
| <i>D2</i> | 1.73 | 1.83 |
| <i>E</i> | 4.75 | 5.05 |
| <i>E1</i> | 2.90 | 3.10 |
| <i>E2</i> | 1.37 | 1.47 |
| <i>e</i> | 0.65 BSC | |
| <i>L</i> | 0.40 | 0.70 |
| <i>L2</i> | 0.254 BSC | |



* FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

GENERIC MARKING DIAGRAM*



- XXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)
*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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