



PMXB360ENEA

80 V, N-channel Trench MOSFET

5 July 2018

Product data sheet

1. General description

N-channel enhancement mode Field-Effect Transistor (FET) in a leadless ultra small DFN1010D-3 (SOT1215) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Logic-level compatible
- Leadless ultra small and ultra thin SMD plastic package: $1.1 \times 1.0 \times 0.37$ mm
- Tin-plated 100 % solderable side pads for optical solder inspection
- ElectroStatic Discharge (ESD) protection > 2 kV HBM
- AEC-Q101 qualified

3. Applications

- Relay driver
- Power management in automotive and industrial applications
- LED driver
- DC-to-DC converter

4. Quick reference data

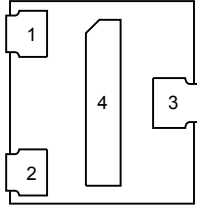
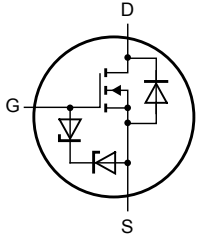
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$	-	-	80	V
V_{GS}	gate-source voltage		-20	-	20	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	1.1	A
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 1.1\text{ A}; T_j = 25\text{ °C}$	-	345	450	m Ω

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm^2 .

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>Transparent top view DFN1010D-3 (SOT1215)</p>	 <p>017aaa255</p>
2	S	source		
3	D	drain		
4	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMXB360ENEA	DFN1010D-3	DFN1010D-3: plastic thermal enhanced ultra thin small outline package; no leads; 3 terminals; body 1.1 x 1.0 x 0.37 mm	SOT1215

7. Marking

Table 4. Marking codes

Type number	Marking code
PMXB360ENEA	11 10 10

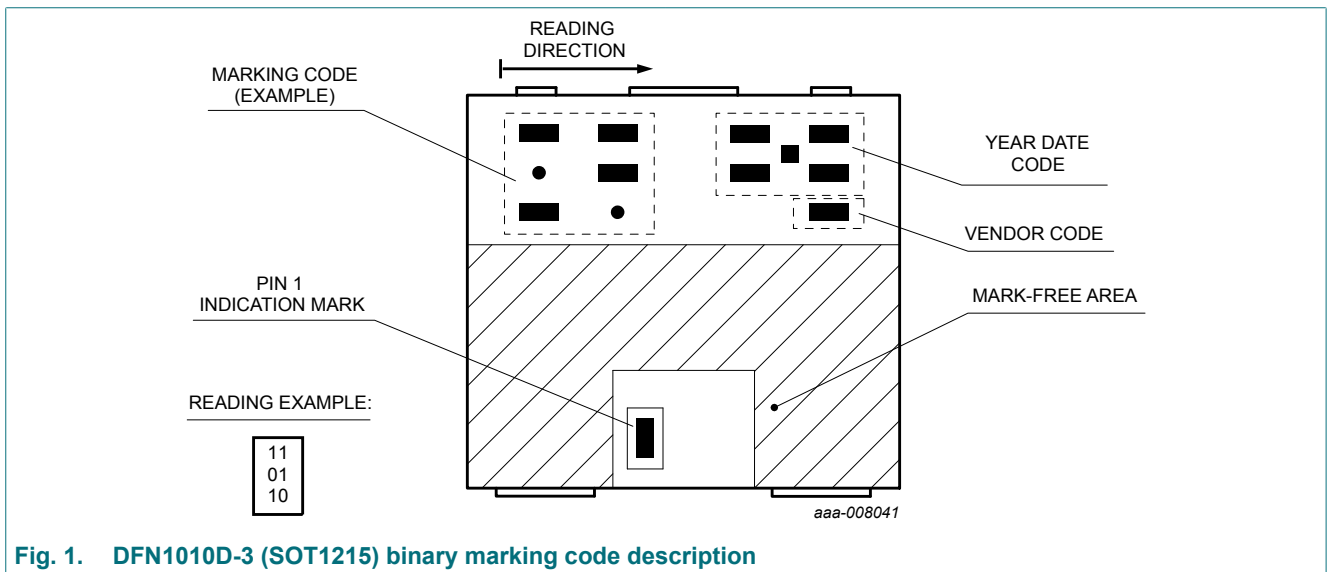


Fig. 1. DFN1010D-3 (SOT1215) binary marking code description

8. Limiting values

Table 5. Limiting values

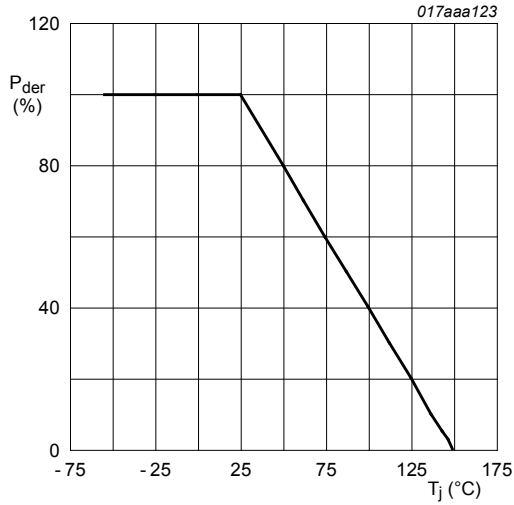
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$		-	80	V
V_{GS}	gate-source voltage			-20	20	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	1.1	A
		$V_{GS} = 10\text{ V}; T_{amb} = 100\text{ °C}$	[1]	-	0.7	A
I_{DM}	peak drain current	$T_{amb} = 25\text{ °C}$; single pulse; $t_p \leq 10\text{ }\mu\text{s}$		-	4.4	A
P_{tot}	total power dissipation	$T_{amb} = 25\text{ °C}$	[2]	-	400	mW
			[1]	-	1070	mW
		$T_{sp} = 25\text{ °C}$		-	6250	mW
T_j	junction temperature			-55	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C
Source-drain diode						
I_S	source current	$T_{amb} = 25\text{ °C}$	[1]	-	0.8	A
ESD maximum rating						
V_{ESD}	electrostatic discharge voltage	HBM	[3]	-	2000	V
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$T_{j(\text{init})} = 25\text{ °C}$; $I_D = 0.17\text{ A}$; DUT in avalanche (unclamped)		-	7.1	mJ

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm^2 .

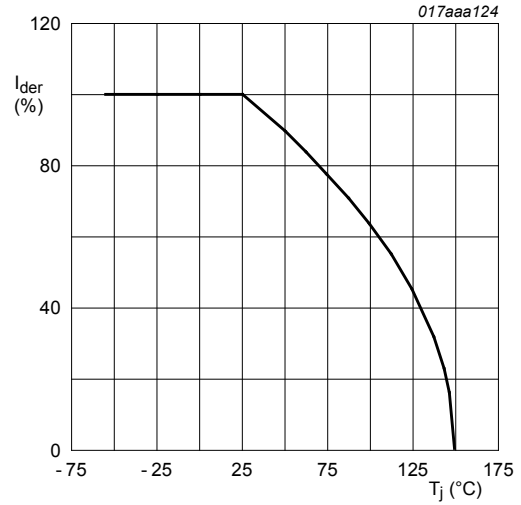
[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

[3] Measured between all pins.



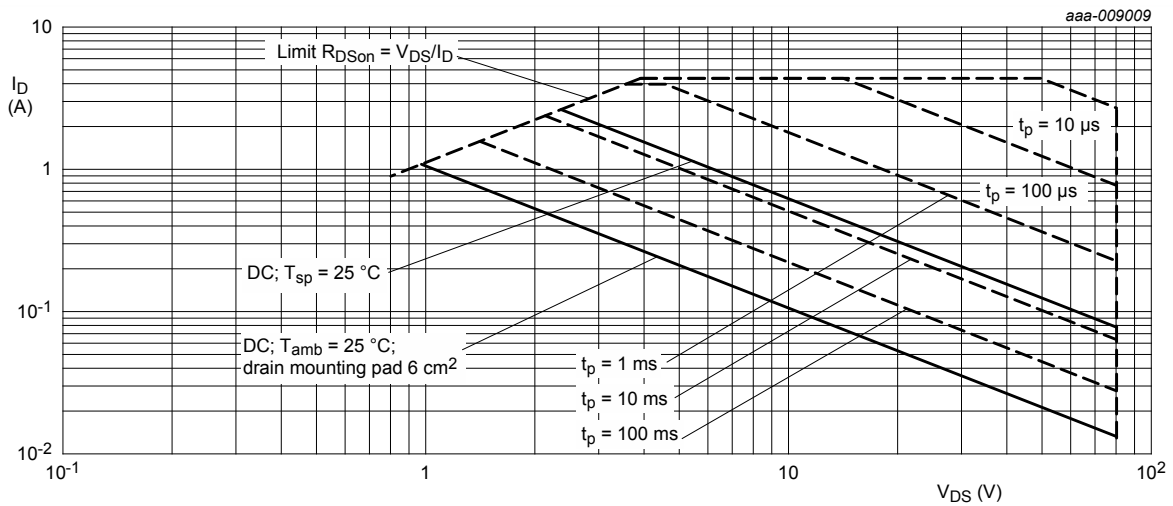
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100 \%$$

Fig. 2. Normalized total power dissipation as a function of junction temperature



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100 \%$$

Fig. 3. Normalized continuous drain current as a function of junction temperature



I_{DM} = single pulse

Fig. 4. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

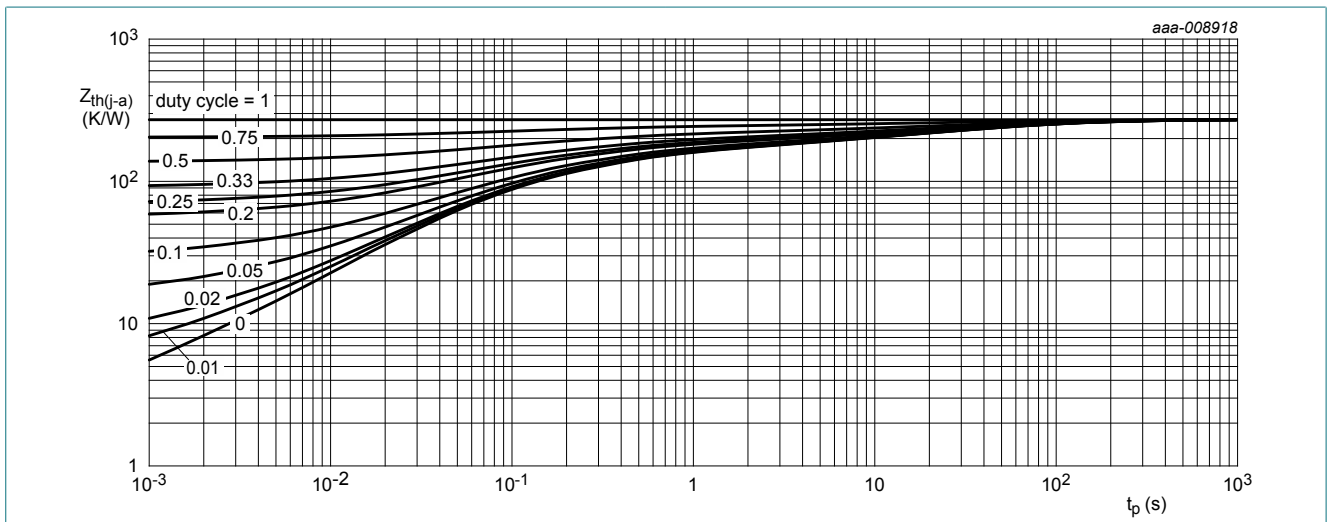
9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	271	312	K/W
			[2]	-	102	117	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	15	20	K/W

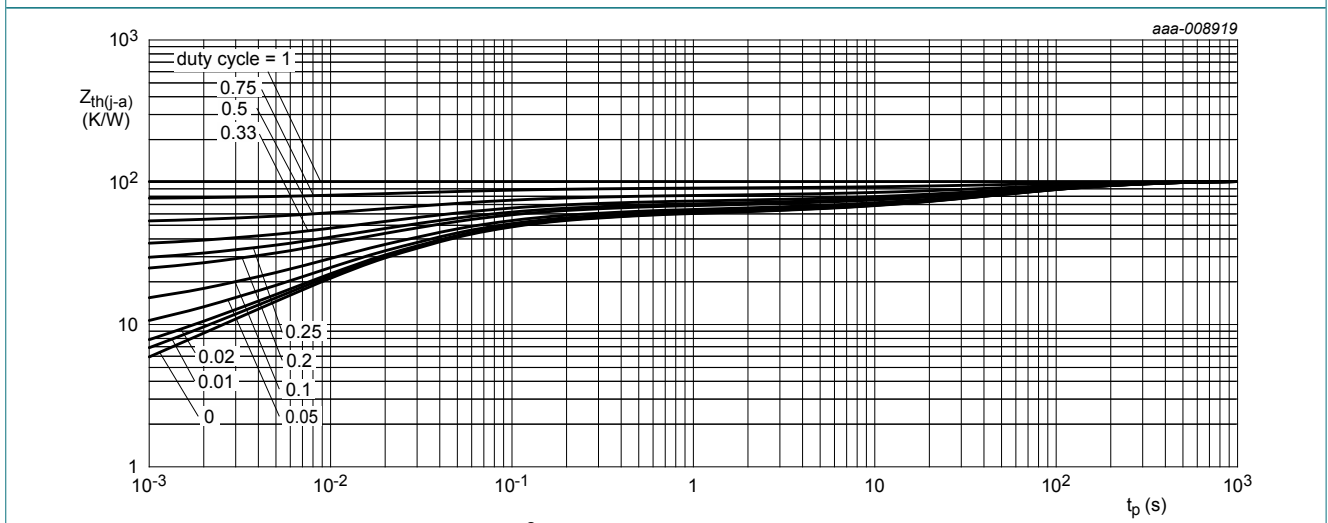
[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm².



FR4 PCB, standard footprint

Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, mounting pad for drain 6 cm²

Fig. 6. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A$; $V_{GS} = 0 V$; $T_j = 25 \text{ }^\circ C$	80	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = 250 \mu A$; $V_{DS} = V_{GS}$; $T_j = 25 \text{ }^\circ C$	1.3	1.7	2.7	V
I_{DSS}	drain leakage current	$V_{DS} = 80 V$; $V_{GS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	-	1	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 V$; $V_{DS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	-	15	μA
		$V_{GS} = -20 V$; $V_{DS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	-	-15	μA
		$V_{GS} = 10 V$; $V_{DS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	-	1	μA
		$V_{GS} = -10 V$; $V_{DS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	-	-1	μA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10 V$; $I_D = 1.1 A$; $T_j = 25 \text{ }^\circ C$	-	345	450	m Ω
		$V_{GS} = 10 V$; $I_D = 1.1 A$; $T_j = 150 \text{ }^\circ C$	-	660	887	m Ω
		$V_{GS} = 4.5 V$; $I_D = 1 A$; $T_j = 25 \text{ }^\circ C$	-	390	540	m Ω
g_{fs}	forward transconductance	$V_{DS} = 10 V$; $I_D = 1.1 A$; $T_j = 25 \text{ }^\circ C$	-	3.2	-	S
R_G	gate resistance	$f = 1 \text{ MHz}$; $T_j = 25 \text{ }^\circ C$	-	13	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$V_{DS} = 40 V$; $I_D = 1.1 A$; $V_{GS} = 10 V$; $T_j = 25 \text{ }^\circ C$	-	3	4.5	nC
Q_{GS}	gate-source charge		-	0.4	-	nC
Q_{GD}	gate-drain charge		-	0.6	-	nC
C_{iss}	input capacitance	$V_{DS} = 40 V$; $f = 1 \text{ MHz}$; $V_{GS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	130	-	pF
C_{oss}	output capacitance		-	20	-	pF
C_{rss}	reverse transfer capacitance		-	11	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 40 V$; $I_D = 1.1 A$; $V_{GS} = 10 V$; $R_{G(ext)} = 6 \Omega$; $T_j = 25 \text{ }^\circ C$	-	2	-	ns
t_r	rise time		-	3.5	-	ns
$t_{d(off)}$	turn-off delay time		-	9	-	ns
t_f	fall time		-	3	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 0.8 A$; $V_{GS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	0.8	1.2	V

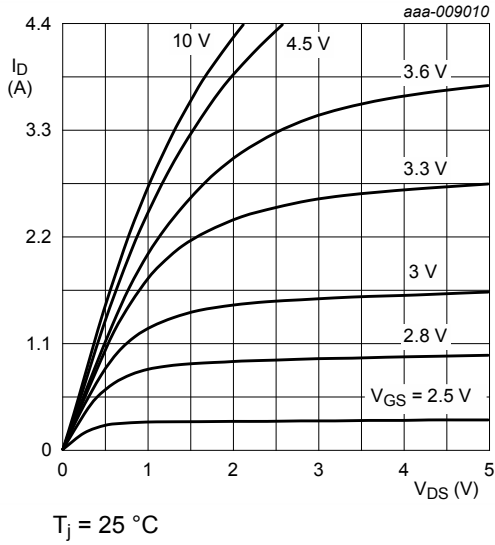


Fig. 7. Output characteristics: drain current as a function of drain-source voltage; typical values

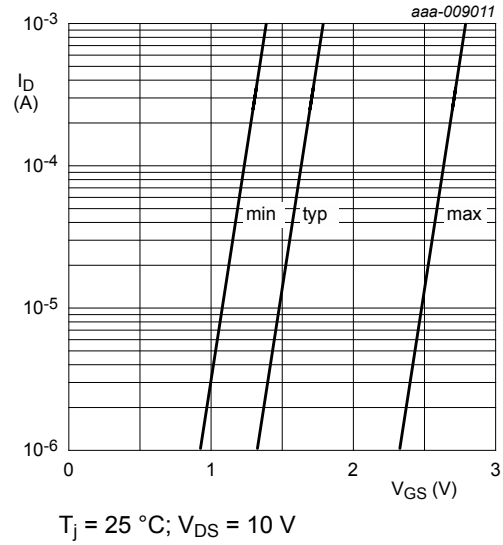


Fig. 8. Sub-threshold drain current as a function of gate-source voltage

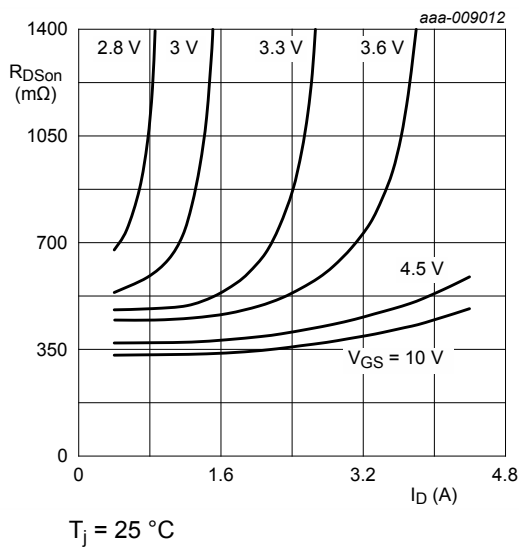


Fig. 9. Drain-source on-state resistance as a function of drain current; typical values

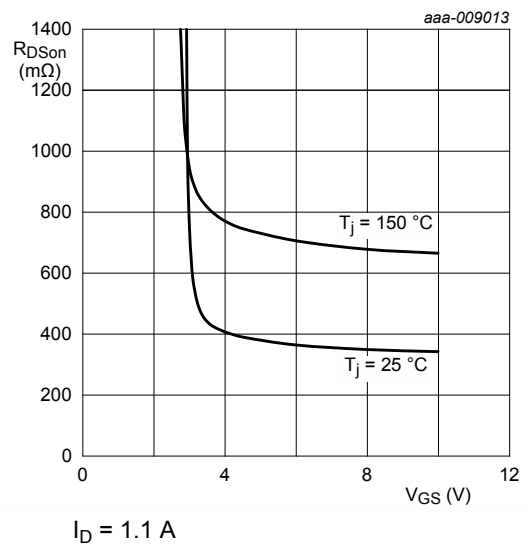
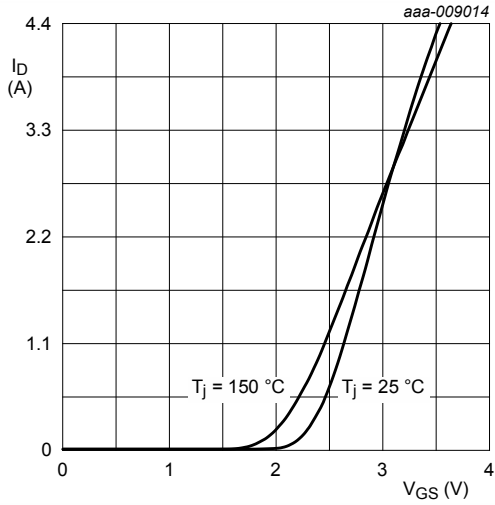
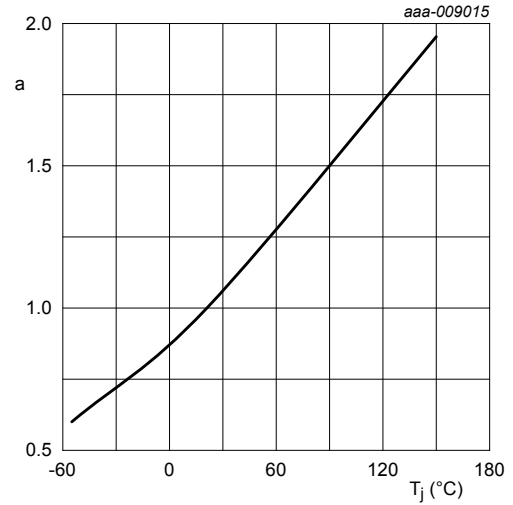


Fig. 10. Drain-source on-state resistance as a function of gate-source voltage; typical values



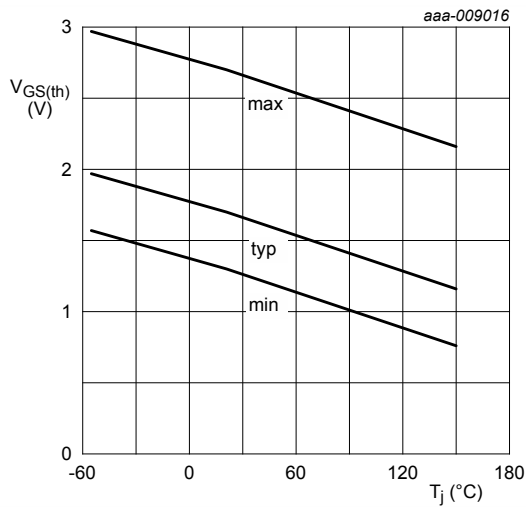
$$V_{DS} > I_D \times R_{DSon}$$

Fig. 11. Transfer characteristics: drain current as a function of gate-source voltage; typical values



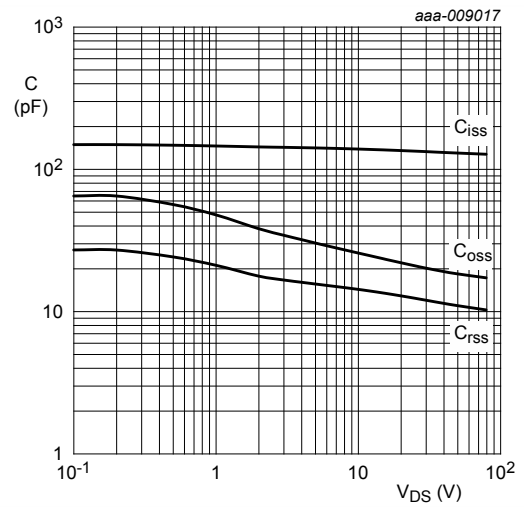
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ C)}}$$

Fig. 12. Normalized drain-source on-state resistance as a function of junction temperature; typical values



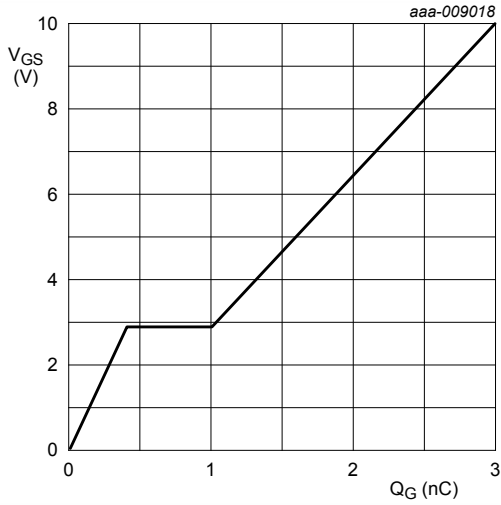
$$I_D = 0.25 \text{ mA}; V_{DS} = V_{GS}$$

Fig. 13. Gate-source threshold voltage as a function of junction temperature



$$f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}$$

Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$I_D = 1.1 \text{ A}; V_{DS} = 40 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}$

Fig. 15. Gate-source voltage as a function of gate charge; typical values

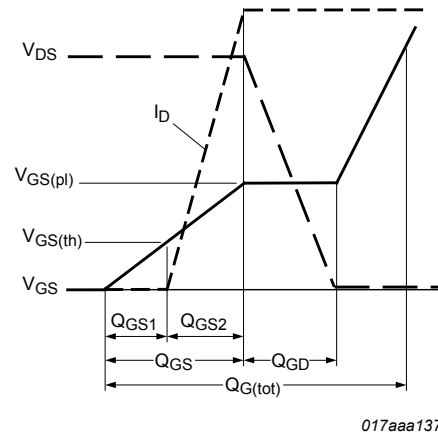
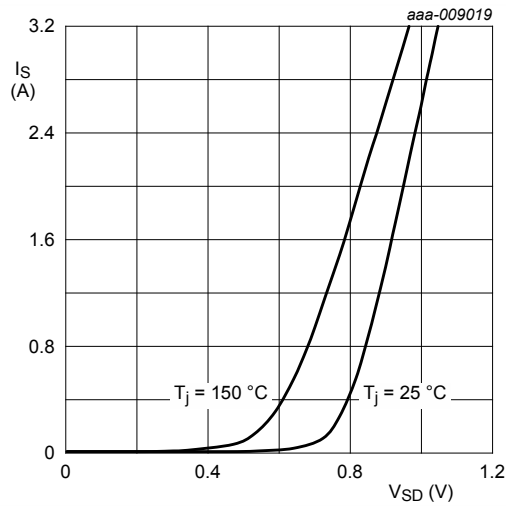


Fig. 16. MOSFET transistor: Gate charge waveform definitions



$V_{GS} = 0 \text{ V}$

Fig. 17. Source current as a function of source-drain voltage; typical values

11. Test information

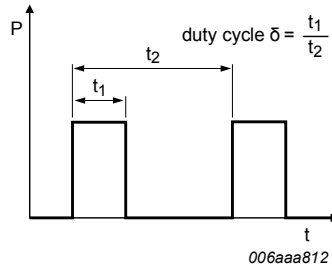


Fig. 18. Duty cycle definition

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

12. Package outline

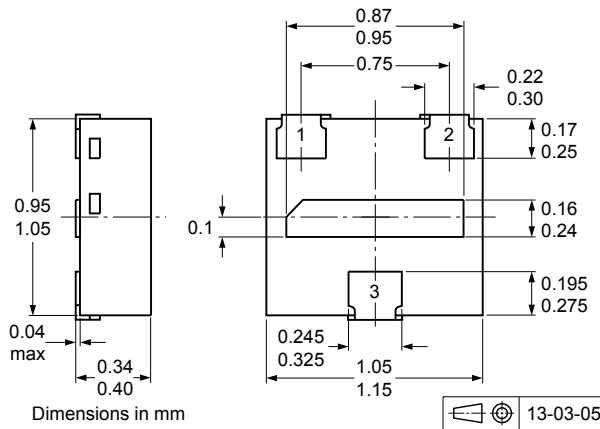


Fig. 19. Package outline DFN1010D-3 (SOT1215)

13. Soldering

Footprint information for reflow soldering of DFN1010D-3 package

SOT1215

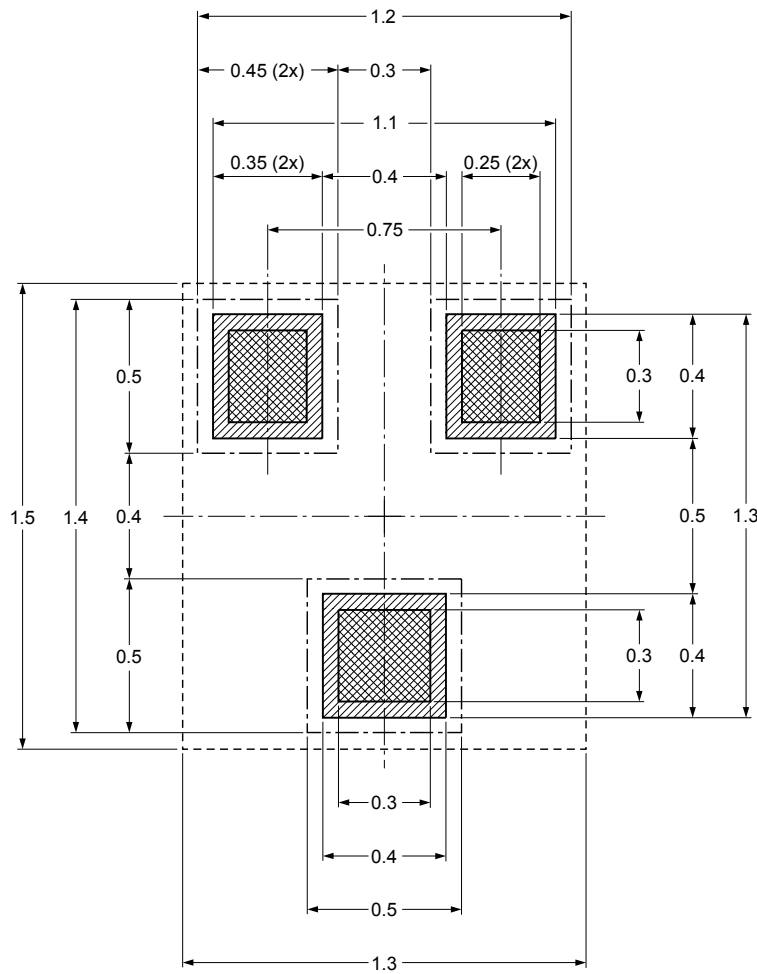


Fig. 20. Reflow soldering footprint for DFN1010D-3 (SOT1215)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMXB360ENEA v.2	20180705	Product data sheet	-	PMXB360ENEA v.1
Modification:	<ul style="list-style-type: none">Gate resistance changed to R_G 13 Ω			
PMXB360ENEA v.1	20130916	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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