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Evaluating the ADGS1212 for SPI Interface, Quad SPST Switch, Low Q_{INJ}, Low C_{ON}, ±15 V/+12 V, Mux Configurable

FEATURES

- SPI interface with error detection
- Includes CRC error detection, invalid read or write address detection, and SCLK count error detection
- Analog supply voltages
- Dual-supply: ±15 V
- Single-supply: +12 V
- PC control in conjunction with the evaluation software
- EVAL-SDP-CB1Z SDP

EVALUATION KIT CONTENTS

- EVAL-ADGS1212SDZ

EQUIPMENT NEEDED

- EVAL-SDP-CB1Z controller board
- ACE software with EVAL-ADGS1212SDZ plug in
- DC voltage source
  - ±15 V for dual-supply
  - +12 V for single-supply
- Optional digital logic supply: 3.3 V
- Analog signal source
- Method to measure voltage, such as a digital multimeter (DMM)

DOCUMENTS NEEDED

- ADGS1212 data sheet

GENERAL DESCRIPTION

The EVAL-ADGS1212SDZ is the evaluation board for the ADGS1212. The ADGS1212 is a low Q_{IN}, low C_{ON}, quad single-pole, single throw (SPST) switch controlled by a serial peripheral interface (SPI). The SPI has robust error detection features, including cyclic redundancy check (CRC) error detection, invalid read or write address detection, and serial clock (SCLK) count error detection. It is possible to daisy-chain multiple ADGS1212 devices together to enable the configuration of multiple devices with a minimal amount of digital lines. The ADGS1212 also supports burst mode that decreases the time between SPI commands.

Figure 1 shows the EVAL-ADGS1212SDZ typical evaluation board setup. The EVAL-ADGS1212SDZ is controlled by the EVAL-SDP-CB1Z system demonstration platform (SDP), which connects to a PC via a USB port. The ADGS1212 is on the center of the evaluation board and wire screw terminals are provided to connect to each of the source and drain pins. Three screw terminals power the device and, if required, a fourth terminal provides users with a defined digital logic supply voltage. Alternatively, the digital logic supply voltage can be supplied from the SDP.

Full specifications of the ADGS1212 can be found in the ADGS1212 data sheet available from Analog Devices, Inc., and should be consulted in conjunction with this user guide when using the evaluation board.

The evaluation board interfaces to the USB port of a PC via the SDP board. The EVAL-SDP-CB1Z board (SDP-B controller board) is available for order at: www.analog.com/SDP-B.

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REVISION HISTORY

9/2017—Revision 0: Initial Version

EVAL-ADGS1212SDZ EVALUATION BOARD LAYOUT

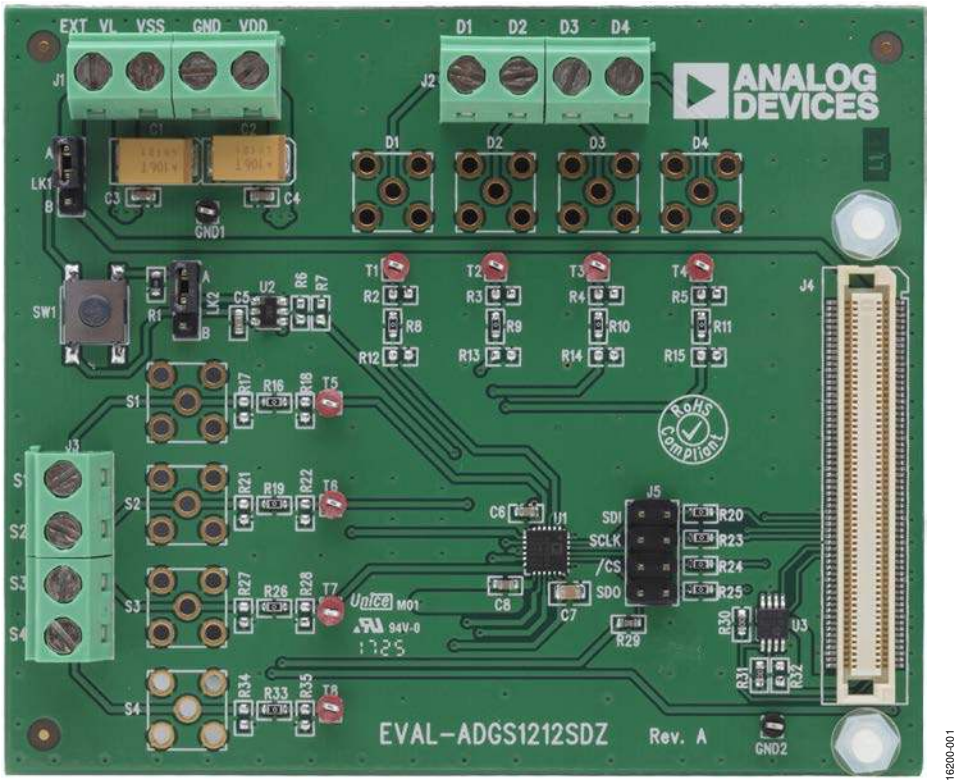

Figure 1.

EVALUATION BOARD HARDWARE

POWER SUPPLIES

Connector J1 provides access to the supply pins of the ADGS1212. VDD, GND, and VSS on J1 terminal block link to the appropriate pins on the ADGS1212. For dual-supply voltages, the evaluation board can be powered from ±15 V. For single-supply voltages, the GND and VSS terminals must connect together and power the evaluation board from 12 V. Additionally, the SDP supplies 3.3 V to the V_L pin of the ADGS1212 when Link LK1 is in Position B. When using a method other than the SDP to control the ADGS1212, supply between 2.7 V and 5.5 V to the V_L pin of the ADGS1212 via the EXT_VL screw terminal input on J1. LK1 must be in Position A.

INPUT SIGNALS

Provided are two screw connectors, J2 and J3, to connect to both the source and drain pins of the ADGS1212. Additional subminiature version B (SMB) connector pads are available if extra connections are required.

Each trace on the source and drain pins includes two sets of 0603 pads, which can place a load on the signal path to ground. A 0 Ω resistor is placed in the signal path and can be replaced with a user defined value. The resistor combined with the 0603 pads can create a simple resistor capacitor filter.

LINK OPTIONS

The EVAL-ADGS1212SDZ evaluation board provides several link options that must be set at the required operating conditions before using it. Table 1 describes the positioning of the links necessary for controlling the evaluation board via the SDP board using a PC and external power supplies. Table 2 describes the functions of these link options.

LK1 must be in Position B to avoid damaging the SDP when using it in conjunction with the EVAL-ADGS1212SDZ.

Table 1. Link Options for SDP Control (Default)

Link Number	Option
LK1	B
LK2	B

Table 2. Link Functions

Link Number	Function
LK1	This link selects the source of the V_L voltage supplied to the ADGS1212. Position A selects EXT_VL from J1. Position B selects the 3.3 V from the SDP.
LK2	This link selects how a hardware reset is performed. Position A indicates the SW1 push button can perform a hardware reset. Position B indicates the SDP can perform a hardware reset.

EVALUATION BOARD SOFTWARE

INSTALLING THE SOFTWARE

The EVAL-ADGS1212SDZ evaluation board uses the Analog Devices Analysis Control Evaluation (ACE) software. ACE is a desktop software application that facilitates the control and evaluation of multiple evaluation systems.

ACE installs the required SDP drivers and .NET Framework 4 by default. Install ACE before connecting the SDP. Find ACE software and comprehensive instructions on its installment and use at the Analog Devices website, www.analog.com/ACE.

After the installation is finished, the EVAL-ADGS1212SDZ evaluation board plug ins appear when opening ACE.

INITIAL SET UP

To set up the EVAL-ADGS1212SDZ evaluation board, complete the following steps:

1. Connect the EVAL-ADGS1212SDZ evaluation board to the SDP board and connect the SDP board to the PC via a USB cable.
2. Power the evaluation board as described in the Power Supplies section.
3. Run the ACE application. The EVAL-ADGS1212SDZ board plug ins appear in the attached hardware section of the **Start** tab.
4. Double click on the **ADGS1212SDZ Board** plug in to open the evaluation board view shown in Figure 2.
5. Double click the ADGS1212 icon in Figure 2 to access the chip block diagram. Figure 3 shows the basic functionality and main functions of the EVAL-ADGS1212SDZ evaluation board.

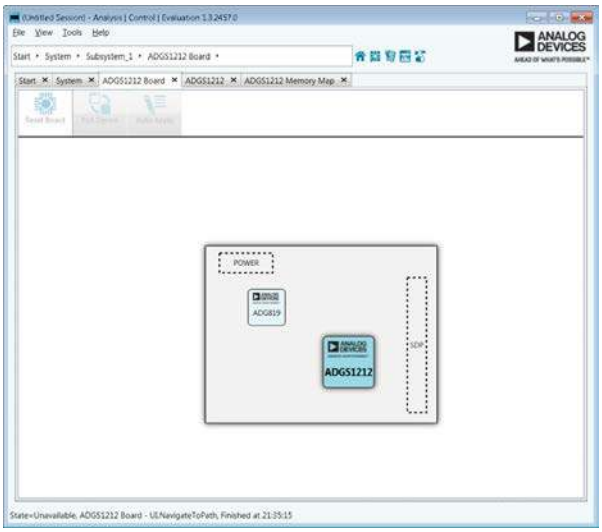

Figure 2. Evaluation Board View of the EVAL-ADGS1212SDZ

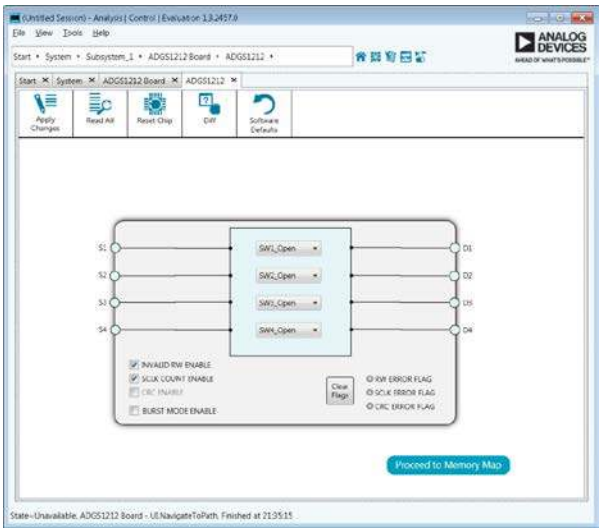

Figure 3. Chip Block Diagram View for the ADGS1212

BLOCK DIAGRAM AND DESCRIPTION

The similar appearance of the EVAL-ADGS1212SDZ software to the functional block diagram of the ADGS1212 data sheet renders it easy to correlate the board functions of the EVAL-ADGS1212SDZ with the description of the functional block diagram in the data sheet. The ADGS1212 data sheet provides comprehensive descriptions for each function, block, register, and setting.

Table 3 describes the blocks and their functions pertaining to the evaluation board. The full screen block diagram shown in Figure 4 shows the functionality of each block.

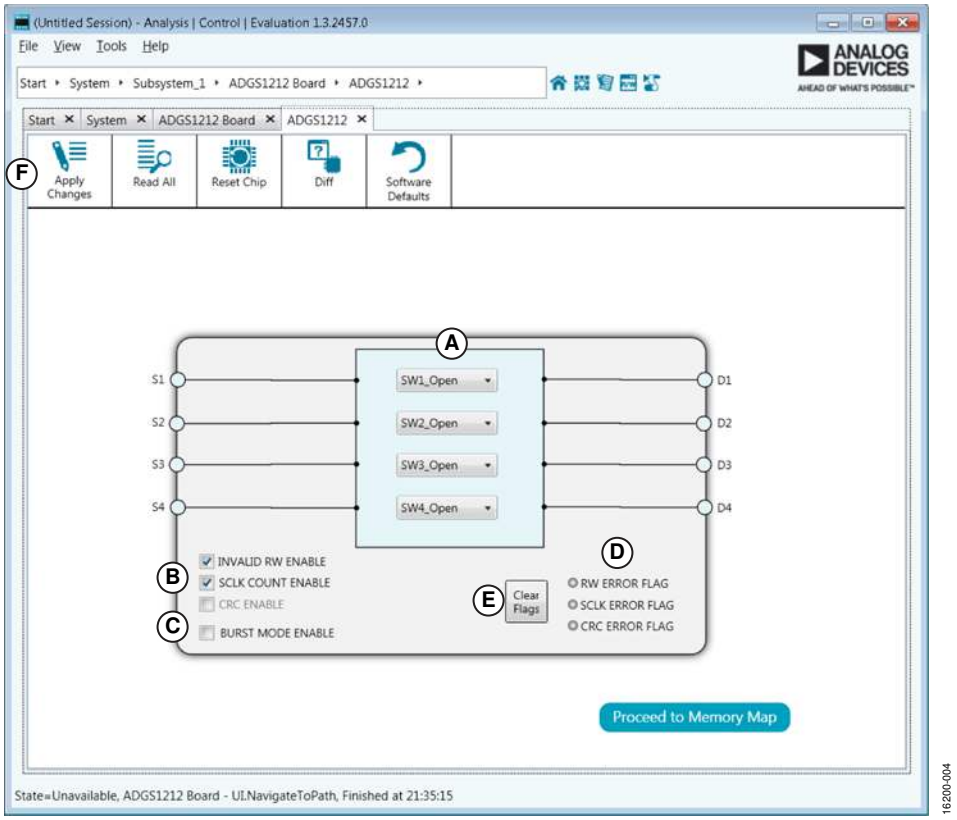

Figure 4. EVAL-ADGS1212SDZ Block Diagram with Labels

Table 3. Block Diagram Functions

Label	Function
A	The dropdown menus configure SW1 to SW4 as open or closed.
B	The **INVALID RW ENABLE**, **SCLK COUNT ENABLE**, and **CRC ENABLE** check boxes enable or disable the error detection features on the SPI interface.
C	The **BURST MODE ENABLE** check box enables or disables burst mode.
D	The **RW ERROR FLAG**, **SCLK ERROR FLAG**, and **CRC ERROR FLAG** indicators illuminate red when the relevant error flags are asserted in the error flags register.
E	The **Clear Flags** button clears the error flags register.
F	The **Apply Changes** button applies all modified values to the devices.

MEMORY MAP

From the **Memory Map** button, all registers are fully accessible and can be edited at a bit level (see Figure 5 and Figure 6). Bits shaded in dark gray are read-only bits and inaccessible from ACE. All other bits are toggled. The **Apply Changes** button transfers data modifications to the device.

All changes here correspond to the block diagram. For example, if the internal register bit is enabled, it displays as enabled on the block diagram. Bolded bits or registers represent modified values that have not been transferred to the evaluation board. After clicking **Apply Changes**, the data is transferred to the evaluation board and no longer appears as bolded.

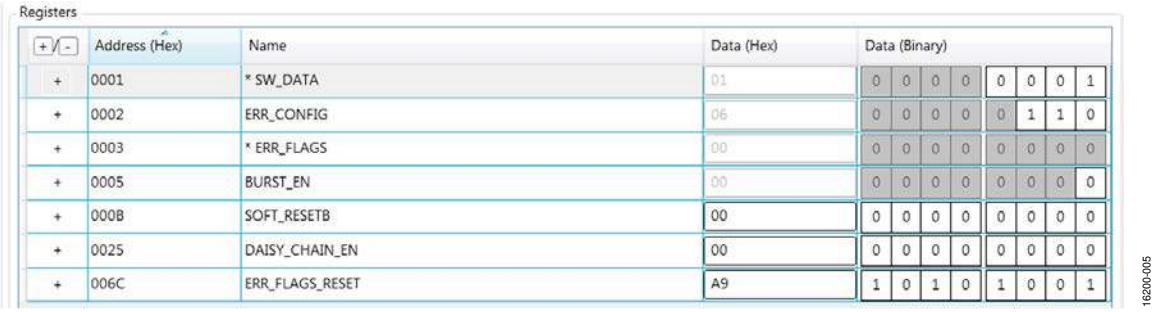

Figure 5. ADGS1212 Memory Map

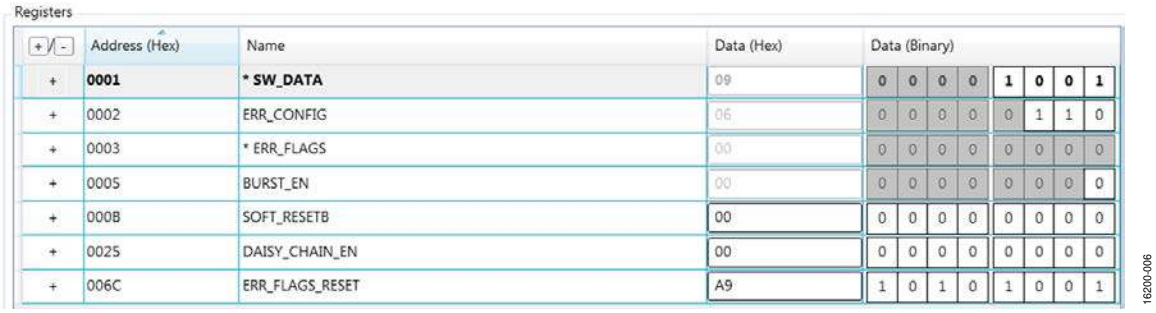

Figure 6. ADGS1212 Memory Map with Unapplied Changes in the SW_DATA Register

EVALUATION BOARD SCHEMATICS AND ARTWORK

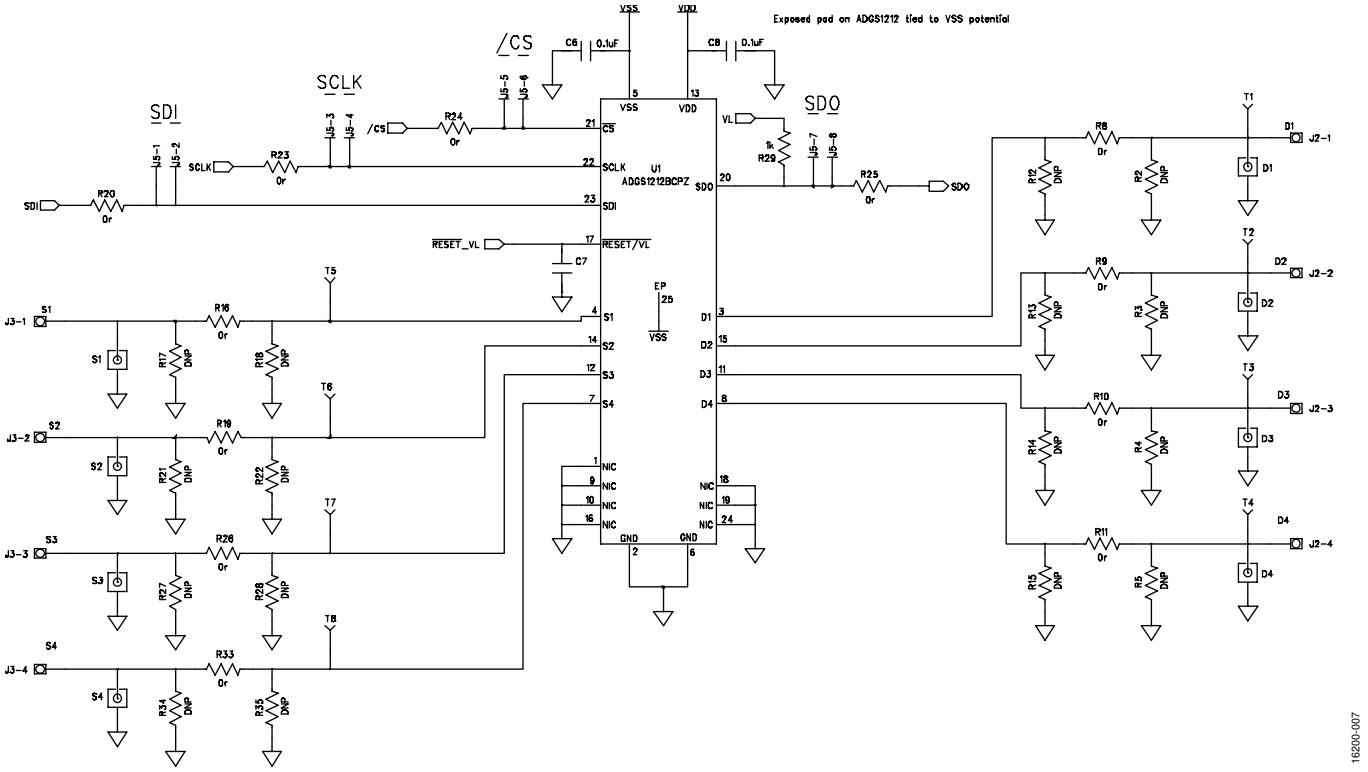

Figure 7. EVAL-ADGS1212SDZ Schematic 1

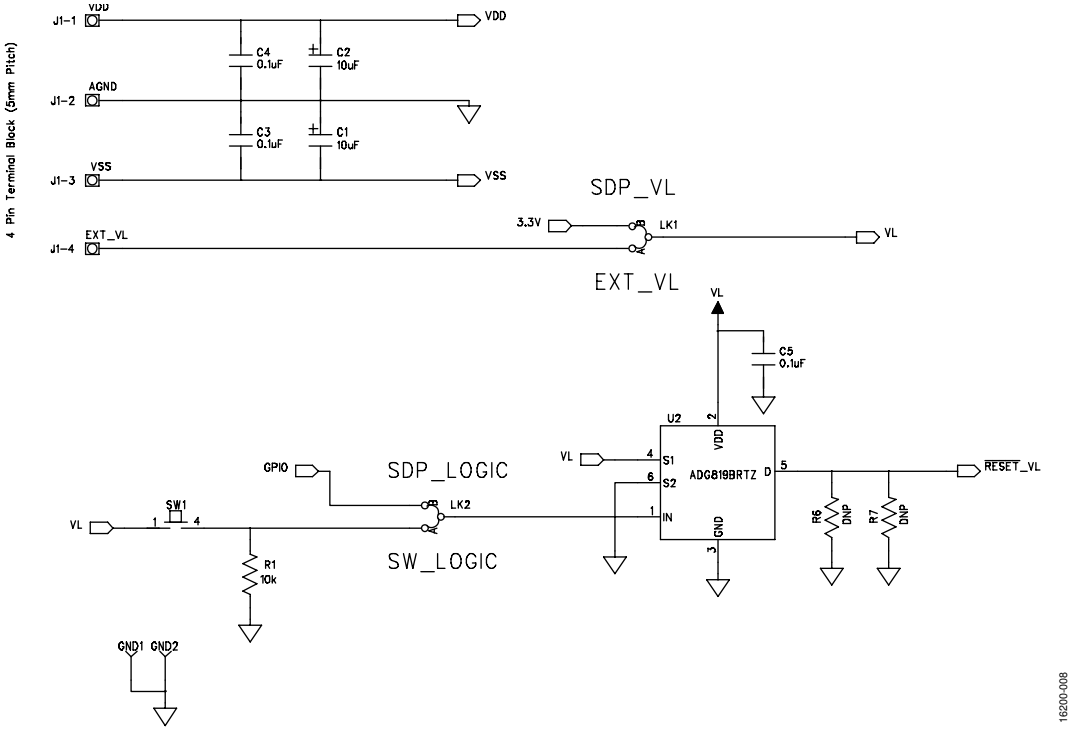

Figure 8. EVAL-ADGS1212SDZ Schematic 2

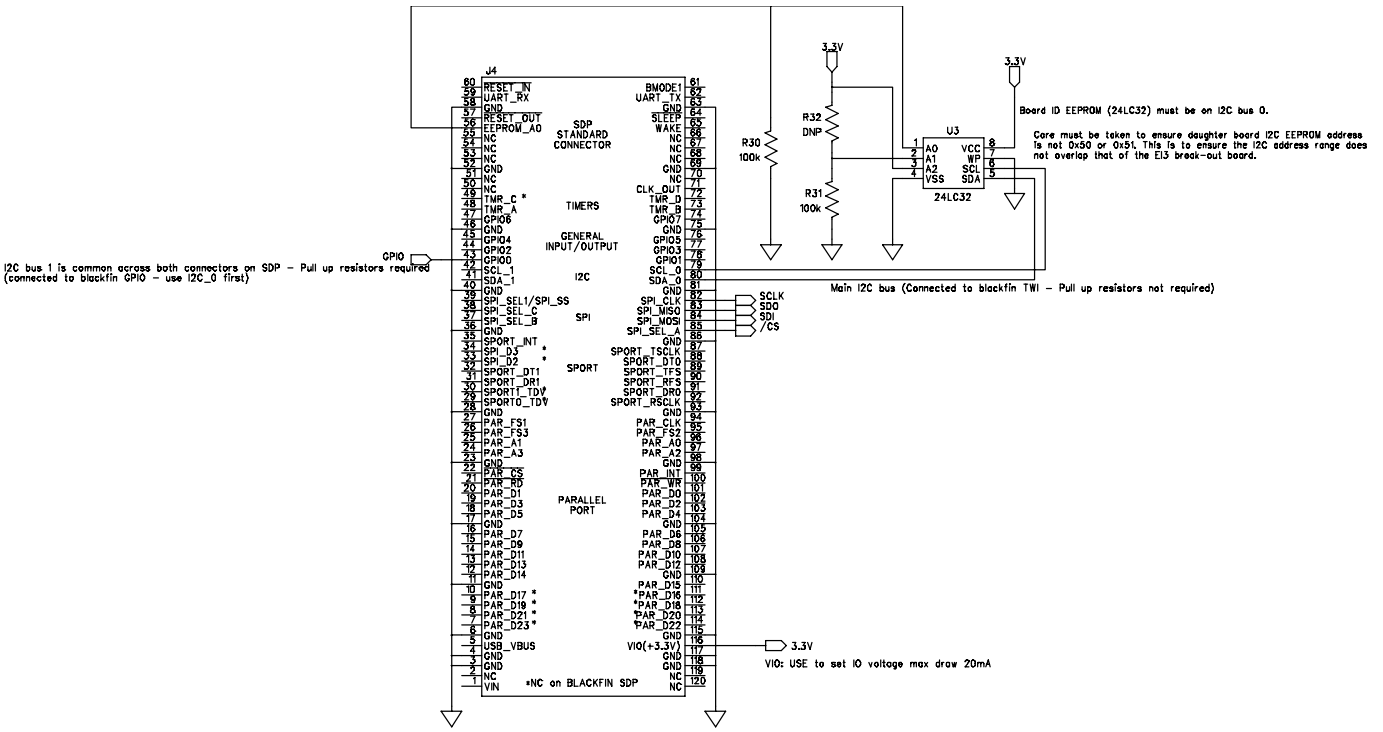

Figure 9. EVAL-ADGS1212SDZ Schematic 3

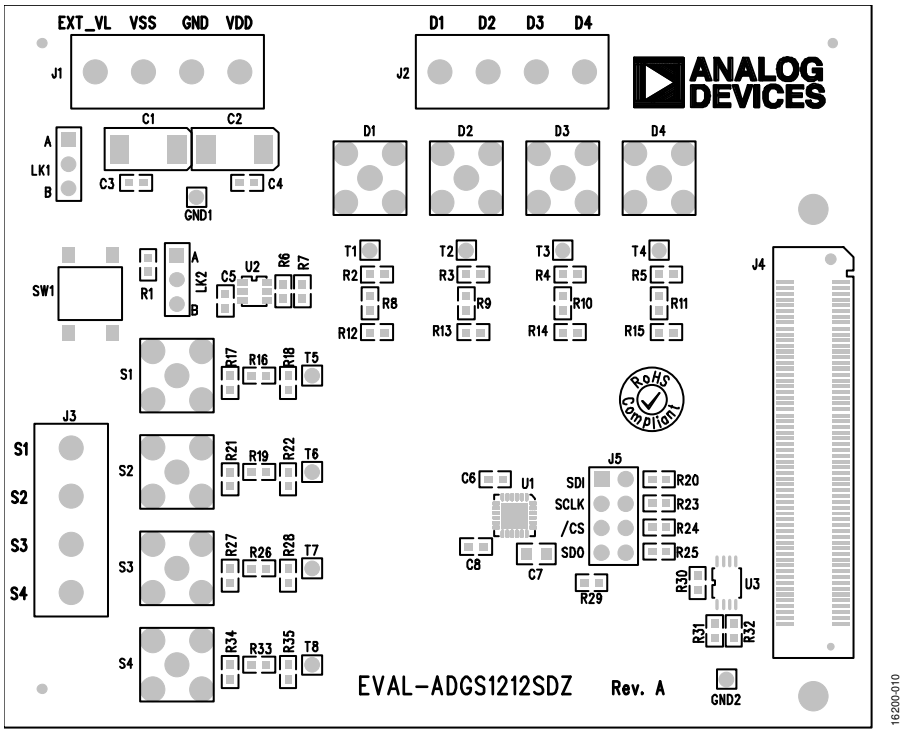

Figure 10. EVAL-ADGS1212SDZ Silk Screen

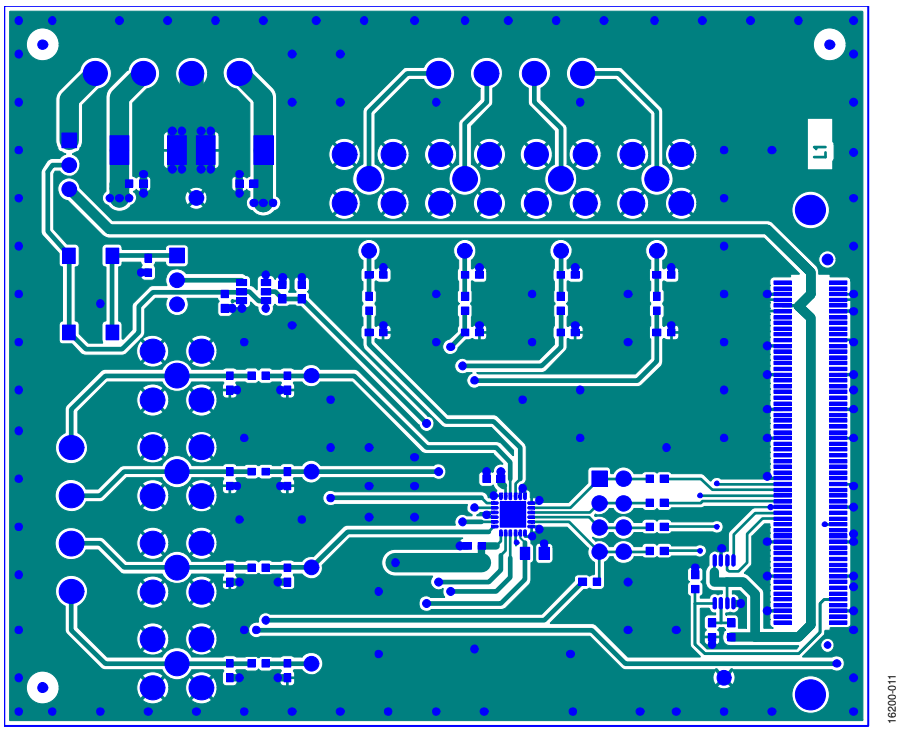

Figure 11. EVAL-ADGS1212SDZ Top Layer

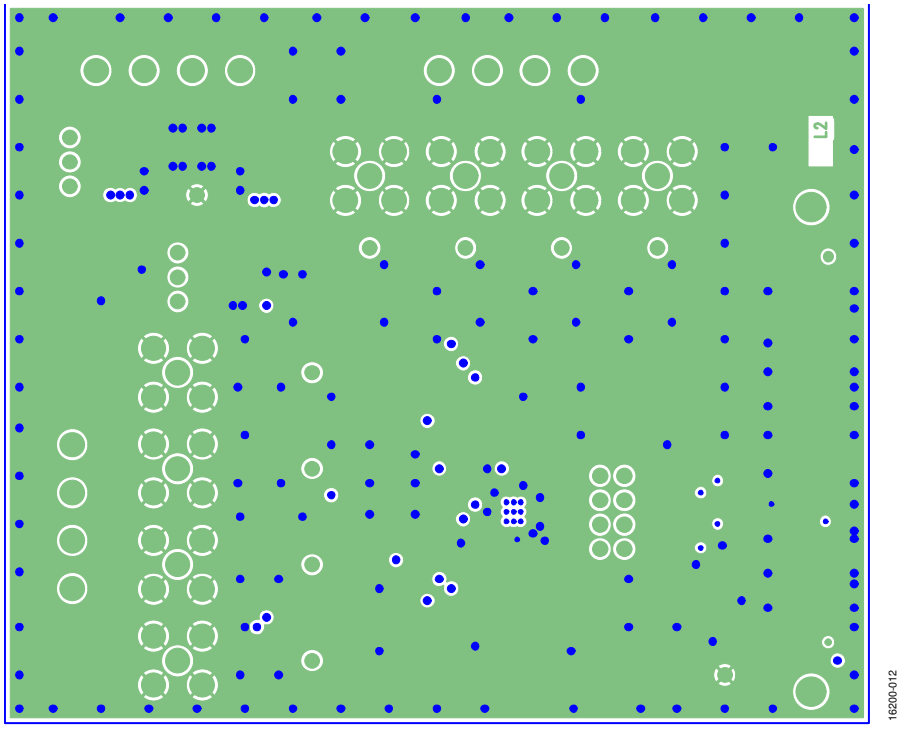

Figure 12. EVAL-ADGS1212SDZ Layer 2

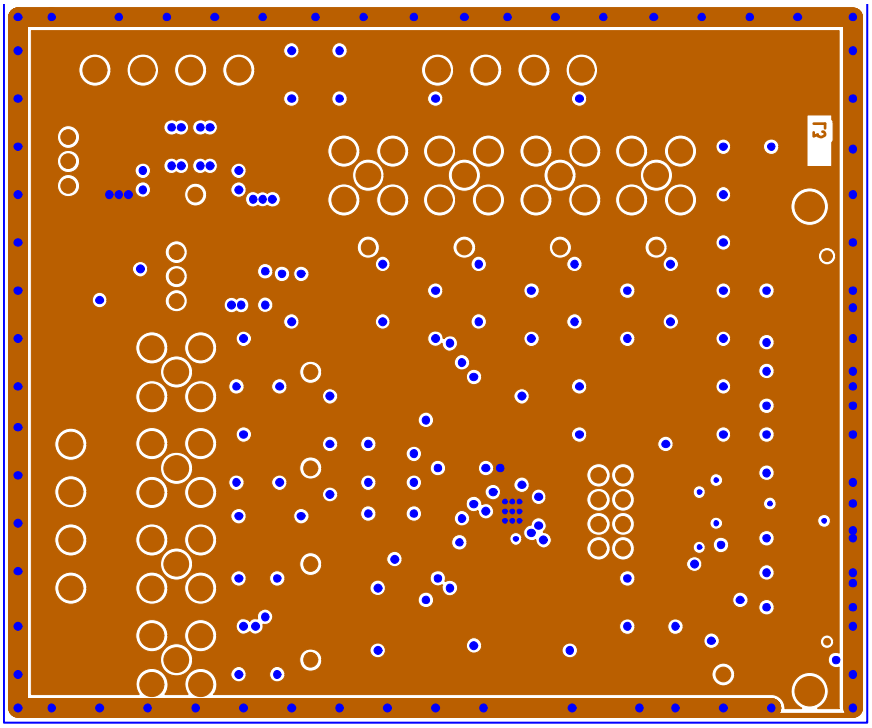

Figure 13. EVAL-ADGS1212SDZ Layer 3

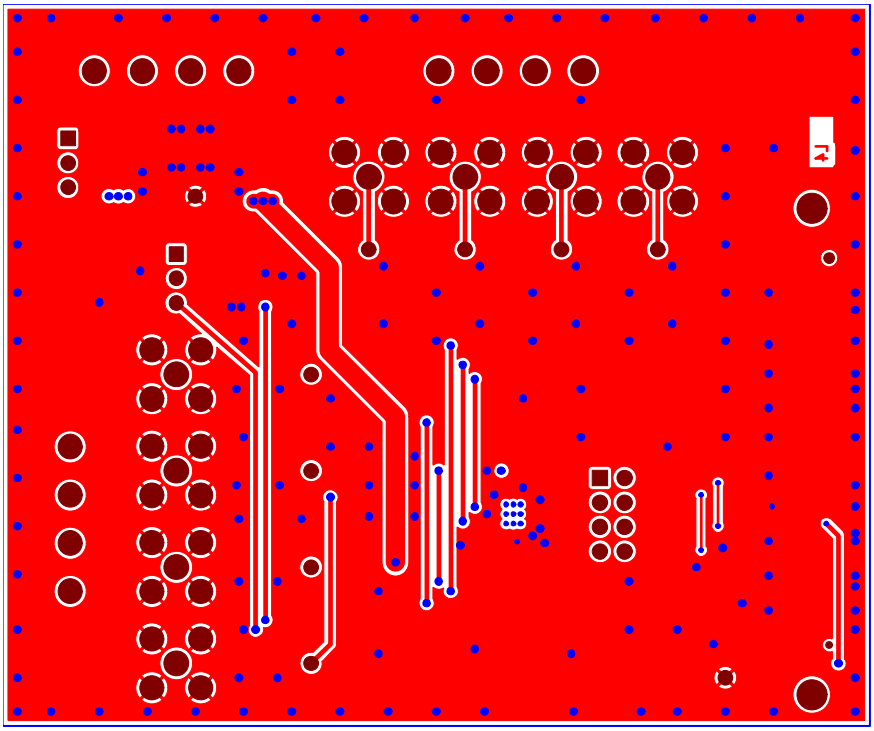

Figure 14. EVAL-ADGS1212SDZ Bottom Layer

ORDERING INFORMATION

BILL OF MATERIALS

Table 4.

Reference Designator	Description
C1 to C2	50 V tantalum capacitors, 10 µF, D size
C3 to C6, C8	50 V, X7R multilayer ceramic capacitors, 0.1 µF, 0603
C7	Capacitor, 10 µF, 0805, 16 V
D1 to D4	Not placed
S1 to S4	Not placed
T1 to T8	Red test points
GND1, GND2	Black test points
J1 to J3	4-pin terminal blocks, 5 mm pitch
J4	120 way connector, 0.6 mm pitch
J5	Through hole, header, 4 × 2, 2.54 mm
LK1, LK2	3-pin single inline (SIL) headers and shorting link
R2 to R7, R12 to R15, R17, R18, R21, R22, R27, R28, R32, R34, R35	Not placed
R8 to R11, R16, R19, R20, R23 to R26, R33	Resistors, 0 Ω, 0603, 1%
R1	Resistor, 10 kΩ, 0.063 W, 1%, 0603
R29	Resistor, 1 kΩ, 0.063 W, 1%, 0603
R30, R31	Resistor, 100 kΩ, 0.063 W, 1%, 0603
SW1	Surface-mount device (SMD) push button switch
U1	ADGS1212, SPI interface, quad SPST switch
U2	ADG819, 1.8 V to 5.5 V, 2:1 multiplexer and SPDT switch
U3	24LC32A-I/MS, 32 kΩ, I²C serial EEPROM

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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