

Evaluating the **ADGS1212** for SPI Interface, Quad SPST Switch, Low Q_{INJ} , Low C_{ON} , $\pm 15\text{ V}/+12\text{ V}$, Mux Configurable

FEATURES

SPI interface with error detection
Includes CRC error detection, invalid read or write address detection, and SCLK count error detection

Analog supply voltages
Dual-supply: $\pm 15\text{ V}$
Single-supply: $+12\text{ V}$

PC control in conjunction with the evaluation software
[EVAL-SDP-CB1Z](#) SDP

EVALUATION KIT CONTENTS

EVAL-ADGS1212SDZ

EQUIPMENT NEEDED

[EVAL-SDP-CB1Z](#) controller board
[ACE](#) software with EVAL-ADGS1212SDZ plug in

DC voltage source
 $\pm 15\text{ V}$ for dual-supply
 $+12\text{ V}$ for single-supply

Optional digital logic supply: 3.3 V

Analog signal source

Method to measure voltage, such as a digital multimeter (DMM)

DOCUMENTS NEEDED

[ADGS1212](#) data sheet

GENERAL DESCRIPTION

The EVAL-ADGS1212SDZ is the evaluation board for the [ADGS1212](#). The [ADGS1212](#) is a low Q_{INJ} , low C_{ON} , quad single-pole, single throw (SPST) switch controlled by a serial peripheral interface (SPI). The SPI has robust error detection features, including cyclic redundancy check (CRC) error detection, invalid read or write address detection, and serial clock (SCLK) count error detection. It is possible to daisy-chain multiple [ADGS1212](#) devices together to enable the configuration of multiple devices with a minimal amount of digital lines. The [ADGS1212](#) also supports burst mode that decreases the time between SPI commands.

Figure 1 shows the EVAL-ADGS1212SDZ typical evaluation board setup. The EVAL-ADGS1212SDZ is controlled by the [EVAL-SDP-CB1Z](#) system demonstration platform (SDP), which connects to a PC via a USB port. The [ADGS1212](#) is on the center of the evaluation board and wire screw terminals are provided to connect to each of the source and drain pins. Three screw terminals power the device and, if required, a fourth terminal provides users with a defined digital logic supply voltage. Alternatively, the digital logic supply voltage can be supplied from the SDP.

Full specifications of the [ADGS1212](#) can be found in the [ADGS1212](#) data sheet available from Analog Devices, Inc., and should be consulted in conjunction with this user guide when using the evaluation board.

The evaluation board interfaces to the USB port of a PC via the SDP board. The [EVAL-SDP-CB1Z](#) board ([SDP-B](#) controller board) is available for order at: www.analog.com/SDP-B.

TABLE OF CONTENTS

Features	1	Evaluation Board Software	5
Evaluation Kit Contents.....	1	Installing the Software	5
Equipment Needed.....	1	Initial Set Up	5
Documents Needed.....	1	Block Diagram and Description.....	6
General Description	1	Memory Map	7
Revision History	2	Evaluation Board Schematics and Artwork.....	8
EVAL-ADGS1212SDZ Evaluation Board Layout.....	3	Ordering Information.....	12
Evaluation Board Hardware.....	4	Bill of Materials.....	12
Power Supplies	4		
Input Signals.....	4		
Link Options	4		

REVISION HISTORY

9/2017—Revision 0: Initial Version

EVAL-ADGS1212SDZ EVALUATION BOARD LAYOUT

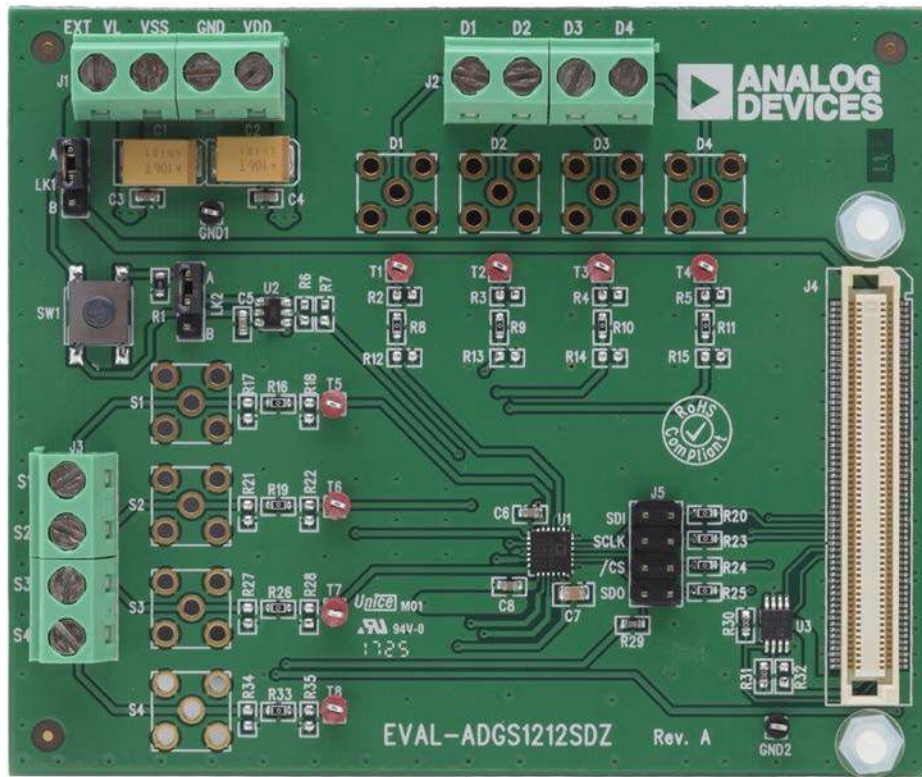


Figure 1.

EVALUATION BOARD HARDWARE

POWER SUPPLIES

Connector J1 provides access to the supply pins of the [ADGS1212](#). VDD, GND, and VSS on J1 terminal block link to the appropriate pins on the [ADGS1212](#). For dual-supply voltages, the evaluation board can be powered from ± 15 V. For single-supply voltages, the GND and VSS terminals must connect together and power the evaluation board from 12 V. Additionally, the SDP supplies 3.3 V to the V_L pin of the [ADGS1212](#) when Link LK1 is in Position B. When using a method other than the SDP to control the [ADGS1212](#), supply between 2.7 V and 5.5 V to the V_L pin of the [ADGS1212](#) via the EXT_VL screw terminal input on J1. LK1 must be in Position A.

INPUT SIGNALS

Provided are two screw connectors, J2 and J3, to connect to both the source and drain pins of the [ADGS1212](#). Additional subminiature version B (SMB) connector pads are available if extra connections are required.

Each trace on the source and drain pins includes two sets of 0603 pads, which can place a load on the signal path to ground.

Table 2. Link Functions

Link Number	Function
LK1	This link selects the source of the V_L voltage supplied to the ADGS1212 . Position A selects EXT_VL from J1. Position B selects the 3.3 V from the SDP.
LK2	This link selects how a hardware reset is performed. Position A indicates the SW1 push button can perform a hardware reset. Position B indicates the SDP can perform a hardware reset.

A $0\ \Omega$ resistor is placed in the signal path and can be replaced with a user defined value. The resistor combined with the 0603 pads can create a simple resistor capacitor filter.

LINK OPTIONS

The EVAL-ADGS1212SDZ evaluation board provides several link options that must be set at the required operating conditions before using it. Table 1 describes the positioning of the links necessary for controlling the evaluation board via the SDP board using a PC and external power supplies. Table 2 describes the functions of these link options.

LK1 must be in Position B to avoid damaging the SDP when using it in conjunction with the EVAL-ADGS1212SDZ.

Table 1. Link Options for SDP Control (Default)

Link Number	Option
LK1	B
LK2	B

BLOCK DIAGRAM AND DESCRIPTION

The similar appearance of the EVAL-ADGS1212SDZ software to the functional block diagram of the [ADGS1212](#) data sheet renders it easy to correlate the board functions of the EVAL-ADGS1212SDZ with the description of the functional block diagram in the data sheet. The [ADGS1212](#) data sheet provides

comprehensive descriptions for each function, block, register, and setting.

Table 3 describes the blocks and their functions pertaining to the evaluation board. The full screen block diagram shown in Figure 4 shows the functionality of each block.

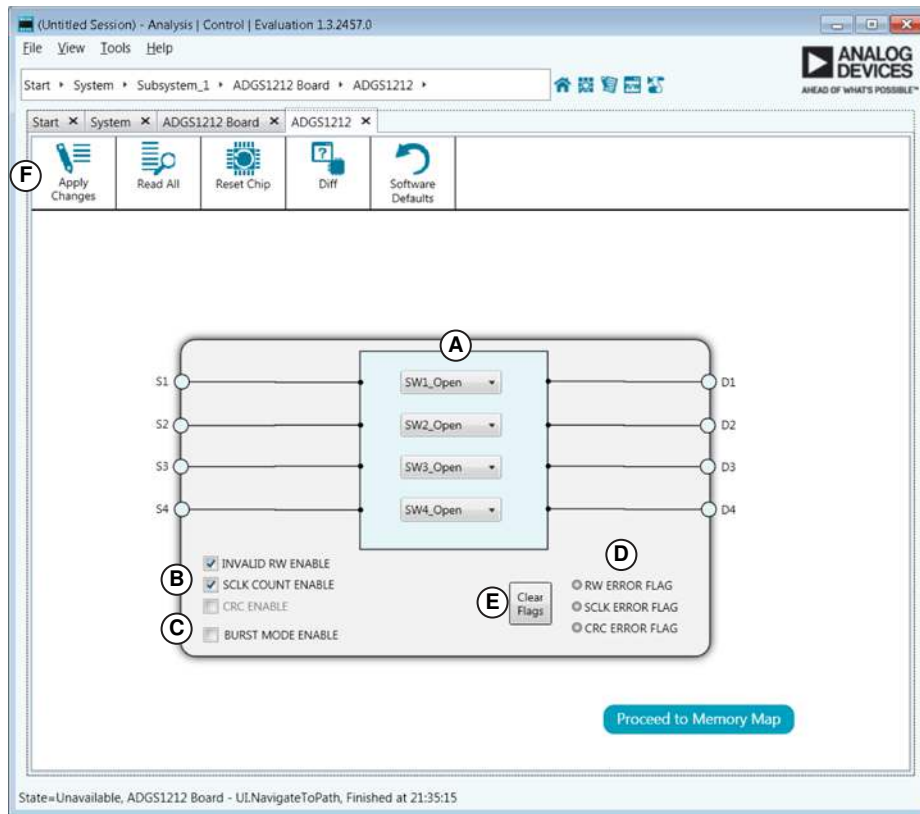


Figure 4. EVAL-ADGS1212SDZ Block Diagram with Labels

Table 3. Block Diagram Functions

Label	Function
A	The dropdown menus configure SW1 to SW4 as open or closed.
B	The INVALID RW ENABLE , SCLK COUNT ENABLE , and CRC ENABLE check boxes enable or disable the error detection features on the SPI interface.
C	The BURST MODE ENABLE check box enables or disables burst mode.
D	The RW ERROR FLAG , SCLK ERROR FLAG , and CRC ERROR FLAG indicators illuminate red when the relevant error flags are asserted in the error flags register.
E	The Clear Flags button clears the error flags register.
F	The Apply Changes button applies all modified values to the devices.

MEMORY MAP

From the **Memory Map** button, all registers are fully accessible and can be edited at a bit level (see Figure 5 and Figure 6). Bits shaded in dark gray are read-only bits and inaccessible from **ACE**. All other bits are toggled. The **Apply Changes** button transfers data modifications to the device.

All changes here correspond to the block diagram. For example, if the internal register bit is enabled, it displays as enabled on the block diagram. Bolded bits or registers represent modified values that have not been transferred to the evaluation board. After clicking **Apply Changes**, the data is transferred to the evaluation board and no longer appears as bolded.

Registers

+/-	Address (Hex)	Name	Data (Hex)	Data (Binary)
+	0001	* SW_DATA	01	0 0 0 0 0 0 0 1
+	0002	ERR_CONFIG	06	0 0 0 0 0 1 1 0
+	0003	* ERR_FLAGS	00	0 0 0 0 0 0 0 0
+	0005	BURST_EN	00	0 0 0 0 0 0 0 0
+	000B	SOFT_RESETB	00	0 0 0 0 0 0 0 0
+	0025	DAISY_CHAIN_EN	00	0 0 0 0 0 0 0 0
+	006C	ERR_FLAGS_RESET	A9	1 0 1 0 1 0 0 1

Figure 5. ADGS1212 Memory Map

Registers

+/-	Address (Hex)	Name	Data (Hex)	Data (Binary)
+	0001	* SW_DATA	09	0 0 0 0 1 0 0 1
+	0002	ERR_CONFIG	06	0 0 0 0 0 1 1 0
+	0003	* ERR_FLAGS	00	0 0 0 0 0 0 0 0
+	0005	BURST_EN	00	0 0 0 0 0 0 0 0
+	000B	SOFT_RESETB	00	0 0 0 0 0 0 0 0
+	0025	DAISY_CHAIN_EN	00	0 0 0 0 0 0 0 0
+	006C	ERR_FLAGS_RESET	A9	1 0 1 0 1 0 0 1

Figure 6. ADGS1212 Memory Map with Unapplied Changes in the SW_DATA Register

EVALUATION BOARD SCHEMATICS AND ARTWORK

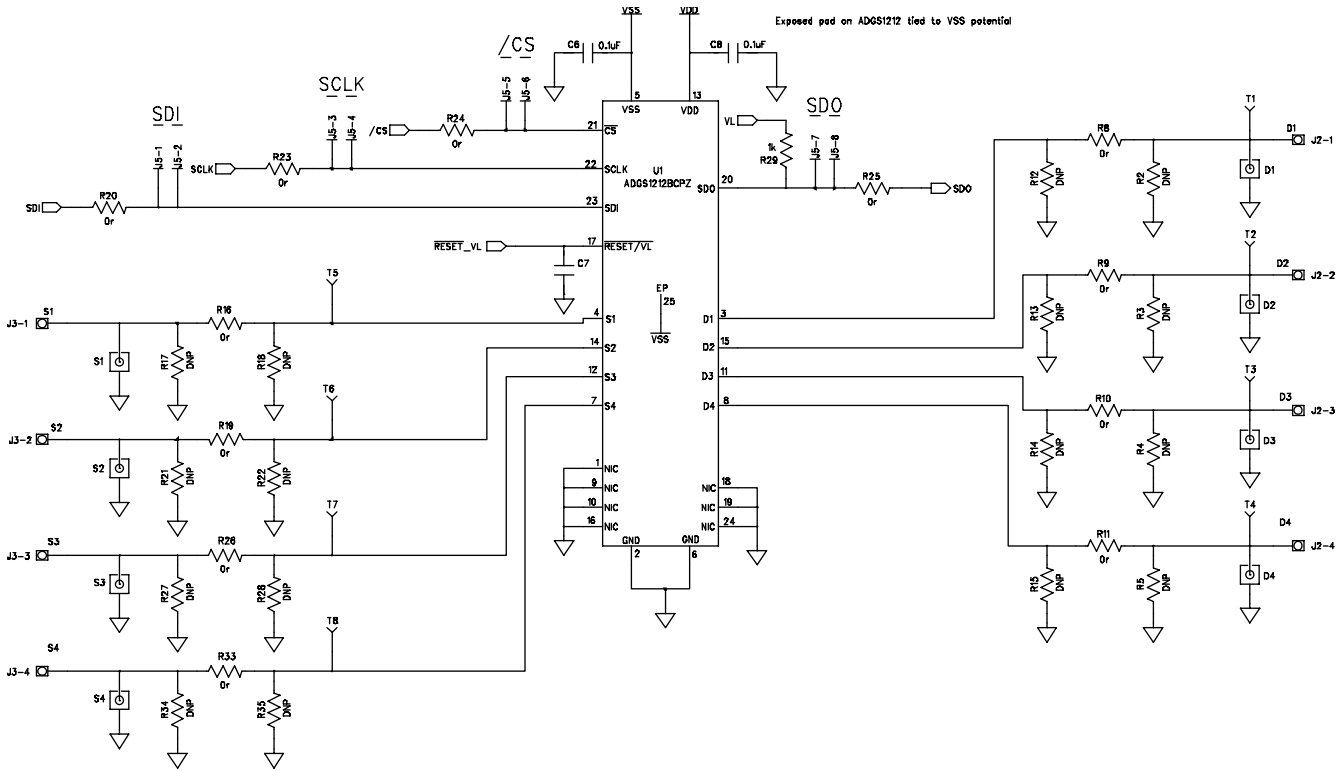


Figure 7. EVAL-ADGS1212SDZ Schematic 1

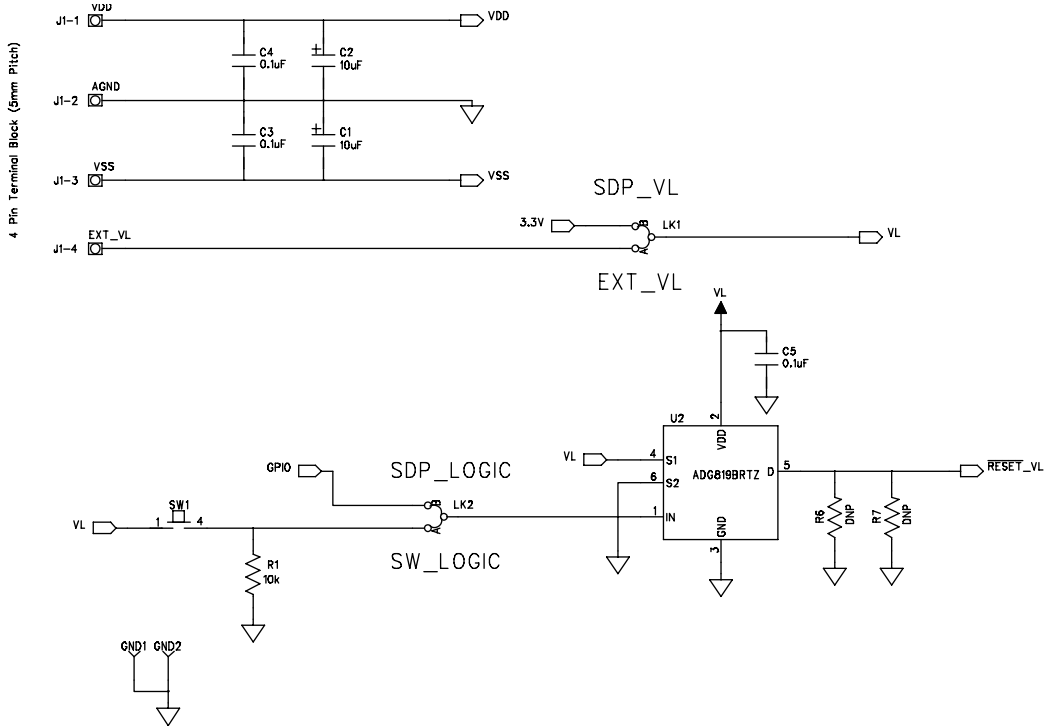


Figure 8. EVAL-ADGS1212SDZ Schematic 2

16200-007

16200-008

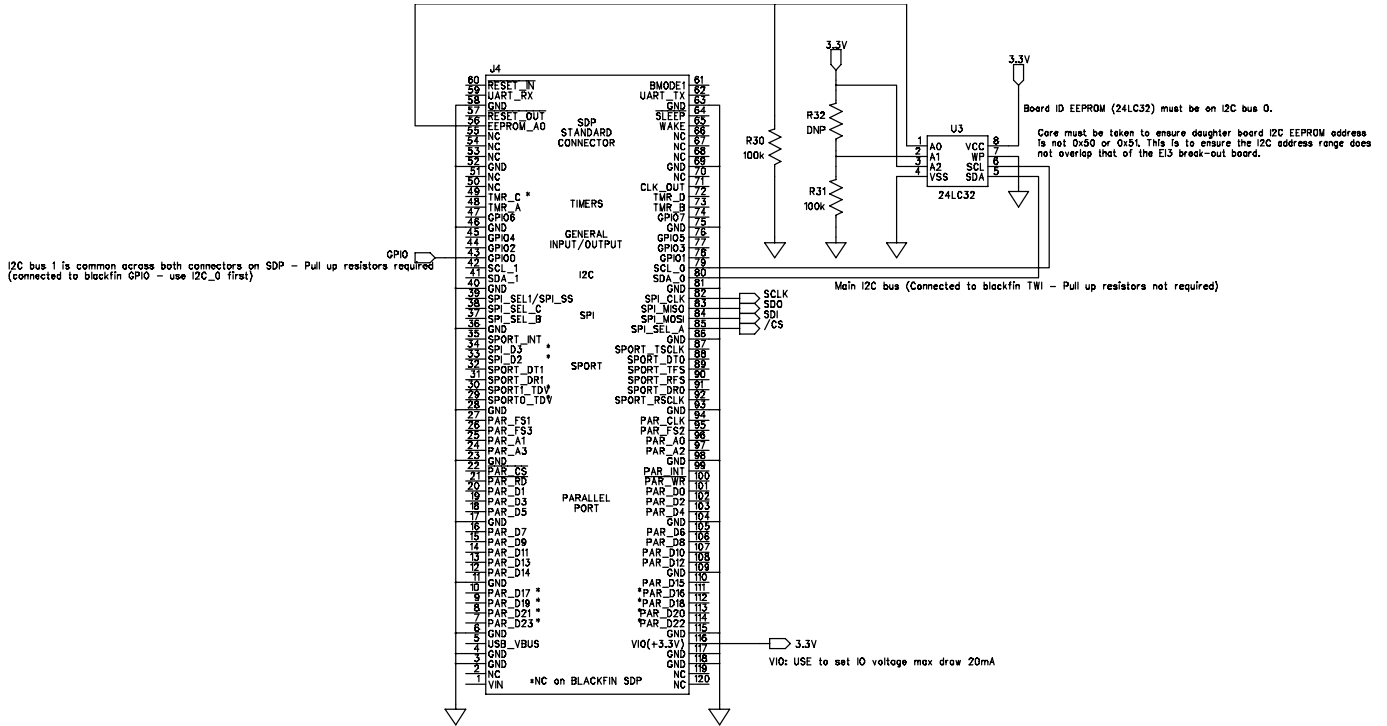


Figure 9. EVAL-ADGS1212SDZ Schematic 3

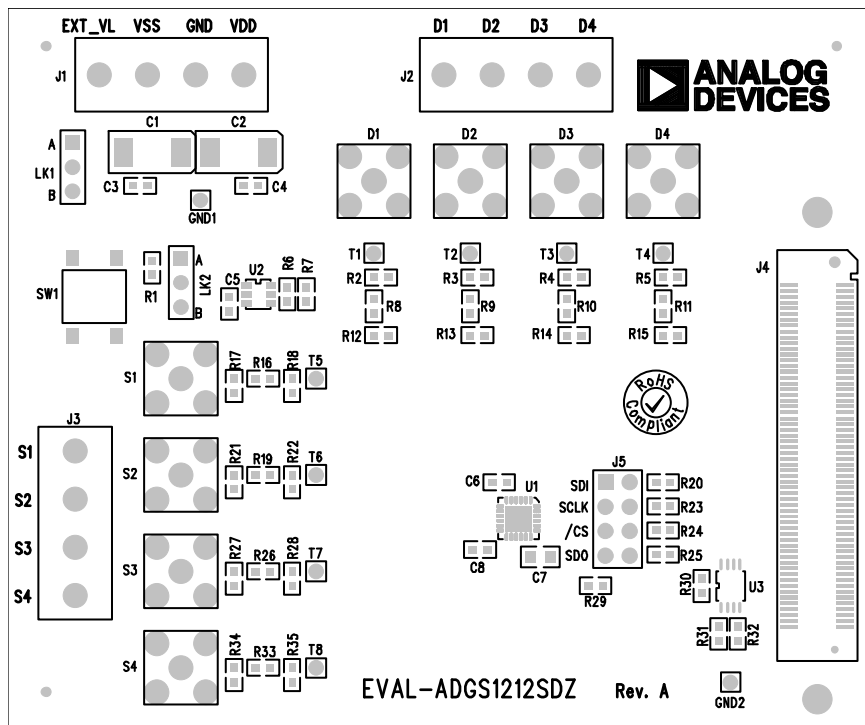
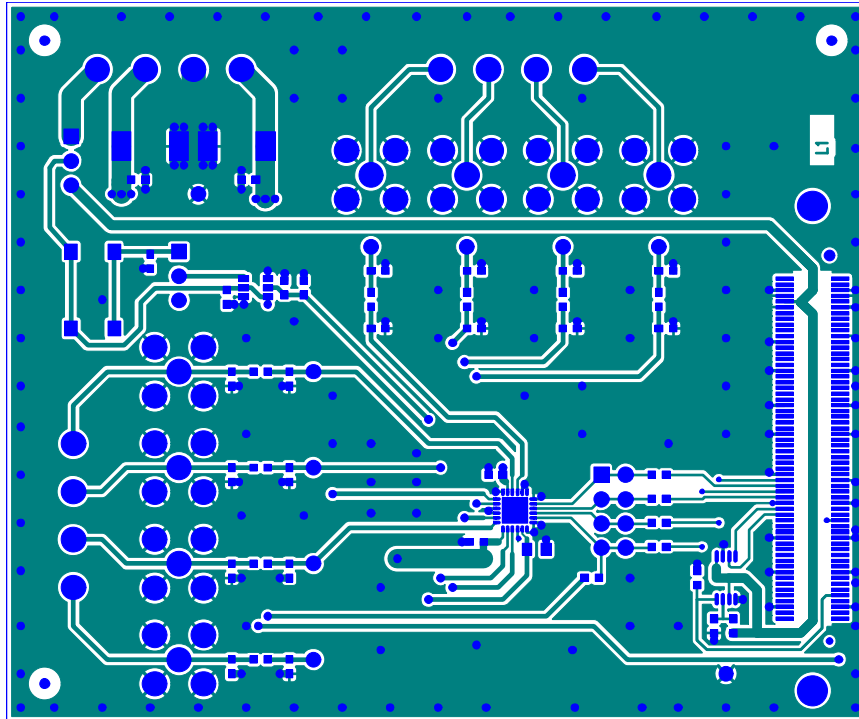
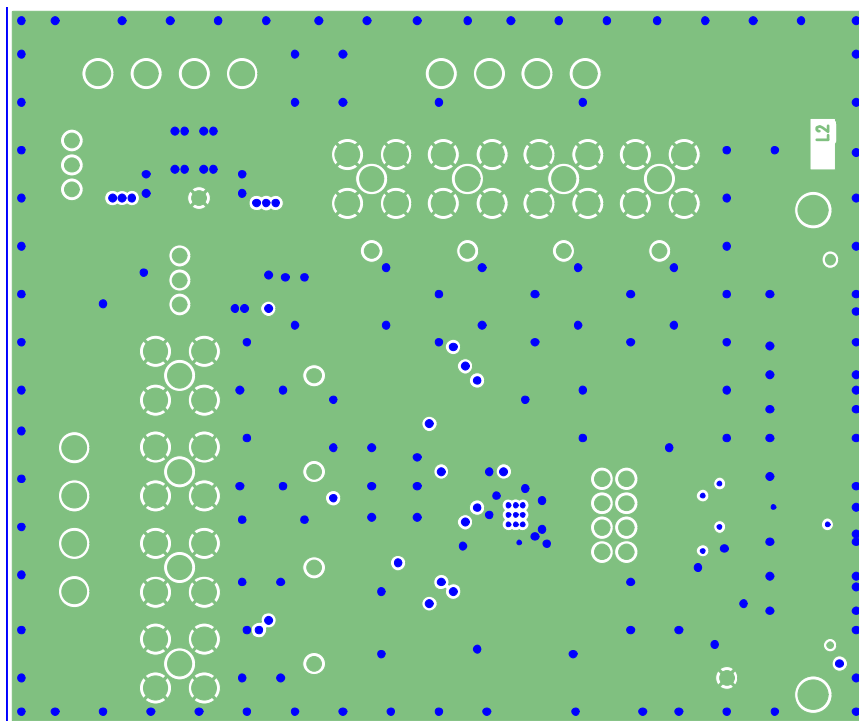


Figure 10. EVAL-ADGS1212SDZ Silk Screen



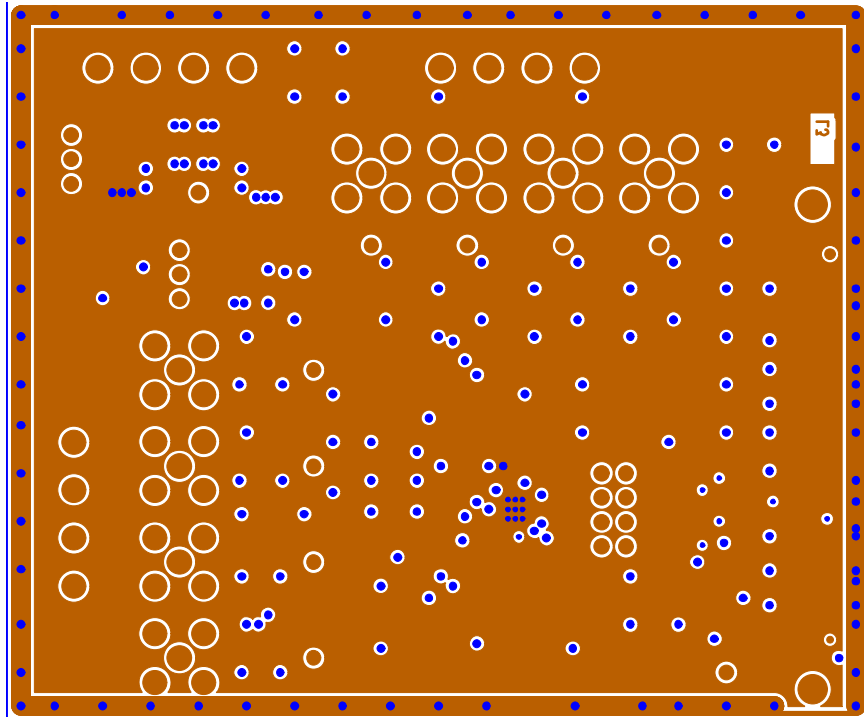
16200-011

Figure 11. EVAL-ADGS1212SDZ Top Layer



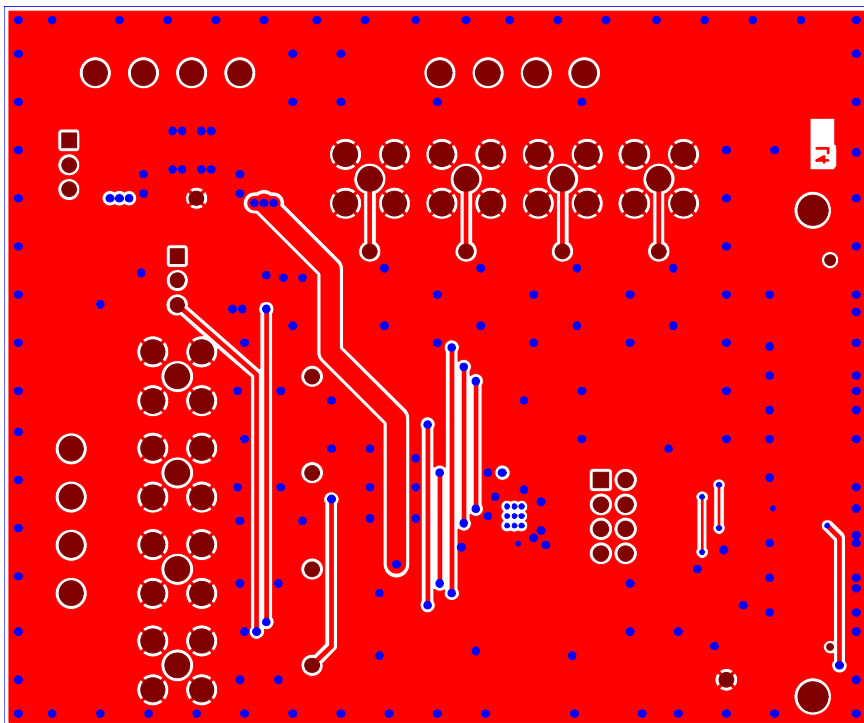
16200-012

Figure 12. EVAL-ADGS1212SDZ Layer 2



162200-013

Figure 13. EVAL-ADGS1212SDZ Layer 3



162200-014

Figure 14. EVAL-ADGS1212SDZ Bottom Layer

ORDERING INFORMATION

BILL OF MATERIALS

Table 4.

Reference Designator	Description
C1 to C2	50 V tantalum capacitors, 10 μ F, D size
C3 to C6, C8	50 V, X7R multilayer ceramic capacitors, 0.1 μ F, 0603
C7	Capacitor, 10 μ F, 0805, 16 V
D1 to D4	Not placed
S1 to S4	Not placed
T1 to T8	Red test points
GND1, GND2	Black test points
J1 to J3	4-pin terminal blocks, 5 mm pitch
J4	120 way connector, 0.6 mm pitch
J5	Through hole, header, 4 \times 2, 2.54 mm
LK1, LK2	3-pin single inline (SIL) headers and shorting link
R2 to R7, R12 to R15, R17, R18, R21, R22, R27, R28, R32, R34, R35	Not placed
R8 to R11, R16, R19, R20, R23 to R26, R33	Resistors, 0 Ω , 0603, 1%
R1	Resistor, 10 k Ω , 0.063 W, 1%, 0603
R29	Resistor, 1 k Ω , 0.063 W, 1%, 0603
R30, R31	Resistor, 100 k Ω , 0.063 W, 1%, 0603
SW1	Surface-mount device (SMD) push button switch
U1	ADGS1212 , SPI interface, quad SPST switch
U2	ADG819 , 1.8 V to 5.5 V, 2:1 multiplexer and SPDT switch
U3	24LC32A-I/MS, 32 k Ω , I ² C serial EEPROM

**ESD Caution**

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Legal Terms and Conditions

By using the evaluation board discussed herein (together with any tools, components documentation or support materials, the "Evaluation Board"), you are agreeing to be bound by the terms and conditions set forth below ("Agreement") unless you have purchased the Evaluation Board, in which case the Analog Devices Standard Terms and Conditions of Sale shall govern. Do not use the Evaluation Board until you have read and agreed to the Agreement. Your use of the Evaluation Board shall signify your acceptance of the Agreement. This Agreement is made by and between you ("Customer") and Analog Devices, Inc. ("ADI"), with its principal place of business at One Technology Way, Norwood, MA 02062, USA. Subject to the terms and conditions of the Agreement, ADI hereby grants to Customer a free, limited, personal, temporary, non-exclusive, non-sublicensable, non-transferable license to use the Evaluation Board FOR EVALUATION PURPOSES ONLY. Customer understands and agrees that the Evaluation Board is provided for the sole and exclusive purpose referenced above, and agrees not to use the Evaluation Board for any other purpose. Furthermore, the license granted is expressly made subject to the following additional limitations: Customer shall not (i) rent, lease, display, sell, transfer, assign, sublicense, or distribute the Evaluation Board; and (ii) permit any Third Party to access the Evaluation Board. As used herein, the term "Third Party" includes any entity other than ADI, Customer, their employees, affiliates and in-house consultants. The Evaluation Board is NOT sold to Customer; all rights not expressly granted herein, including ownership of the Evaluation Board, are reserved by ADI. CONFIDENTIALITY. This Agreement and the Evaluation Board shall all be considered the confidential and proprietary information of ADI. Customer may not disclose or transfer any portion of the Evaluation Board to any other party for any reason. Upon discontinuation of use of the Evaluation Board or termination of this Agreement, Customer agrees to promptly return the Evaluation Board to ADI. ADDITIONAL RESTRICTIONS. Customer may not disassemble, decompile or reverse engineer chips on the Evaluation Board. Customer shall inform ADI of any occurred damages or any modifications or alterations it makes to the Evaluation Board, including but not limited to soldering or any other activity that affects the material content of the Evaluation Board. Modifications to the Evaluation Board must comply with applicable law, including but not limited to the RoHS Directive. TERMINATION. ADI may terminate this Agreement at any time upon giving written notice to Customer. Customer agrees to return to ADI the Evaluation Board at that time. LIMITATION OF LIABILITY. THE EVALUATION BOARD PROVIDED HEREUNDER IS PROVIDED "AS IS" AND ADI MAKES NO WARRANTIES OR REPRESENTATIONS OF ANY KIND WITH RESPECT TO IT. ADI SPECIFICALLY DISCLAIMS ANY REPRESENTATIONS, ENDORSEMENTS, GUARANTEES, OR WARRANTIES, EXPRESS OR IMPLIED, RELATED TO THE EVALUATION BOARD INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTY OF MERCHANTABILITY, TITLE, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS. IN NO EVENT WILL ADI AND ITS LICENSORS BE LIABLE FOR ANY INCIDENTAL, SPECIAL, INDIRECT, OR CONSEQUENTIAL DAMAGES RESULTING FROM CUSTOMER'S POSSESSION OR USE OF THE EVALUATION BOARD, INCLUDING BUT NOT LIMITED TO LOST PROFITS, DELAY COSTS, LABOR COSTS OR LOSS OF GOODWILL. ADI'S TOTAL LIABILITY FROM ANY AND ALL CAUSES SHALL BE LIMITED TO THE AMOUNT OF ONE HUNDRED US DOLLARS (\$100.00). EXPORT. Customer agrees that it will not directly or indirectly export the Evaluation Board to another country, and that it will comply with all applicable United States federal laws and regulations relating to exports. GOVERNING LAW. This Agreement shall be governed by and construed in accordance with the substantive laws of the Commonwealth of Massachusetts (excluding conflict of law rules). Any legal action regarding this Agreement will be heard in the state or federal courts having jurisdiction in Suffolk County, Massachusetts, and Customer hereby submits to the personal jurisdiction and venue of such courts. The United Nations Convention on Contracts for the International Sale of Goods shall not apply to this Agreement and is expressly disclaimed.