DELKIN DEVICES®

H300 Series

Industrial SATA M.2 2242

Engineering Specification

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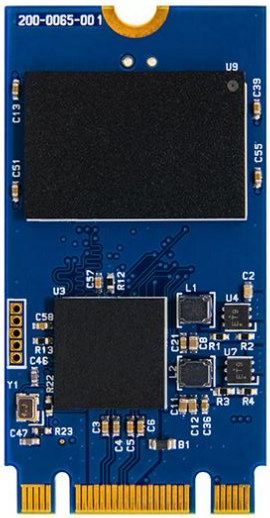


Product Overview

- **Capacity**
  - 8GB – 64GB
- **SATA Interface**
  - SATA 3.3 Compliant
  - Supports 1.5, 3 & 6 Gbps transfer speeds
- **Flash Interface**
  - Flash type: SLC
- **Form Factor**
  - Compliant with SATA-IO M.2 2242 form factor standard
  - B & M keying
- **Performance**
  - Read: up to 260 MB/s
  - Write: up to 115 MB/s
- **Power Consumption**[Note1]
  - Active mode: < 315mA
  - Idle mode: < 65mA
- **MTBF**
  - More than 2,000,000 hours at 0°C
- **Features**
  - Static and Dynamic Wear Leveling
  - Bad Block Management
  - SMART
  - Firmware Update Capability
- **Temperature Range**
  - Operation: -40°C ~ 85°C
  - Storage: -50°C ~ +100°C
- **RoHS compliant**

Notes:

1. Please see “5.2 Power Consumption” for details.

TABLE OF CONTENTS

LIST OF TABLES

1.Introduction

1.1. General Description

Delkin's H300 Series Industrial SATA M.2 2242 is designed as compact, embedded storage media to be used as a boot device or for storing critical data. The industrial-grade drive is fully compliant with SATA-IO standards, and is built with industrial temp SLC NAND flash.

1.2. Flash Management

1.2.1. Error Correction Code (ECC)

Flash memory cells will deteriorate with use, which might generate random bit errors in the stored data. Thus, the controller in Delkin's Industrial M.2 drive applies an advanced BCH ECC algorithm, which can detect and correct errors occur during read processes, ensuring data been read correctly, as well as protecting data from corruption. The Delkin Industrial M.2 also employs "near-miss" ECC, such that all blocks which reach a certain error threshold are automatically refreshed immediately upon detection. The threshold is determined by the specific flash and ECC configuration in the card.

1.2.2.Wear Leveling

NAND Flash devices can only undergo a limited number of program/erase cycles, and in most cases, the flash media are not used evenly. If some blocks are updated more frequently than others, the lifetime of the device would be reduced significantly. Thus, Wear Leveling techniques are applied to extend the lifespan of NAND Flash by evenly distributing write and erase cycles across the media.

The controller in Delkin's newest Industrial M.2 drive utilizes an advanced Wear Leveling algorithm, which optimizes life and performance, through a combination of static and global wear leveling. Static wear leveling is utilized until one flash reaches 90% of the rated P/E cycles, which is more efficient from a performance standpoint. Once a flash reaches 90%, wear leveling switches to a global scheme, and all flash blocks participate in wear leveling as one large pool, which enables the card to maximize lifetime.

1.2.3. Bad Block Management

Bad blocks are blocks that include one or more invalid bits and therefore, their reliability is not guaranteed. Blocks that are identified and marked as bad by the manufacturer are referred to as “Initial Bad Blocks”. Blocks that develop invalid bits during the lifespan of the flash are named “Later Bad Blocks”. The controller in Delkin’s Industrial M.2 drive implements an efficient bad block management algorithm to detect the factory-produced bad blocks and manage any bad blocks that appear with use. This practice further prevents data being stored into bad blocks and improves data reliability.

1.2.4. SMART

SMART, an acronym for Self-Monitoring, Analysis and Reporting Technology, is a special function that allows a memory device to automatically monitor its health. Refer to Section 7 for the command details and the information that can be extracted from the card.

1.2.5.Read Disturb Management

Delkin’s Industrial M.2 drives have advanced Read Disturb Management to prevent uncorrectable errors in heavy read applications. As flash geometries shrink, the likelihood of disturbances when adjacent pages are frequently read is increased, and typically wear leveling is triggered by writing and erasing. However, the advanced read disturb management system actually counts all reads on a block level, and compares them to a configurable threshold. Once the threshold has been reached, a read wear level is triggered and the block is refreshed, sending it to the back of the line. This ensures that errors will not accumulate to the point that they will be uncorrectable.

1.2.6.Firmware Redundancy

Since flash storage is often used in applications with unstable sources of power, protecting the firmware is critical. Delkin’s Industrial M.2 drives maintain two copies of firmware within the flash, so that if the primary copy of the firmware is damaged, the back-up copy can be used. If the back-up copy is used, then the original copy is repaired.

1.2.7. Dynamic Data Refresh

Typically, when a drive is new and less than 10% of the program/erase cycles have been consumed, the data retention time of the flash is 5 or 10 years, depending on the type of flash. At end of life, however, when 100% of the program/erase cycles have been consumed, typically, the retention time is 1 year. To extend long term data retention over the life of a card, Delkin's Industrial M.2 will automatically refresh data that is not accessed for a long time, which can be triggered based on a configurable power-on count threshold and operate in the background.

1.2.8. Power Fail Robustness

With the goal of preventing data corruption and card failure, Delkin's Industrial M.2 drives have been developed to survive unscheduled power interruptions with minimal effect. In the event of a power loss, the controller will reset and flash is immediately write-protected. A log is kept of recent flash transactions, and if the last data in the log is corrupt, then the controller will recover the latest valid entry. If a write operation was in process at the time of the power loss, but not committed to flash, or the tables had not yet been updated, then this data might be lost. Since the original data is always kept in a "twin" of the active block, we can always revert back to the last known valid state of the card.

1.2.9. Page-based Mapping

The H300 M.2 utilizes page-based mapping, which has the advantages of improved random performance and reduced write amplification, which improves device overall life.

2.Product Specifications

2.1. Overview

- **Capacity / Flash Type**
  - 8GB to 64GB Industrial Temperature SLC

- **Electrical/Physical Interface**
  - Compliant with SATA 3.3 Specifications, supporting 6.0 Gbps, 3.0 Gbps and 1.5 Gbps transfer speeds
  - Compliant with SATA-IO M.2 standards
  - B and M Keying

- **ECC**
  - Flexible BCH & GCC engines, providing correction capability based on flash configuration
  - Controller SRAM ECC

- **Supports SMART commands**

- **Supports Secure Erase and Sanitize via ATA pass through commands**

- **OS Compatibility**
  - All SATA 3.3 Compatible Operating Systems supported, including:
    - Windows 7 (32 & 64bit), Windows 8, Windows 10, Windows XP
    - Linux Kernel 4.2.0-27 (Ubuntu 15.10)
    - Mac OS X 10.8.4, 10.11.2

2.2. Sequential and Random Performance

Table 2-1 Performance by Capacity & Firmware Type

Capacity	Sequential		Random	
	Read (MB/s)	Write (MB/s)	Read (MB/s)	Write (MB/s)
8GB SLC	255	50	14	5
16GB SLC	255	70	14	5
32GB SLC	255	90	14	5
64GB SLC	260	115	14	5

Measured with CrystalDiskMark 3.0.3 64 bit, Random performance for 4K blocks.

2.3. Part Numbers

Industrial SLC M.2 2242 (-40 to 85°C Operating Temperature)

Table 2-2 Part Numbers by Capacity

Capacity	Standard Length Case
8GB	MB08TLJF5-42000-D
16GB	MB16TLJF5-42000-D
32GB	MB32TRDF5-42000-D
64GB	MB64TRDF5-42000-D

NOTES:

1. For optional Acrylic conformal coating (contact Delkin for additional cost and MOQ) to protect the devices from moisture and contaminants, replace the 000 in the part number with 050.
2. Customized parts will have a special code in place of the 000 to indicate the customer-specific features or attributes of the part – options include labeling, formatting, content loading, etc.
3. Contact Delkin for Security version details.

3. Environmental Specifications

3.1. Environmental Conditions

3.1.1. Temperature and Humidity

- Temperature:
  - Storage: -50°C to +100°C
  - Operational: -40°C to +85°C

- Humidity:
  - RH 10 - 95% under 55°C

3.1.2. Shock & Vibration

- Shock Specification
  - 12G Sawtooth pulse, 11 ms duration, 3 axes

- Vibration Specification
  - Sine Vibration: 10Hz ~2000Hz, 16.3 G peak to peak, 3 axes
  - Random Vibration: 10Hz ~2000Hz, 1.49 GRMS, 3 axes

3.2. MTBF

MTBF, an acronym for Mean Time Between Failures, is a measure of a device's reliability. Its value represents the average time between a repair and the next failure. The measure is typically in units of hours. The higher the MTBF value, the higher the reliability of the device. The predicted result of the H300 M.2 drive is more than 2,000,000 hours for 0°C to 25°C operation.

3.3. Certification & Compliance

- RoHS

4.Endurance & Data Retention

Attribute	Value
Raw Flash Program/Erase Rating	100,000 cycles
TBW	Contact Delkin for TBW and life estimate based on your specific application / workload
Data Retention	10 years when P/E cycles < 10% of rated cycling 1 year when P/E cycles at 100% of rated cycling

5. Electrical Specifications

5.1. Supply Voltage

Table 5-1 Supply Voltage

Parameter	Rating
Operating Voltage	3.3V ± 5%

5.2. Power Consumption

Table 5-2 Power Consumption

Capacity	Read (max)	Write (max)	Idle (max)
8GB	315	190	65
16GB	315	210	65
32GB	315	230	65
64GB	315	255	65

Unit: mA

NOTES:
1. The measured input power voltage is 3.3V.
2. Power Consumption may vary according to flash configuration, host platform and other factors.

6.Interface

6.1. Pin Assignment and Descriptions

Table 6-1 Pin Assignment and Description for M.2

Pin #	Type	Description
1	CONFIG_3	Defines module type = Ground for SATA
2	3.3V	Supply pin, 3.3V
3	GND	Ground
4	3.3V	Supply pin, 3.3V
5	No connect	No connect
6 - 8	Not available	No connect (used for other purposes)
9	No connect	No connect
10	DAS/DSS	Device Activity Signal / Disable Staggered Spin-up
11	No connect	No connect
12 – 19	(Removed for key)	Mechanical Notch B
20	Not available	No connect (used for other purposes)
21	CONFIG_0	Defines module type = Ground for SATA
22 - 26	Not available	No connect (used for other purposes)
27	GND	Ground
28 - 32	Not available	No connect (used for other purposes)
33	GND	Ground
34 - 37	Not available	No connect (used for other purposes)
38	DEVSLP	Device Sleep, input. If driven high, the host is informing the SSD to enter a low power state
39	GND	Ground
40	Not available	No connect (used for other purposes)
41	SATA B+	Host receiver differential signal pair
42	Not available	No connect (used for other purposes)
43	SATA B-	Hose receiver differential signal pair
44	Not available	No connect (used for other purposes)
45	GND	Ground
46	Not available	No connect (used for other purposes)
47	SATA A-	Host transmitter differential signal pair
48	Not available	No connect (used for other purposes)
49	SATA A+	Host transmitter differential signal pair

Pin #	Type	Description
50	Not available	No connect (used for other purposes)
51	GND	Ground
52 – 55	Not available	No connect (used for other purposes)
56	MFG1	Manufacturing pin. Use determined by vendor (no connect on host)
57	GND	Ground
58	MFG2	Manufacturing pin. Use determined by vendor (no connect on host)
59 – 66	(Removed for key)	Mechanical Notch M
67 - 68	Not available	No connect (used for other purposes)
69	CONFIG_1	Defines module type = Ground for SATA
70	3.3V	Supply pin, 3.3V
71	GND	Ground
72	3.3V	Supply pin, 3.3V
73	GND	Ground
74	3.3V	Supply pin, 3.3V
75	CONFIG_2	Defines module type = Ground for SATA

7. Physical Attributes

7.1. Mechanical Form Factor

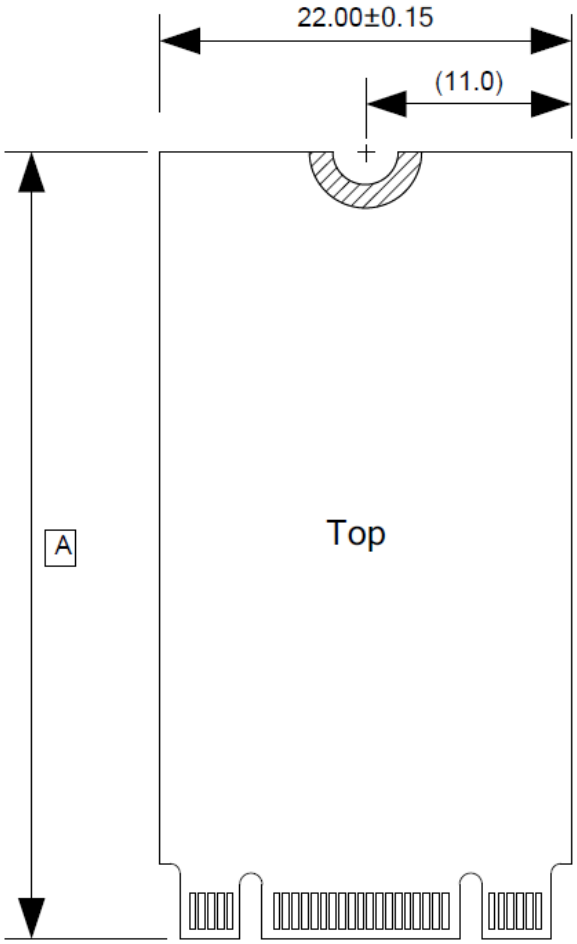
Table 7-1 M.2 Mechanical Form Factor Attributes

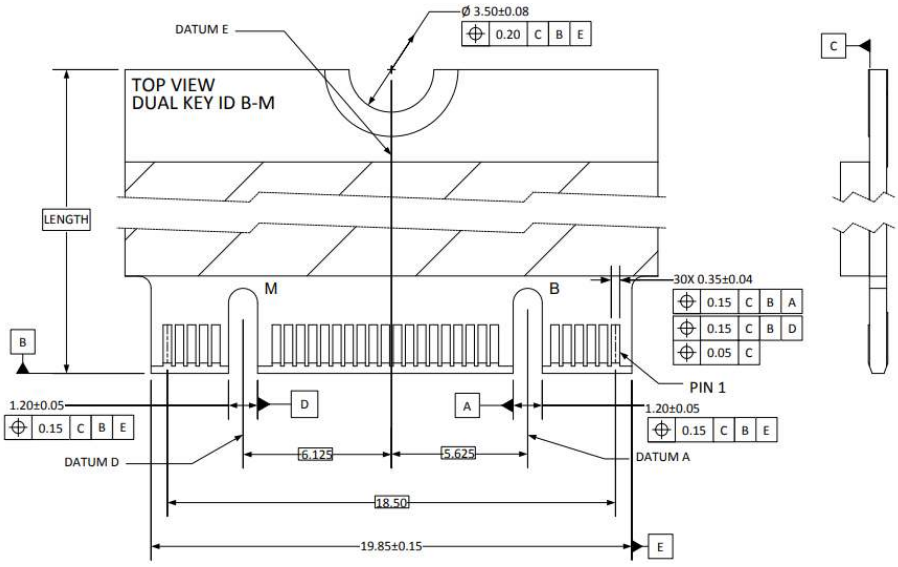
Dimension	Measurement
Height	3.2 mm ± 0.15
Width	22.0 mm ± 0.15
Length	42.0 mm ± 0.15

7.2. Mechanical Dimensions

A (mm)

Type	Nominal	Tolerance
2242	42.0	± 0.15





All dimensions in mm.

There are two mechanical keys defined for SSDs:

a) Key B pinout supports SSD/WWAN/Others:

   A) 1x SATA SSD; or

   B) 1x, 2x PCIe SSD (and WWAN) Host Interfaces;

and

b) Key M pinout supports SSDs only:

   A) 1x SATA; or

   B) 1x, 2x, or 4x PCIe Host Interfaces.

Notch Location for Key B - Pins 12 to 19
Notch Location for Key M - Pins 59 to 66

SSD solutions targeting Key B Host I/F set should also employ two notches that coincide with Key B and Key M to enable these to be pluggable into both Socket 2 and Socket 3 (see 3.1). SSD solutions targeting Key M Host I/F set should only emply Key M notch and can only plug into Socket 3. It is not possible to plug a Key M only device into Socket 2 (with Key B).

8. IDENTIFY DEVICE & SMART

8.1. ATA Identify Device Information

The following table lists the information returned by the Identify Device ATA Passthrough command.

Word Address	Default Value	Total Bytes	Data Field Type Information
0	0000h	2	General configuration bit significant information
1	XXXXh	2	Default number of cylinders
2	C837h	2	Specific configuration
3	00XXh	2	Default number of heads
4 – 5	0000h	4	Reserved
6	XXXXh	2	Default number of sectors per track
7 – 8	XXXXh	4	Number of sectors per card
9	0000h	2	Reserved
10-19	XXXXh	20	Serial number (20 ASCII characters)
20 – 21	0000h	4	Reserved
22	0000h	2	Number of ECC bytes passed on Read/Write Long Commands
23 – 26	XXXXh	8	Firmware revision (8 ASCII characters)
27 – 46	XXXXh	40	Model number (40 ASCII characters)
47	8001h	2	Maximum 1 sector on Read/Write Multiple command
48	0000h	2	Double Word not Supported
49	0F00h	2	Capabilities: DMA, LBA, IORDY supported
50	4001h	2	Capabilities: device specific standby timer minimum
51	0200h	2	PIO data transfer cycle timing mode 2
52	0000h	2	DMA data transfer cycle timing mode not supported
53	0007h	2	Data Fields 54 to 58, 64 to 70 and 88 are valid
54	XXXXh	2	Number of current logical cylinders
55	XXXXh	2	Number of current logical heads
56	XXXXh	2	Number of current logical sectors per track
57 – 58	XXXXh	4	Current capacity in sectors
59	010Xh	2	Multiple sector setting is valid
60-61	XXXXh	4	Total number of sectors addressable in LBA Mode
62	0000h	2	Single Word DMA transfer not implemented
63	0X0Xh	2	Multiword DMA transfer mode
64	0003h	2	Advanced PIO modes: modes 3 and 4 supported
65	0078h	2	Minimum Multiword DMA cycle time, 0 if no MDMA
66	0078h	2	Recommended Multiword DMA cycle time, 0 if no MDMA
67	0078h	2	Minimum PIO transfer cycle time without flow control
68	0078h	2	Minimum PIO transfer cycle time with flow control
69	C100h	2	Deterministic read after DSM Trim, Download Microcode DMA supported
70 – 74	0000h	10	Reserved
75	001Fh	2	Queue depth
76	E20Eh	2	Serial ATA capabilities: READ LOG DMA EXT, Device Automatic Partial to Slumber transitions, SATA Gen 1-3 Supported, Host Automatic Partial to Slumber transitions, Receipt of host-initiated interface power management requests

Word Address	Default Value	Total Bytes	Data Field Type Information
77	00CXh	2	Serial ATA Additional capabilities: DevSleep to reduced power state, RECEIVE FPDMA QUEUED, SEND FPDMA QUEUED supported
78	015Eh	2	Serial ATA Features supported: Device Sleep, software settings preservation, in-order data delivery, device initiated interface power management, DMA Setup Auto-Activate, non-zero buffer offsets supported
79	0XXXh	2	Serial ATA features enabled
80	0FE0h	2	Major version number, ATA-5 to ATA-8, ACS-1 to ACS-4 support
81	0000h	2	Minor version number, not reported
82	746Bh	2	Command set: NOP, READ BUFFER, WRITE BUFFER, Host Protected Area, look-ahead, volatile write cache, power management feature set, Security Mode feature set, SMART feature set
83	7509h	2	Command set: FLUSH CACHE, FLUSH CACHE EXT, LBA48, Set Max Security Extension, Advanced Power Management, DOWNLOAD MICROCODE
84	4161h	2	Command set/feature supported extension: World Wide Name, Write FUA Ext, General Purpose Logging, SMART self-test, SMART error logging
85	74XXh	2	Command set enabled: NOP, READ BUFFER, WRITE BUFFER, Host Protected Area, look ahead enabled/disabled, volatile write cache enabled/disabled, power management feature set, Security Mode feature set enabled/disabled, SMART feature set enabled/disabled
86	F409h	2	Command set enabled: FLUSH CACHE, FLUSH CACHE EXT, LBA48, DOWNLOAD MICROCODE, words 119 & 120 supported
87	4161h	2	Command set/feature default
88	XXXXh	2	UDMA transfer mode enabled and supported
89	00XXh	2	Time for Security Erase Unit
90	00XXh	2	Time for Enhanced Security Erase Unit
91	00XXh	2	Advanced power management level
92	XXXXh	2	Master Password Revision Code
93	XXXXh	2	Hardware Reset Result
94 – 99	0000h	12	Reserved
100 – 103	XXXXh	8	Total number of sectors addressable in LBA48 mode
104	0000h	2	Reserved
105	0001h	2	Number of sectors per Data Set Management command
106	4000h	2	Physical sector size / Logical sector size
107	0000h	2	Reserved
108 – 111	XXXXh	8	World wide name
112 – 118	0000h	14	Reserved
119	4008h	2	Commands and feature sets supported
120	4008h	2	Commands and feature sets supported or enabled
121-127	0000h	14	Reserved
128	0XXXh	2	Security Status
129	XX00h	2	Write Protect Status Bit 9 = permanent write protect from vendor command Bit 8 = temporary write protect from vendor command
130-133	XXXXh	8	Firmware date string
134-135	0000h	4	Reserved
136-141	XXXXh	12	Firmware file name
142-147	XXXXh	12	Preformat file name

Word Address	Default Value	Total Bytes	Data Field Type Information
148-153	XXXXh	12	Anchor program file name
154	0000h	2	Firmware major revision
155	0000h	2	Firmware minor revision
156-160	0000h	10	Reserved
161	8202h	2	Reserved
162 – 164	0000h	6	Reserved
165	80XXh	2	Operating Temperature Range
166 – 168	0000h	6	Reserved
169	0001h	2	Trim bit in Data Set Management supported
170 to 208	0000h	78	Reserved
209	4000h	2	Alignment of logical blocks within a larger physical block
210 – 216	0000h	14	Reserved
217	0001H	2	Solid State Device (non-rotating media)
218 – 221	0000h	8	Reserved
222	11FFh	2	Transport major revision number: ATA8-AST, SATA 1.0 – SATA 3.3
223	0000h	2	Transport minor revision number
224-254	0000h	62	Reserved
255	XXA5h	2	Integrity Word

8.2. ATA SMART Functionality

The H300 M.2 firmware supports the following SMART commands, determined by the Feature Register value.

Value	Command
D0h	Read Data
D1h	Read Attribute Thresholds
D2h	SMART Enable/Disable Attribute Autosave
D5h	SMART Read Log
D6h	SMART Write Log
D8h	Enable SMART Operations
D9h	Disable SMART Operations
DAh	SMART Return Status
E0h	SMART Read Remap Data
E1h	SMART Read Wear Level Data

SMART commands with Feature Register values not mentioned in the above table are not supported and will be aborted.

8.2.1. SMART Enable Operations

COMMAND CODE: B0h with a Feature Register value of D8h

PROTOCOL: Non-data command

INPUTS:

Register	7	6	5	4	3	2	1	0
Features	D8h							
Sector Count								
Sector Number								
Cylinder Low	4Fh							
Cylinder High	C2h							
Device/Head	1	1	1	D				
Command	B0h							

NORMAL OUTPUTS: None required.

ERROR OUTPUTS: Aborted if the signature in the Cylinder registers is invalid.

DESCRIPTION: This command enables access to the SMART capabilities of the M.2 controller firmware. The state of SMART (enabled or disabled) is preserved across power cycles.

8.2.2.SMART Disable Operations

COMMAND CODE: B0h with a Feature Register value of D9h

PROTOCOL: 5Ah

INPUTS:

Register	7	6	5	4	3	2	1	0
Features	D9h							
Sector Count								
Sector Number								
Cylinder Low	4Fh							
Cylinder High	C2h							
Device/Head	1	1	1	D				
Command	B0h							

NORMAL OUTPUTS: None required.

ERROR OUTPUTS: Aborted if either the signature in the Cylinder registers is invalid or if SMART is not enabled.

DESCRIPTION: This command disables access to the SMART capabilities of the M.2 controller firmware. The state of SMART (enabled or disabled) is preserved across power cycles.

8.2.3.SMART Enable/Disable Attribute Autosave

COMMAND CODE: B0h with a Feature Register value of D2h

PROTOCOL: 5Ah

INPUTS:

Register	7	6	5	4	3	2	1	0
Features	D2h							
Sector Count	00h or F1h							
Sector Number								
Cylinder Low	4Fh							
Cylinder High	C2h							
Device/Head	1	1	1	D				
Command	B0h							

NORMAL OUTPUTS: None required.

ERROR OUTPUTS: Aborted if either the signature in the Cylinder registers is invalid or if SMART is not enabled.

DESCRIPTION: This command is effectively a no-operation, as the data for the SMART function is always available and kept current in the firmware.

8.2.4.SMART Read Data

COMMAND CODE: B0h with a Feature Register value of D0h

PROTOCOL: PIO data in.

INPUTS:

Register	7	6	5	4	3	2	1	0
Features	D0h							
Sector Count								
Sector Number								
Cylinder Low	4Fh							
Cylinder High	C2h							
Device/Head	1	1	1	D				
Command	B0h							

NORMAL OUTPUTS: None required.

ERROR OUTPUTS: Aborted if the signature in the Cylinder registers is invalid or if SMART is not enabled.

DESCRIPTION: This command returns one sector of SMART data. The data structure returned is shown in 8.2.5.

8.2.5.SMART Data Structure

The following 512 bytes make up the device SMART data structure. Users can obtain the data using the “SMART Read Data” command (D0h.)

Byte	F / V	Description
0 – 1	0010h	SMART structure version
2 – 361		Attribute entries 1 to 30 (12 bytes each)
362	00h	Off-line data collection status (no off-line data collection)
363	00h	Self-test execution status byte (self-test completed)
364 – 365	0000h	Total time to complete off-line data collection activity
366	00h	--
367	00h	Off-line data collection capability (no off-line data collection)
368 – 369	0003h	SMART capability
370	00h	Error logging capability (no error logging)
371	00h	--
372	00h	Short self-test routine recommended polling time
373	00h	Extended self-test routine recommended polling time
374 – 385	00h	Reserved
386 – 387	0004h	SMART Structure Version
388 – 391		Firmware “Commit” Counter
392 - 395		Firmware Wear Level Threshold
396	01h	Global Wear Leveling Active
397	01h	Global Bad Block Management active
398 – 401		Average Flash Block Erase Count in native mode block pool
402 – 405		Number of Flash Blocks involved in Wear Leveling in all block pools
406 – 409		Number of total ECC errors in all block pools during firmware initialization
410 – 413		Number of correctable ECC errors in all block pools during firmware initialization
414 – 417		Number of Flash Blocks involved in wear leveling in native mode block pool
418 – 421		Number of total ECC errors in native mode block pool during firmware initialization
422 – 425		Number of correctable ECC errors in native block mode pool during firmware initialization
426 – 429		Average Flash Block Erase Count in SLC mode block pool
430 – 433		Number of Flash Blocks involved in wear leveling inSLC mode block pool
434 – 437		Number of total ECC errors in SLC mode block pool during firmware initialization
438 – 441		Number of correctable ECC errors in SLC mode block pool during firmware initialization
442 – 510	00h	-
511		Data structure checksum

- The attributes that are defined for the M.2 firmware return their data in the attribute section of the SMART data, using a 12 byte data field.
- The field at offset 386 gives a version number for the contents of the SMART data structure. For the controller in the Delkin M.2, only version 4 is defined.
- The byte at offset 396 is fixed to 1 for page-based firmware. All chips within an interleaved channel are used for wear leveling.
- The byte at offset 397 is fixed to 1 for page-based firmware. Bad block management is always done within all chips of an interleaved channel.
- The data at offsets 414 – 441 are available only for TLC flash types with separate block pools for native and SLC mode blocks.

Spare Block Count Attribute

This attribute gives information about the amount of available spare blocks.

Offset	Value	Description
0	196	Attribute ID – Reallocation Count
1 – 2	0013h	Flags – Pre-fail type, attribute value is updated during normal operation, attribute is an event count
3		Attribute value. The value returned here is the percentage of remaining spare blocks summed over all flash chips, i.e. (100 x current spare blocks / initial spare blocks)
4		Attribute value (worst value)
5 – 7		Sum of the initial number of spare blocks for all flash chips
8 – 10		Sum of the current number of spare blocks for all flash chips
11	00h	Reserved

This attribute is used for the SMART Return Status command. If the attribute value field is less than the spare block threshold (currently fixed at 10), the SMART Return Status command will indicate a threshold exceeded condition.

Spare Block Count Worst Chip Attribute Threshold

This attribute gives information about the amount of available spare blocks on the interleave channel that has the lowest current number of spare blocks.

Offset	Value	Description
0	213	Attribute ID – Spare Block Count Worst Channel (vendor specific)
1 – 2	0013h	Flags – Pre-fail type, attribute value is updated during normal operation, attribute is an event count
3		Attribute value. The value returned here is from all interleaved channels the worst percentage of remaining spare blocks i.e. (100 * current spare blocks / initial spare blocks).
4		Attribute value (worst value)
5 – 7		Initial number of spare blocks of the interleave channel with the lowest current number of spare blocks
8 – 10		Current number of spare blocks of the interleave channel with the lowest current number of spare blocks
11	00h	Reserved

Erase Count Attribute

This attribute gives information about the amount of flash block erases that have been performed.

Offset	Value	Description
0	229	Attribute ID – Erase Count Usage (vendor specific)
1 – 2	001Xh	Flags – Pre-fail or Advisory type, attribute value is updated during normal operation, attribute is an event count
3		Attribute value. The value returned here is an estimation of the remaining card life, in percent, based on the number of flash block erases compared to the target number of erase cycles per block.
4		Attribute value (worst value)
5 – 10		Estimated total number of block erases.
11	00h	Reserved

This attribute is used for the SMART Return Status command. If the attribute value field is less than the erase count threshold (currently fixed at 10), the SMART Return Status command will indicate a threshold exceeded condition.
The target number of erase cycles per flash block is taken from the MaxBlockEraseCount column in the Device Description file.

Total ECC Errors Attribute

This attribute gives information about the total number of ECC errors that have occurred on flash read commands during firmware runtime. This attribute is not used for the SMART Return Status command.

Offset	Value	Description
0	203	Attribute ID – Number of ECC Errors
1 – 2	001Ah	Flags – Advisory type, attribute value is updated during normal operation, attribute is an event count, attribute is an error rate
3	64h	Attribute value. This value is fixed at 100.
4	64h	Attribute value (worst value)
5 – 8		Total number of ECC errors (correctable and uncorrectable)
9 – 10		---
11	00h	Reserved

Correctable ECC Errors Attribute

This attribute gives information about the total number of correctable ECC errors that have occurred on flash read commands during firmware runtime. This attribute is not used for the SMART Return Status command.

Offset	Value	Description
0	204	Attribute ID – Number of corrected ECC Errors
1 – 2	001Ah	Flags – Advisory type, attribute value is updated during normal operation, attribute is an event count, attribute is an error rate
3	64h	Attribute value. This value is fixed at 100.
4	64h	Attribute value (worst value)
5 – 8		Total number of correctable ECC errors
9 – 10		---
11	00h	Reserved

UDMA CRC Errors Attribute

This attribute gives information about the total number of SATA CRC errors

Offset	Value	Description
0	199	Attribute ID –UDMA CRC error rate
1 – 2	001Ah	Flags – Advisory type, attribute value is updated during normal operation, attribute is an event count, attribute is an error rate
3	64h	Attribute value. This value is fixed at 100.
4	64h	Attribute value (worst value)
5 – 8		Total number of SATA CRC errors
9 – 10		---
11	00h	Reserved

Total Number of Reads Attribute

This attribute gives information about the total number of sectors read from flash, which can be useful for the interpretation of the number of correctable or total ECC errors. This attribute is not used for the SMART Return Status command.

Offset	Value	Description
0	232	Attribute ID – Number of Reads (vendor specific)
1 – 2	0012h	Flags – Advisory type, attribute value is updated during normal operation, attribute is an event count
3	64h	Attribute value. This value is fixed at 100.
4	64h	Attribute value (worst value)
5 - 10		Total number of flash read commands
11	00h	Reserved

Power On Count Attribute

Offset	Value	Description
0	12	Attribute ID – Power On Count (vendor specific)
1 – 2	0012h	Flags – Advisory type, attribute value is updated during normal operation, attribute is an event count
3	64h	Attribute value. This value is fixed at 100.
4	64h	Attribute value (worst value)
5 - 8		Number of Power On cycles
9 – 10		---
11	00h	Reserved

Total LBAs Written Attribute

This attribute gives the total amount of data written to the disk, in units of 32MB (65536 sectors.) This number can be converted to Terabytes Written (TBW) by dividing the raw attribute value by 2^{15}.

Offset	Value	Description
0	241	Attribute ID – Total LBAs Written (vendor specific)
1 – 2	0012h	Flags – Advisory type, attribute value is updated during normal operation, attribute is an event count
3	64h	Attribute value. This value is fixed at 100.
4	64h	Attribute value (worst value)
5 - 10		Total number of LBAs written to the disk, divided by 65536
11	00h	Reserved

Total LBAs Read Attribute

This attribute gives the total amount of data read from the disk, in units of 32MB (65536 sectors.) This number can be converted to Terabytes read by dividing the raw attribute value by 2^{15}.

Offset	Value	Description
0	241	Attribute ID – Total LBAs Read (vendor specific)
1 – 2	0012h	Flags – Advisory type, attribute value is updated during normal operation, attribute is an event count
3	64h	Attribute value. This value is fixed at 100.
4	64h	Attribute value (worst value)
5 - 10		Total number of LBAs read from the disk, divided by 65536
11	00h	Reserved

Anchor Block Status Attribute

This attribute reports how many times the Anchor block of the card has been re-written, either by the Anchor block repair routine, or by a firmware update.

Offset	Value	Description
0	214	Attribute ID – Anchor Block Status (vendor specific)
1 – 2	0002h	Flags – Advisory type, attribute value is updated during normal operation
3	64h	Attribute value. This value is fixed at 100.
4	64h	Attribute value (worst value)
5 – 8		Anchor Block Write Count
9 – 10		---
11	00h	Reserved

Trim Status Attribute

This attribute gives percent ratio for the disk space that is currently in the trimmed state (as a percentage).

Offset	Value	Description
0	215	Attribute ID – Trim Status (vendor specific)
1 – 2	0002h	Flags – Advisory type, attribute value is updated during normal operation
3		Attribute value.
4		Attribute value (worst value)
5 - 10		---
11	00h	Reserved

Temperature Status Attribute

This attribute reports the current, min and max temperature of the internal temp sensors. The attribute value is set to the current temperature and the worst value is set to the maximum temperature. Temperature is read every 4 seconds.

Offset	Value	Description
0	194	Attribute ID – Temperature Status (vendor specific)
1 – 2	0002h	Flags – Advisory type, attribute value is updated during normal operation
3		Attribute value.
4		Attribute value (worst value)
5 - 10		---
11	00h	Reserved

8.2.6.SMART Read Attribute Thresholds

COMMAND CODE: B0h with a Feature Register value of D1h

PROTOCOL: PIO data in.

INPUTS:

Register	7	6	5	4	3	2	1	0
Features	D1h							
Sector Count								
Sector Number								
Cylinder Low	4Fh							
Cylinder High	C2h							
Device/Head	1	1	1	D				
Command	B0h							

NORMAL OUTPUTS: None required

ERROR OUTPUTS: Aborted if either the signature in the Cylinder registers is invalid or if SMART is not enabled.

DESCRIPTION: This command returns one sector of SMART attribute thresholds. The data structure returned is:

Offset	Value	Description
0 - 1	001h	SMART structure version
2 – 361		Attribute threshold entries 1 to 30 (12 bytes each)
362 – 379	00h	Reserved
380 – 510	00h	---
511		Data structure checksum

Spare Block Count Attribute Threshold

Offset	Value	Description
0	196	Attribute ID – Reallocation Count
1		Spare Block Count Threshold
2 - 11	00h	Reserved

Spare Block Count Worst Channel Attribute Threshold

Offset	Value	Description
0	213	Attribute ID – Spare Block Count Worst Channel (vendor specific)
1		Spare Block Count Worst Channel Threshold
2 - 11	00h	Reserved

Erase Count Attribute Threshold

Offset	Value	Description
0	229	Attribute ID – Erase Count Usage (vendor specific)
1		Erase Count Threshold
2 - 11	00h	Reserved

Total ECC Errors Attribute Threshold

Offset	Value	Description
0	203	Attribute ID – Number of ECC errors
1	00h	No threshold for the Total ECC Errors Attribute
2 - 11	00h	Reserved

Correctable ECC Errors Attribute Threshold

Offset	Value	Description
0	204	Attribute ID – Number of corrected ECC errors
1	00h	No threshold for the Correctable ECC Errors Attribute
2 - 11	00h	Reserved

UDMA CRC Errors Attribute Threshold

Offset	Value	Description
0	199	Attribute ID –UDMA CRC error rate
1	00h	No threshold for the UDMA CRC Errors Attribute
2 - 11	00h	Reserved

Total Number of Reads Attribute Threshold

Offset	Value	Description
0	232	Attribute ID – Number of Reads (vendor specific)
1	00h	No threshold for the Total Number of Reads Attribute
2 - 11	00h	Reserved

Power On Count Attribute Threshold

Offset	Value	Description
0	12	Attribute ID – Power On Count
1	00h	No threshold for the Power On Count Attribute
2 - 11	00h	Reserved

Total LBAs Written Attribute Threshold

Offset	Value	Description
0	241	Attribute ID –Total LBAs Written (vendor specific)
1	00h	No threshold for the Total LBAs Written Attribute
2 - 11	00h	Reserved

Total LBAs Read Attribute Threshold

Offset	Value	Description
0	242	Attribute ID – Total LBAs Read (vendor specific)
1	00h	No threshold for the Total LBAs Read Attribute
2 - 11	00h	Reserved

Anchor Block Status Attribute Threshold

Offset	Value	Description
0	214	Attribute ID – Anchor Block Status (vendor specific)
1	00h	No threshold for the Anchor Block Status Attribute
2 - 11	00h	Reserved

Trim Status Attribute Threshold

Offset	Value	Description
0	215	Attribute ID – Trim Status (vendor specific)
1	00h	No threshold for the Trim Status Attribute
2 - 11	00h	Reserved

Temperature Status Attribute Threshold

Offset	Value	Description
0	194	Attribute ID – Trim Status (vendor specific)
1	00h	No threshold for the Trim Status Attribute
2 - 11	00h	Reserved

8.2.7.SMART Return Status

COMMAND CODE: B0h with a Feature Register value of DAh

PROTOCOL: 5Ah

INPUTS:

Register	7	6	5	4	3	2	1	0
Features	DAh							
Sector Count								
Sector Number								
Cylinder Low	4Fh							
Cylinder High	C2h							
Device/Head	1	1	1	D				
Command	B0h							

NORMAL OUTPUTS: Returns a status indication as described below.

ERROR OUTPUTS: Aborted if the signature in the Cylinder registers is invalid or if SMART is not enabled.

DESCRIPTION: This command checks the device reliability status. If a threshold exceeded condition exists for either the Spare Block Count Worst Channel attribute or the Erase Count attribute, the device will set the Cylinder Low register to F4h and the Cylinder High register to 2Ch. If no threshold exceeded condition exists, the device will set the Cylinder Low register to 4Fh and the Cylinder High register to C2h.

8.2.8.SMART Read Log

COMMAND CODE: B0h with a Feature Register value of D5h

PROTOCOL: PIO data in

INPUTS:

Register	7	6	5	4	3	2	1	0
Features	D5h							
Sector Count	Number of sectors to be read							
Sector Number	Log address							
Cylinder Low	4Fh							
Cylinder High	C2h							
Device/Head	1	1	1	D				
Command	B0h							

NORMAL OUTPUTS: None required.

ERROR OUTPUTS: Aborted if the signature in the Cylinder registers is invalid or if SMART is not enabled.

DESCRIPTION: This command will return data of the SMART log. The following log addresses are defined:

Address	Description
0x00	Log Directory
0x80 – 0x9F	Host Vendor Specific Logs
0xA0	SMART Wear Level Data
0xA1	SMART Remap Data
0xA2	Reserved

The Log Directory (at Log address 0) returns one sector that shows the number of sectors for Log addresses 1 to 255:

Offset	Value	Description
0 – 1	1	SMART Logging Version
2 – 3	1	Number of sectors in the SMART Error log
4 – 5	51	Number of sectors in the comprehensive SMART Error log
6 – 7	16383	Number of sectors in the extended comprehensive SMART Error log
96 – 97	9	IDENTIFY DEVICE data
256 – 319	16	Number of sectors in the logs at addresses 0x80 – 0x9F
320 – 321	4	Number of sectors in the log at address 0xA0
322 – 323	1	Number of sectors in the log at address 0xA1
324 – 325	1	Number of sectors in the log at address 0xA2

All other bytes in the Log Directory are zero.
The SMART Error Logs contain entries for internal flash errors or host transfer errors, based on the same data that is returned by the Read Error Log command. If the corresponding host command for a flash error could not be determined, the command code field in the error entry is set to 0xF0. For flash errors that do not correspond to a processed host command, the command code field is set to 0xFF.
The Host Vendor Specific Logs can be used by the host to store and retrieve arbitrary data.

8.2.9.SMART Write Log

COMMAND CODE: B0h with a Feature Register value of D6h

PROTOCOL: PIO data out

INPUTS:

Register	7	6	5	4	3	2	1	0
Features	D6h							
Sector Count	Number of sectors to be written							
Sector Number	Log address							
Cylinder Low	4Fh							
Cylinder High	C2h							
Device/Head	1	1	1	D				
Command	B0h							

NORMAL OUTPUTS: None required.

ERROR OUTPUTS: Aborted if the signature in the Cylinder registers is invalid, the log address or the number of sectors is invalid, or if SMART is not enabled.

DESCRIPTION: This command can be used to write data into the SMART log. Writes are only allowed to the Host Vendor Specific logs, all other log addresses can only be read.

8.2.10. SMART Read Remap Data

COMMAND CODE: B0h with a Feature Register value of E0h

PROTOCOL: PIO data in

INPUTS:

Register	7	6	5	4	3	2	1	0
Features	E0h							
Sector Count	01h							
Sector Number								
Cylinder Low	4Fh							
Cylinder High	C2h							
Device/Head	1	1	1	D				
Command	B0h							

NORMAL OUTPUTS: None required.

ERROR OUTPUTS: Aborted if the signature in the Cylinder registers is invalid, if the Sector Count is not 1, or if SMART is not enabled.

DESCRIPTION: This command returns status information for the internal bad block mapping algorithm. The returned data gives the initial number of flash memory blocks available for remapping bad blocks and the current number of blocks available for remapping bad blocks. All numbers are reported per interleave factor.

The data layout is:

Offset	Description
0 – 31	Initial number of spare blocks for interleave units 1 to 16
32 – 63	Current number of spare blocks for interleave units 1 to 16

8.2.1.SMART Read Wear Level Data

COMMAND CODE: B0h with a Feature Register value of E1h

PROTOCOL: PIO data in

INPUTS:

Register	7	6	5	4	3	2	1	0
Features	E1h							
Sector Count	04h							
Sector Number								
Cylinder Low	4Fh							
Cylinder High	C2h							
Device/Head	1	1	1	D				
Command	B0h							

NORMAL OUTPUTS: None required.

ERROR OUTPUTS: Aborted if the signature in the Cylinder registers is invalid, if the Sector Count is greater than 4, or if SMART is not enabled.

DESCRIPTION: This command returns information regarding the status of the wear leveling. The information returned is the distribution of the blocks into the 1024 possible wear level classes. For each of the non-empty wear level classes, the number of blocks that have this class is returned in the return data.

Offset	Description
0 – 3	Marker bytes, fixed value of 0xFFFFFFFF
4 – 5	Lowest wear level class
6 – 7	Highest wear level class
8 – 15	Wear level class entry 1
16 – 23	Wear level class entry 2
….	….
2040 – 2047	Wear level class entry 255

Each wear level class entry consists of this data:

Offset	Description
0 – 3	Wear level class index
4 – 7	Number of blocks in this wear level class

Unused wear level class entries are zero.

WARNING: This product may contain chemicals known to the State of California to cause cancer, birth defects, or other reproductive harm. For more information go to www.p65warnings.ca.gov.