User's Guide
SLAU780–August 2018

MSP432E411Y-BGAEVM User's Guide

This guide provides an overview on how to get started quickly with the MSP432E411Y-BGAEVM, including power, header pinouts and connections, communication interfaces, and programming interfaces.

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1 Board Overview

The SimpleLink™ Ethernet MSP432E411Y microcontroller EVM is an evaluation platform for SimpleLink Arm® Cortex®-M4F-based Ethernet microcontrollers. The MSP432E411Y-BGAEVM demonstrates the MSP432E411Y microcontroller with its on-chip 10/100 Ethernet MAC and PHY, USB 2.0, LCD controller, External Peripheral Interface (EPI), hibernation module, motion control pulse-width modulation, and a multitude of simultaneous serial connectivity. The MSP432E411Y-BGAEVM also features a fully compliant 40-pin BoosterPack™ plug-in module header, a user switch, two user LEDs, and dedicated reset and wake switches.

The preprogrammed quick start application on the EVM is an application that performs a self-test on the onboard SDRAM by writing and reading back values in memory using the MSP432E411Y EPI. The self-test blinks an LED to indicate that the test passes. Figure 1 shows the MSP432E411Y-BGAEVM with key features highlighted.

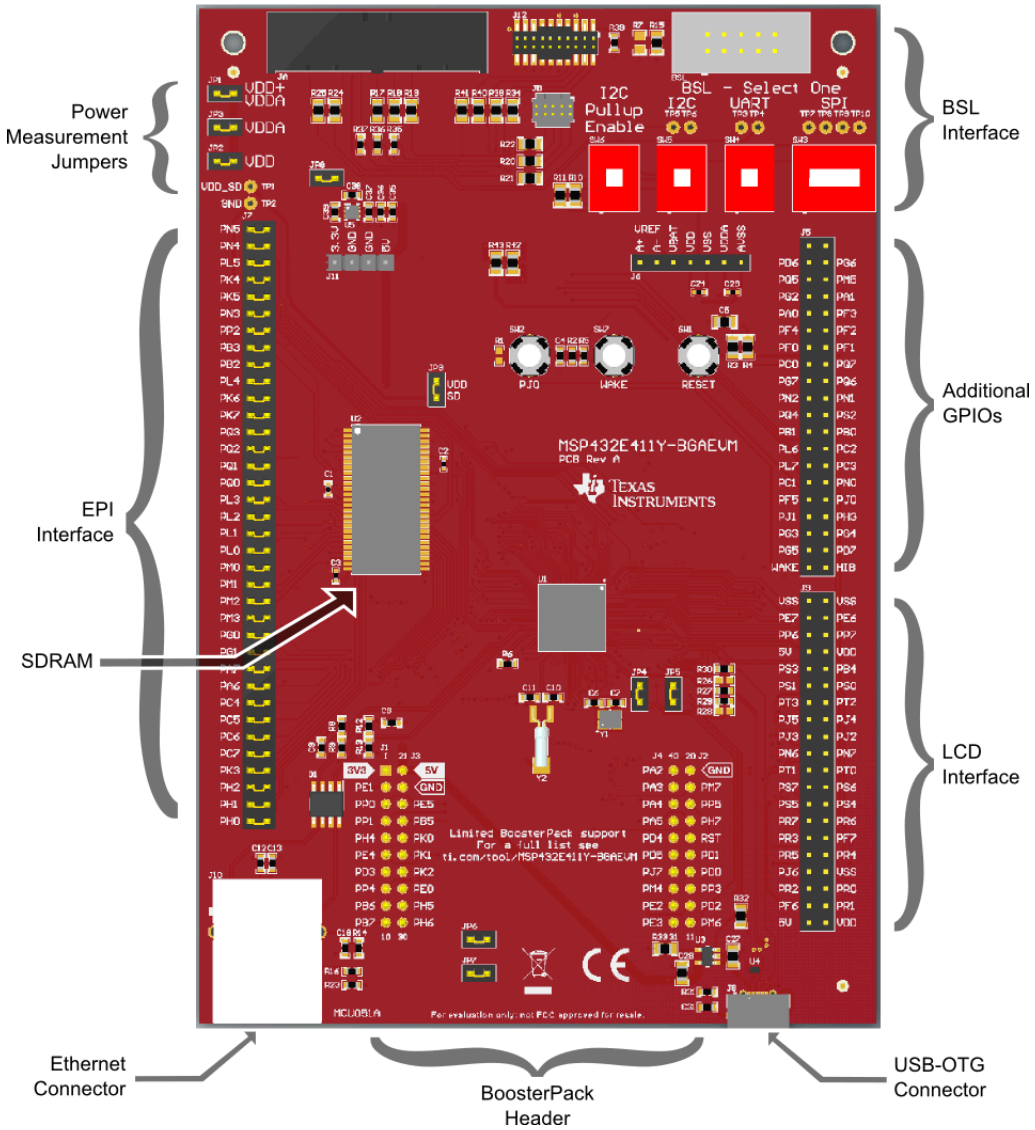

Figure 1. SimpleLink Ethernet MSP432E411Y Evaluation Module

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2 Power the MSP432E411Y-BGAEVM

The MSP432E411Y-BGAEVM requires a 3.3-V power supply, which can be provided in any of several ways:

- Provide 3.3 V from an external emulator through the 20-pin Arm JTAG interface
- Provide 3.3 V directly to the 3.3V pin on the external power header (J11)
- Provide 5 V to the 5V pin on the external power header (J11) and using the onboard LDO to generate 3.3 V
- Provide 3.3 V and 5 V both to the external power header (J11)

2.1 Emulator Power

To use an external emulator as a power source, use an emulator that supplies 3.3 V to pin 1 on the Arm 20-pin JTAG interface. When 3.3 V is supplied to the board from the emulator, disconnect the output of the onboard 3.3-V LDO (U5) from the 3.3-V power rail by removing the jumper on JP8. Figure 2 shows the location of JP8.

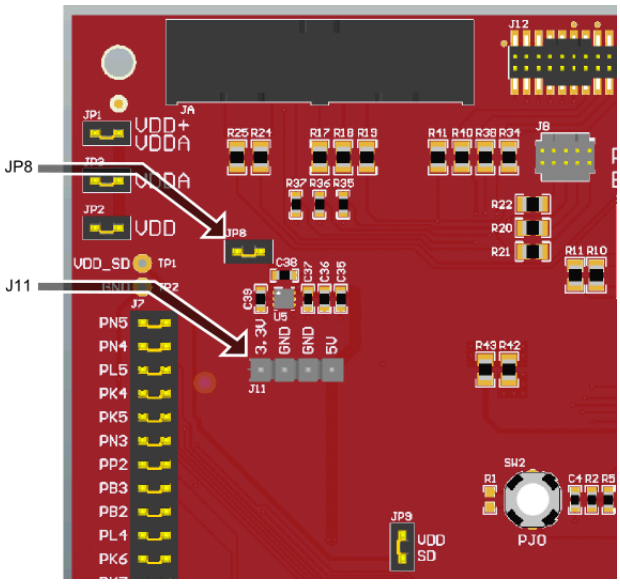

Figure 2. Power Selection

If USB host functionality is required from the onboard USB OTG connector, provide 5 V to the board through the external power header (J11) or the BoosterPack header (J3).

2.2 External 3.3-V Source Only

To use an external 3.3-V source to power the EVM, connect the 3.3-V and GND lines of the supply to the 3.3V and GND pins of the external power header (J11). Disconnect the onboard 3.3-V LDO (U5) from the 3.3-V power rail by removing the jumper on JP8 to prevent back-powering the LDO. Figure 2 shows the location of JP8. If USB host functionality is required from the onboard USB-OTG connector, also provide 5 V to the board. Use the external 3.3-V and 5-V power option in Section 2.4.

2.3 External 5-V Source Only

To use an external 5-V source to power the EVM, connect the 5-V and GND lines of the supply to the 5V and GND pins of the external power header (J11) or to the 5V pin on the BoosterPack header (J3). Connect the onboard 3.3-V LDO (U5) to the 3.3-V power rail by populating the jumper on JP8 to connect the output of the LDO to the 3.3-V power rail. Figure 2 shows the location for JP8.

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2.4 External 3.3-V and 5-V Source

To use external 3.3-V and 5-V supplies to power the EVM, connect the 3.3-V, 5-V, and GND pins of the supply to the 3.3V, 5V, and GND pins of the external power header (J11) or the BoosterPack headers (J1 for 3.3V and J3 for 5V). Disconnect the onboard 3.3-V LDO (U5) from the 3.3-V power rail by removing the jumper on JP8 to prevent back-powering the LDO. Figure 2 shows the location for JP8.

2.5 Measure Current Consumption

To measure current consumption, remove the JP1, JP2, or JP3 jumpers and place an ammeter across the header pins. Connect this jumper when not performing current measurements. Figure 3 shows the location of JP1, JP2, and JP3. Table 1 lists which power rail to measure on each jumper.

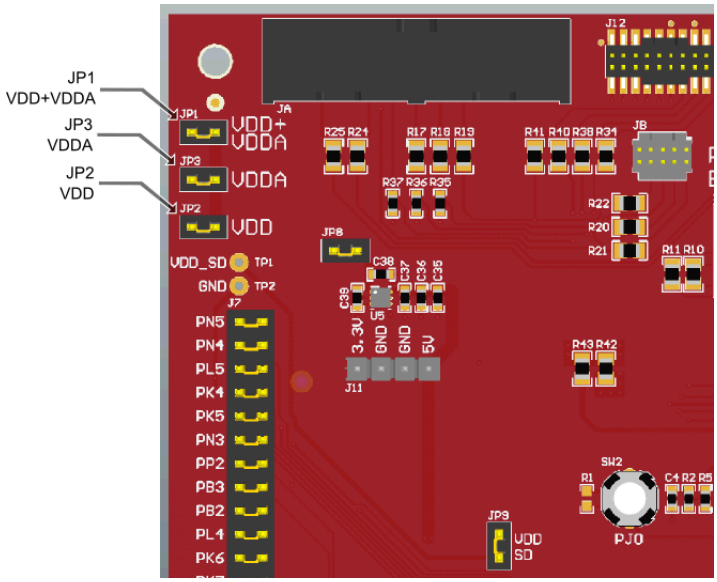

Figure 3. Current Measurement Headers

Table 1. Power Measurement Jumpers

Jumper	Power Rail Measured
JP1	Combined VDD and VDDA
JP2	VDD
JP3	VDDA

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3 Header Pinouts and Connections

3.1 J11 – External Power Connector

Header J11 contains connections for 3.3 V, 5 V, and GND signals and is intended to be used to connect external power supplies to the MSP432E411Y-BGAEVM. Figure 2 shows header J11, and Table 2 lists the pinout.

Table 2. External Power Connector J11 Pinout

J11 Pin	Signal
1	3.3V
2	GND
3	GND
4	5V

3.2 J6 – Power Rail Header

Header J6 contains connections for all the power rails and reference voltages used by the MSP432E411Y device. Figure 4 shows header J6 and Table 3 lists the pinout.

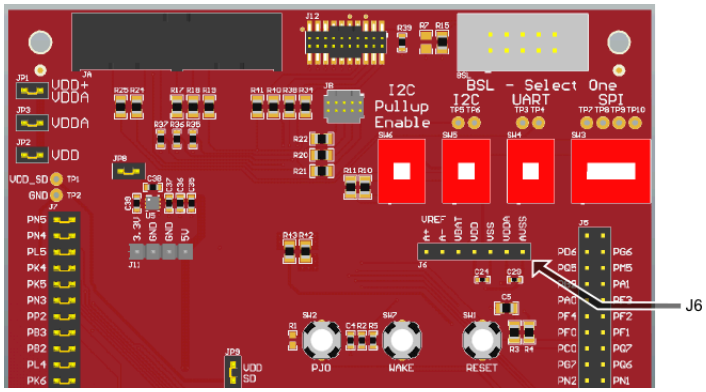

Figure 4. External Power Connector J6

Table 3. External Power Connector J6 Pinout

J6 Pin	Signal	Description
1	VREFA+	Reference voltage for ADC positive input
2	VREFA-	Reference voltage for ADC negative input
3	VBAT	Power source for hibernation module
4	VDD	Positive supply for I/O
5	VSS	Negative supply for I/O
6	VDDA	Positive supply for analog circuits
7	AVSS	Negative supply for analog circuits

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3.3 J7 – External Peripheral Interface Header

Header J7 contains all the signals for the MSP432E411Y's External Peripheral Interface (EPI). The EPI can be connected to an onboard IS42S16320F-7TL – 512 megabit SDRAM, U2, buy shorting all the header pins on J7 horizontally, as shown in Figure 5. Alternatively, the EPI pins can be used to connect to an external device by removing the headers on J7, and connecting to the outside pins of J7, as shown in Figure 6.

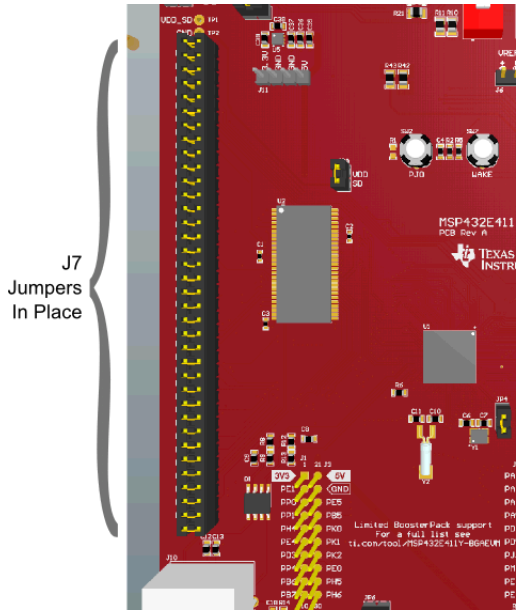

Figure 5. Header J7 With All Jumpers to Connect Onboard SDRAM

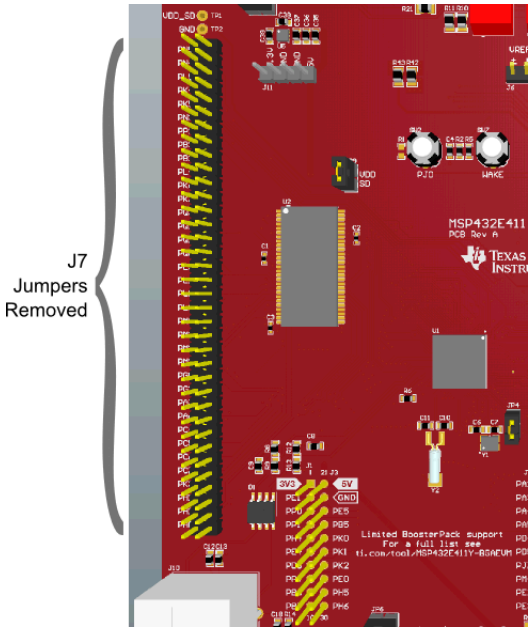

Figure 6. Header J7 With Jumpers Removed to Connect External Device to EPI

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Table 4 lists the pinout of J7.

Table 4. Header J7 Pinout

MSP432E411Y Signal	J7 Pin		J7 Pin	SDRAM Signal
EP0S35	1		2	NC(1)
EP0S34	3		4	NC
EP0S33	5		6	NC
EP0S32	7		8	NC
EP0S31	9		10	CLK
EP0S30	11		12	CKE
EP0S29	13		14	$\overline{CS}$
EP0S28	15		16	$\overline{WE}$
EP0S27	17		18	NC
EP0S26	19		20	NC
EP0S25	21		22	NC
EP0S24	23		24	NC
EP0S23	25		26	NC
EP0S22	27		28	NC
EP0S21	29		30	NC
EP0S20	31		32	NC
EP0S19	33		34	$\overline{RAS}$
EP0S18	35		36	$\overline{CAS}$
EP0S17	37		38	DQMH
EP0S16	39		40	DQML
EP0S15	41		42	DQ15
EP0S14	43		44	BA1, DQ14
EP0S13	45		46	BA0, DQ13
EP0S12	47		48	A12, DQ12
EP0S11	49		50	A11, DQ11
EP0S10	51		52	A10, DQ10
EP0S09	53		54	A9, DQ9
EP0S08	55		56	A8, DQ8
EP0S07	57		58	A7, DQ7
EP0S06	59		60	A6, DQ6
EP0S05	61		62	A5, DQ5
EP0S04	63		64	A4, DQ4
EP0S03	65		66	A3, DQ3
EP0S02	67		68	A2, DQ2
EP0S01	69		70	A1, DQ1
EP0S00	71		72	A0, DQ0

(1) NC = no connection

3.4 LCD Interface Header

Header J9 contains all of the signals for the internal LCD controller in the MSP432E411Y to interface with an external LCD panel, including four additional GPIO pins. The four additional GPIO pins can be used as analog inputs to interface with a resistive touch screen. Alternatively, two of the pins (PE6 and PE7) can be configured as I^2C pins to interface with controllers that require an I^2C interface. Figure 7 shows the location of J9, and Table 5 lists the pinout of J9.

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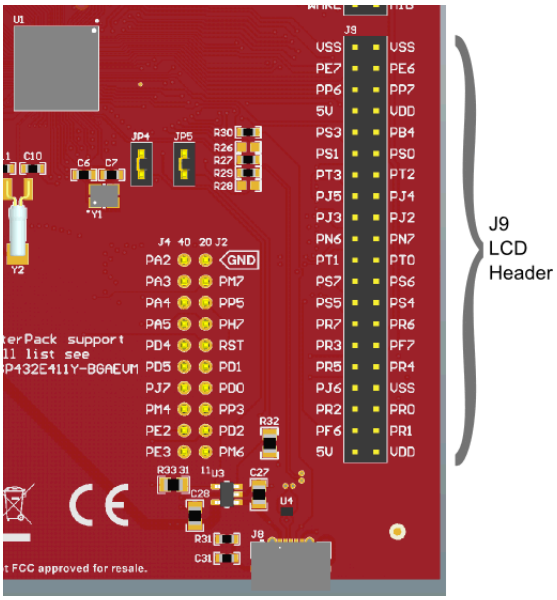

Figure 7. Header J9

Table 5. Header J9 Pinout

GPIO Pin	Function	J9 Pin	J9 Pin	Function	GPIO Pin
GND	GND	40	39	GND	GND
PE7	AIN21/I2C9SDA	38	37	AIN20/I2C9SCL	PE6
PP6	AIN23	36	35	AIN22	PP7
n/a[(1)]	5 V	34	33	3.3 V	VDD
PS3	LCDDATA23	32	31	GPIO	PB4
PS1	LCDDATA21	30	29	LCDDATA20	PS0
PT3	LCDDATA19	28	27	LCDDATA18	PT2
PJ5	LCDDATA17	26	25	LCDDATA16	PJ4
PJ3	LCDDATA15	24	23	LCDDATA14	PJ2
PN6	LCDDATA13	22	21	LCDDATA12	PN7
PT1	LCDDATA11	20	19	LCDDATA10	PT0
PS7	LCDDATA09	18	17	LCDDATA08	PS6
PS5	LCDDATA07	16	15	LCDDATA06	PS4
PR7	LCDDATA05	14	13	LCDDATA04	PR6
PR3	LCDDATA03	12	11	LCDDATA02	PF7
PR5	LCDDATA01	10	9	LCDDATA00	PR4
PJ6	LCDAC	8	7	GND	GND
PR2	LCDLP	6	5	LCDCP	PR0
PF6	LCDMCLK	4	3	LCDFP	PR1
n/a	5 V	2	1	3.3 V	VDD

(1) n/a = not applicable

NOTE: On MSP432E411Y-BGAEVM Rev A boards, LCDDATA22 is not available on the J9 header. If a connection for LCDDATA22 is required, make the connection to J5 pin 19 (MSP432E411Y pin PS2).

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3.5 J1, J2, J3, J4 – BoosterPack Interface Headers

Headers J1, J2, J3, and J4 are aligned correctly and follow the pinout requirements to comply with the BoosterPack plug-in module pinout standard, as shown on www.ti.com/byob. Figure 8 shows the pinouts for the J1, J2, J3, and J4 headers.

1						+3.3V
2			AIN2	U1DSR	(I)	PE1
3		U6RX	SSI3XDAT2	T6CCP0	(I)	PP0
4		U6TX	SSI3XDAT	T6CCP1	(I)	PP1
5				U0DTR	(I)	PH4
6		AIN9	SSI1XDAT0	U1RI	(I)	PE4
7	SSI2CLK	AIN12	T1CCP1	I2C8SDA	(I)	PD3
8		OWIRE	U0DSR	U3RTS	(I)	PP4
9			I2C6SCL	T6CCP0	(I)	PB6
10			I2C6SDA	T6CCP1	(I)	PB7

21							+5V
22							GND
23			AIN8	SSI1XDAT1	(I)	PE5	
24	AIN11	SSI1CLK	U0RTS	I2C5SCL	(I)	PB5	
25			AIN16	U4RX	(I)	PK0	
26			AIN17	U4TX	(I)	PK1	
27			AIN18	U4RTS	(I)	PK2	
28			AIN3	U1RTS	(I)	PE0	
29				U0RI	(I)	PH5	
30			U7RX	U5RX	(I)	PH6	

GND							20
PM7	(I)	U0RI	EN0COL	T5CCP1			19
PP5	(I)	U3CTS	I2C2SCL	OWALT			18
PH7	(I)	U5TX	U7TX				17
RST							16
PD1	(I)	AIN14	I2C7SDA	T0CCP1	C1O	SSI2XDAT0	15
PD0	(I)	AIN15	I2C7SCL	T0CCP0	C0O	SSI2XDAT1	14
PP3	(I)	U1CTS	U0DCD	RTCCLK			13
PD2	(I)	AIN13	I2C8SCL	T1CCP0	C2O	SSI2Fss	12
PM6	(I)	U0DSR	T5CCP0				11

PA2	(I)	U4RX	I2C8SCL	SSI0CLK	T1CCP0	40
PA3	(I)	U4TX	I2C8SDA	SSI0Fss	T1CCP1	39
PA4	(I)	U3RX	I2C7SCL	SSI0XDAT0	T2CCP0	38
PA5	(I)	U3TX	I2C7SDA	SSI0XDAT1	T2CCP1	37
PD4	(I)	U2RX	SSI1XDAT2	T3CCP0		36
PD5	(I)	U2TX	SSI1XDAT3	T3CCP1		35
PJ7	(I)	U4CTS				34
PM4	(I)	U0CTS	T4CCP0			33
PE2	(I)	AIN1	U1DCD			32
PE3	(I)	AIN0	U1DTR	OWIRE		31

Figure 8. BoosterPack Plug-in Module Header Pinout

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3.6 J5 – Additional GPIO Pin Header

Header J5 contains additional GPIO pins that are available for use. Figure 9 shows the location for J5, and Table 6 lists the pinout.

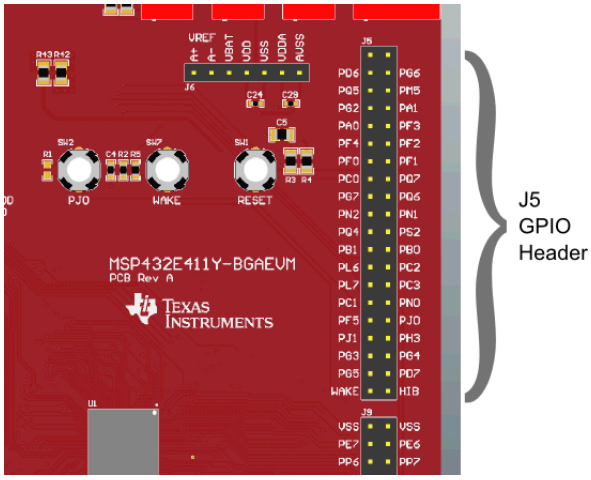

Figure 9. Header J5 Location

Table 6. Header J5 Pinout

MSP432E411Y Pin	J5 Pin		J5 Pin	MSP432E411Y Pin
VDD (3.3 V)	40		39	GND
PD6	38		37	PG6
PQ5	36		35	PM5
PG2	34		33	PA1
PA0	32		31	PF3
PF4	30		29	PF2
PF0	28		27	PF1
PC0	26		25	PQ7
PG7	24		23	PQ6
PN2	22		21	PN1
PQ4	20		19	PS2
PB1	18		17	PB0
PL6	16		15	PC2
PL7	14		13	PC3
PC1	12		11	PN0
PF5	10		9	PJ0
PJ1	8		7	PH3
PG3	6		5	PG4
PG5	4		3	PD7
WAKE	2		1	$\overline{\text{HIB}}$

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4 Communication Interfaces

4.1 Ethernet

The MSP432E411Y-BGAEVM development kit can connect directly to an Ethernet network using RJ45 connectors. The microcontroller contains a fully integrated Ethernet MAC and PHY. This integration creates a simple, elegant, and cost-saving Ethernet circuit design. Example code is available for the lwIP TCP/IP protocol stack. The embedded Ethernet on this device can be programmed to act as an HTTP server, a client, or both. The design and integration of the circuit and microcontroller can also synchronize events over the network using the IEEE 1588 precision time protocol. The existing SimpleLink SDK network stack includes an example of using this feature.

The Ethernet jack on the EVM contains two LEDs, one green and one yellow, that are controlled by pins PN0 and PN1 on the MSP432E411Y. When configured for Ethernet operation, the application should control these pins directly, because the PHY-controlled LED pins have not been provided for LED function.

4.2 USB-OTG

The EVM is USB 2.0 ready. A TPS2051B power switch is connected to and controlled by the microcontroller USB peripheral, which manages power to the USB micro A/B connector when functioning in a USB host. When functioning as a USB device, apply power to the EVM from an external source, (see Section 2). USB 2.0 functionality is provided and supported directly out of the box with the target USB micro A/B connector.

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5 Programming Interfaces

5.1 JTAG

The MSP432E411Y-BGAEVM supports JTAG programming through two different connectors. JA supports the 20-pin Arm standard JTAG programming interface, and JB supports the 10-pin Arm standard mini-JTAG programming interface. Figure 10 shows the two Arm JTAG connectors. When using an external emulator, if the emulator does not provide power to the board, apply power as described in Section 2.

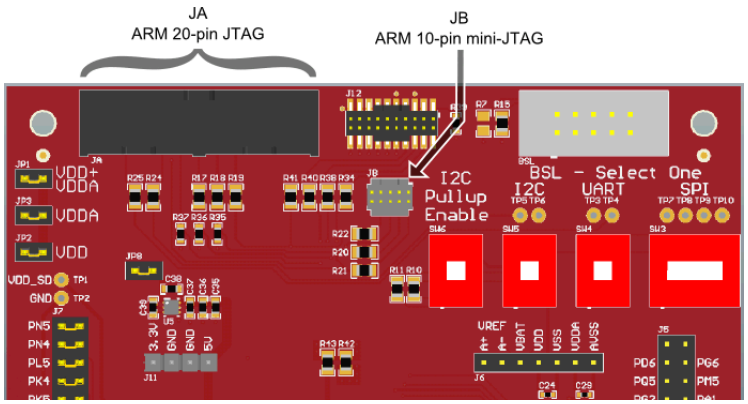

Figure 10. Arm JTAG Connectors

5.2 ETM Trace

The MSP432E411Y-BGAEVM supports ETM Trace capabilities through J12 (see Figure 11).

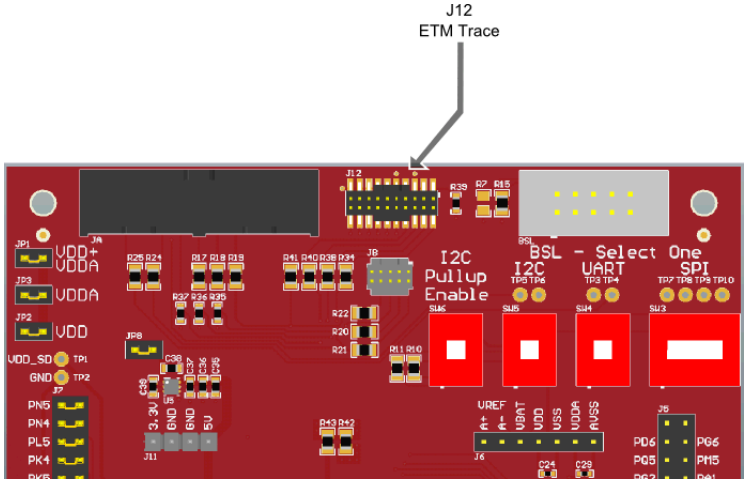

Figure 11. Arm ETM Trace Connector

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5.3 BSL

The MSP432E411Y-BGAEVM supports BSL communication with the MSP432E411Y device through UART, I²C, or SPI BSL. Three switch banks (S3, S4, and S5) control which BSL interface is connected to the BSL connector, BSL. Move the corresponding switch for the desired BSL interface to the ON position, and move the other switches to the OFF position. Figure 12 shows the BSL switches and the BSL connector, with the switches in position to enable the SPI BSL interface. Table 7 shows which switch bank controls which BSL Interface. Switch bank S6 connects 4.7-kΩ resistors to the I²C BSL lines if I²C pullups are needed.

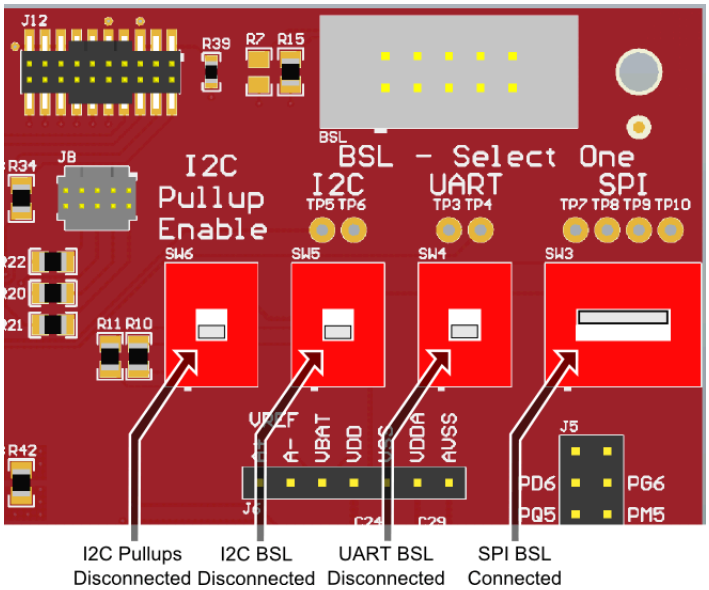

Figure 12. BSL Area on MSP432E411Y-BGAEVM

Table 7. BSL Switch Bank Interfaces

Switch Bank	BSL Interface
SW3	SPI
SW4	UART
SW5	I²C

When connecting to the MSP432E411Y device through the BSL connector:

- If R15 is populated and R7 is not (the default), the BSL host supplies the 3.3-V rail.
- If R7 is populated and R15 is not, the BSL host can sense the 3.3-V rail, which must be externally supplied to the MSP432E411Y-BGAEVM.

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6 Software Development

6.1 Software Description

The SimpleLink MSP432E4 Software Development Kit (SDK) provides drivers for all of the peripheral devices supplied in the design. The Peripheral Driver Library is required to operate the on-chip peripherals as part of the SDK. The SDK includes a set of example applications that use the Peripheral Driver Library. These applications demonstrate the capabilities of the MSP432E411Y microcontroller and provide a starting point for the development of the final application for use on the MSP432E411Y-BGAEVM.

6.2 Source Code

The source code is provided as part of the SimpleLink MSP432E4 SDK.

6.3 Tool Options

The source code installation includes directories containing projects, makefiles, and binaries for the following tool-chains:

- Keil® Arm RealView Microcontroller Development System
- IAR Embedded Workbench® for Arm
- TI Code Composer Studio™ IDE for Arm and GCC compilers

For detailed information on using these tools, see the documentation included in the tool chain installation or visit the website of the tools supplier.

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7 Schematics

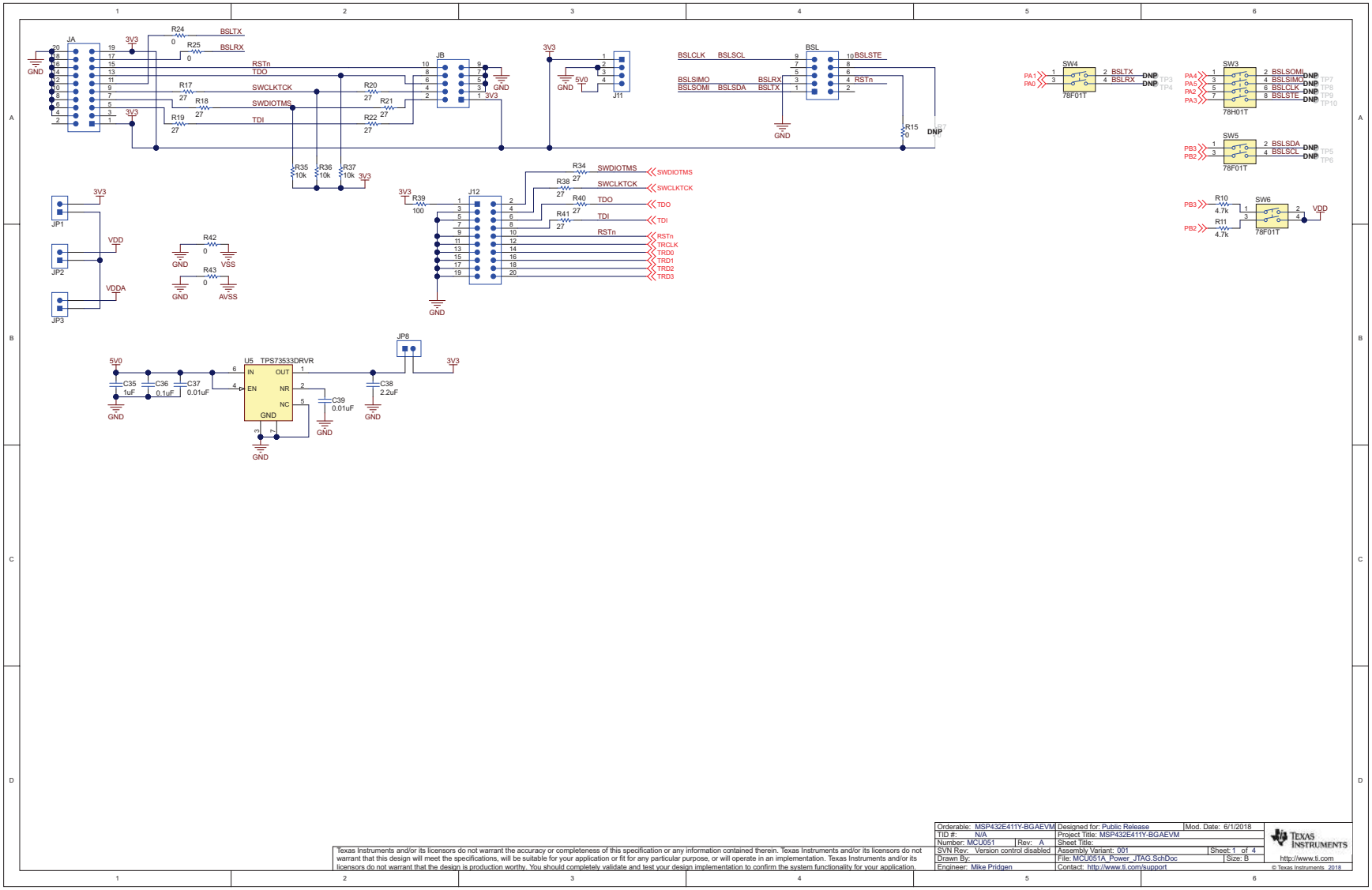

Figure 13. Schematics (1 of 3)

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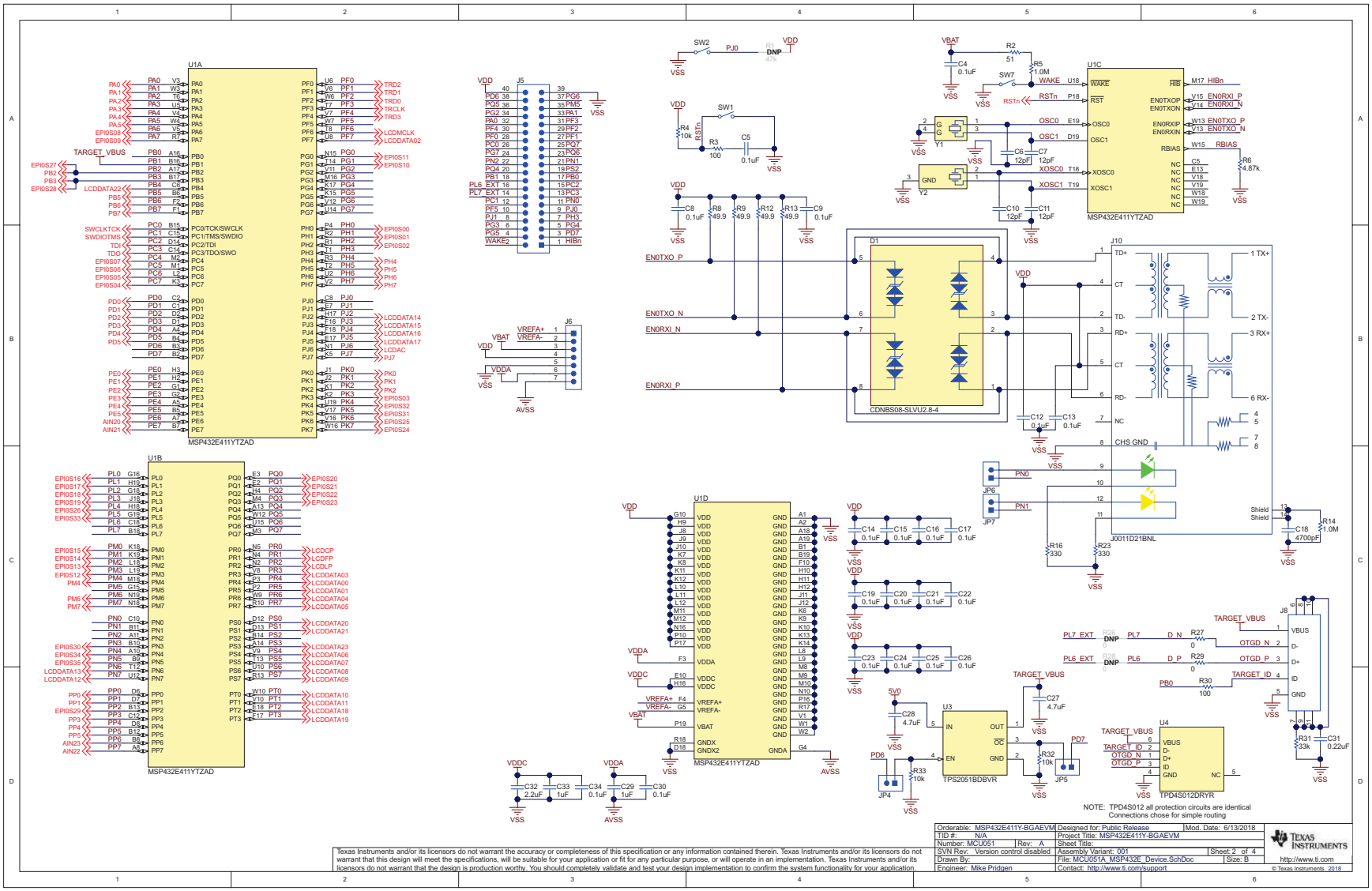

Figure 14. Schematics (2 of 3)

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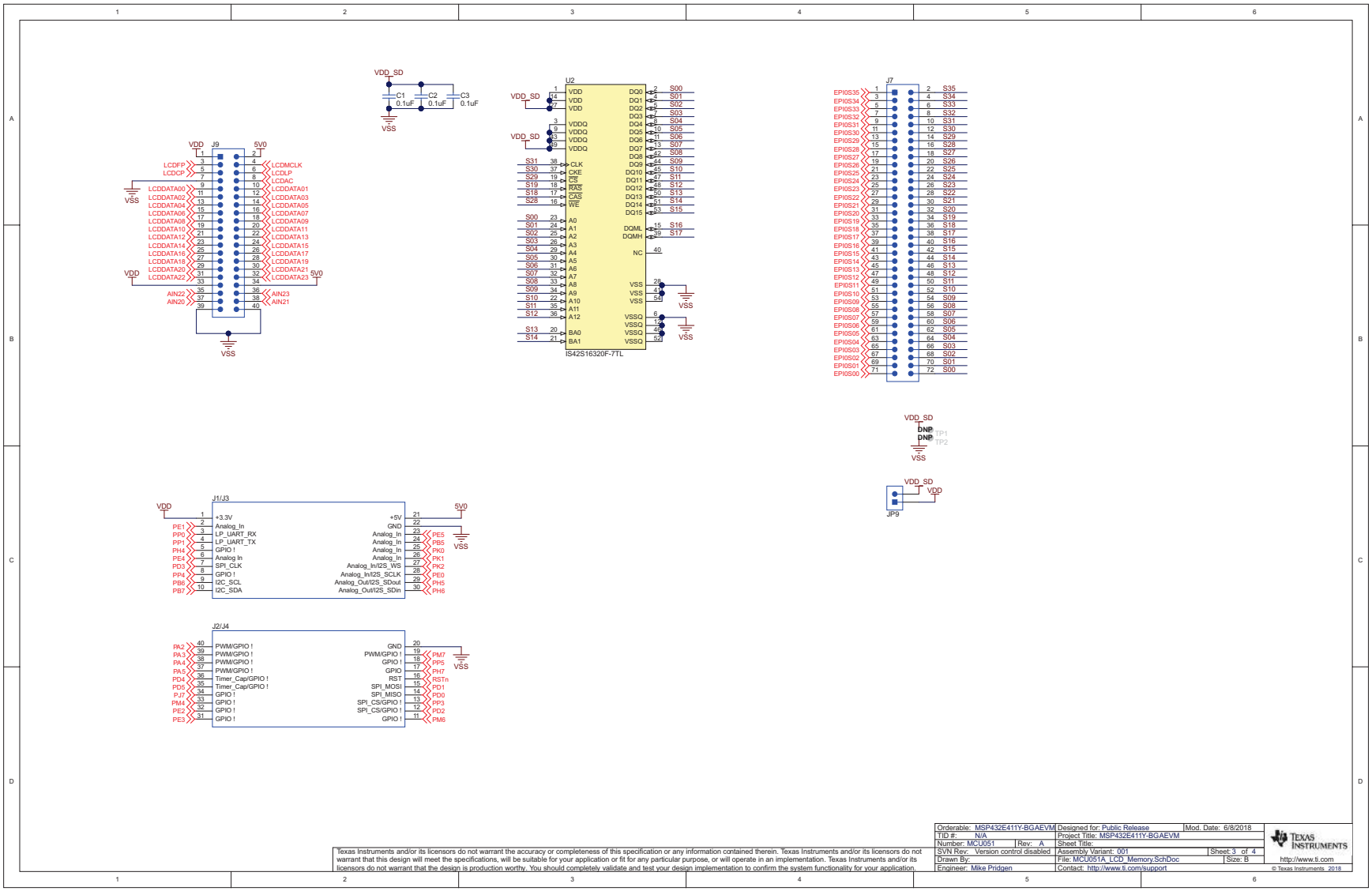

Figure 15. Schematics (3 of 3)

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