# TPSM846C24 4.5-V to 15-V Input, 0.5-V to 2-V Output, 35-A Power Module

## 1 Features

- Complete Integrated 35-A Power Solution
- Pin Compatible With TPSM846C23 (PMBus)
- Stackable up to 70 A With Current Sharing
- Output Voltage Range 0.5 V to 2 V
- Output Voltage Accuracy as Tight as 0.5%
- 15 mm × 16 mm Footprint (6.4 mm Maximum Height)
- 300-kHz to 1-MHz Switching Frequency
- Synchronization to an External Clock
- Differential Remote Sense
- Power-Good Output
- Prebias Output Monotonic Start-up
- Fixed 3-ms Soft-Start / Soft-Stop Time
- Overcurrent Protection
- Operating IC Junction Range: –40°C to +125°C
- Operating Ambient Range: –40°C to +105°C
- Enhanced Thermal Performance: 8.7°C/W
- Meets EN55022 Class A Emissions
- Create a Custom Design Using the TPSM846C24 With the WEBENCH® Power Designer

## 2 Applications

- Compact PCI / PCI Express / PXI Express
- Broadband and Communications Infrastructure
- Automated Test and Medical Equipment
- DSP, FPGA, and ASIC Point-of-Load Applications

## 3 Description

The TPSM846C24 is a 35-A, fixed-frequency, step-down power module. The module incorporates the controller, power MOSFETs, inductor, and associated components into a rugged, thermally enhanced, surface-mount package. The user supplies the input and output capacitors along with a few other passive components to set the operating parameters of the module. Two modules can be configured to work in parallel to provide up to a 70-A, two-phase power solution.

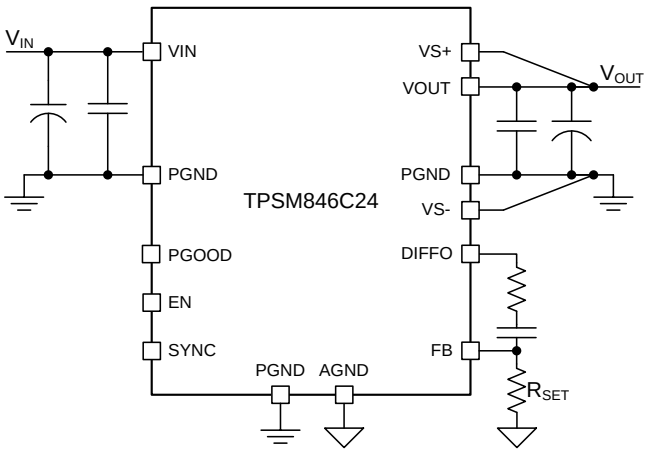
The 15 mm × 16 mm component footprint is easy to solder onto a printed circuit board and allows a compact, point-of-load design.

**Device Information**(1)

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TPSM846C24 | MOL (59) | 15 mm × 16 mm |

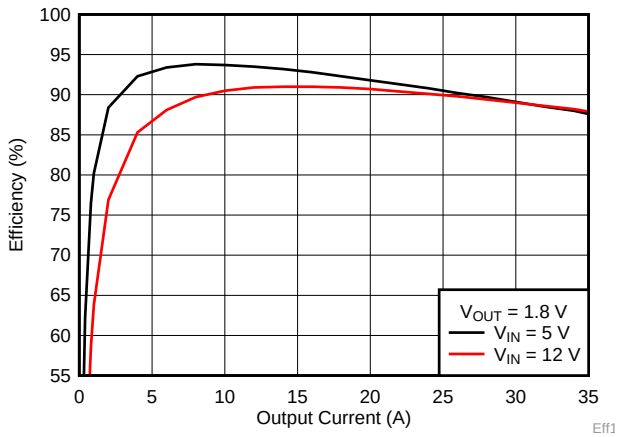
(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Simplified Schematic**






**Efficiency vs Output Current**



# Table of Contents



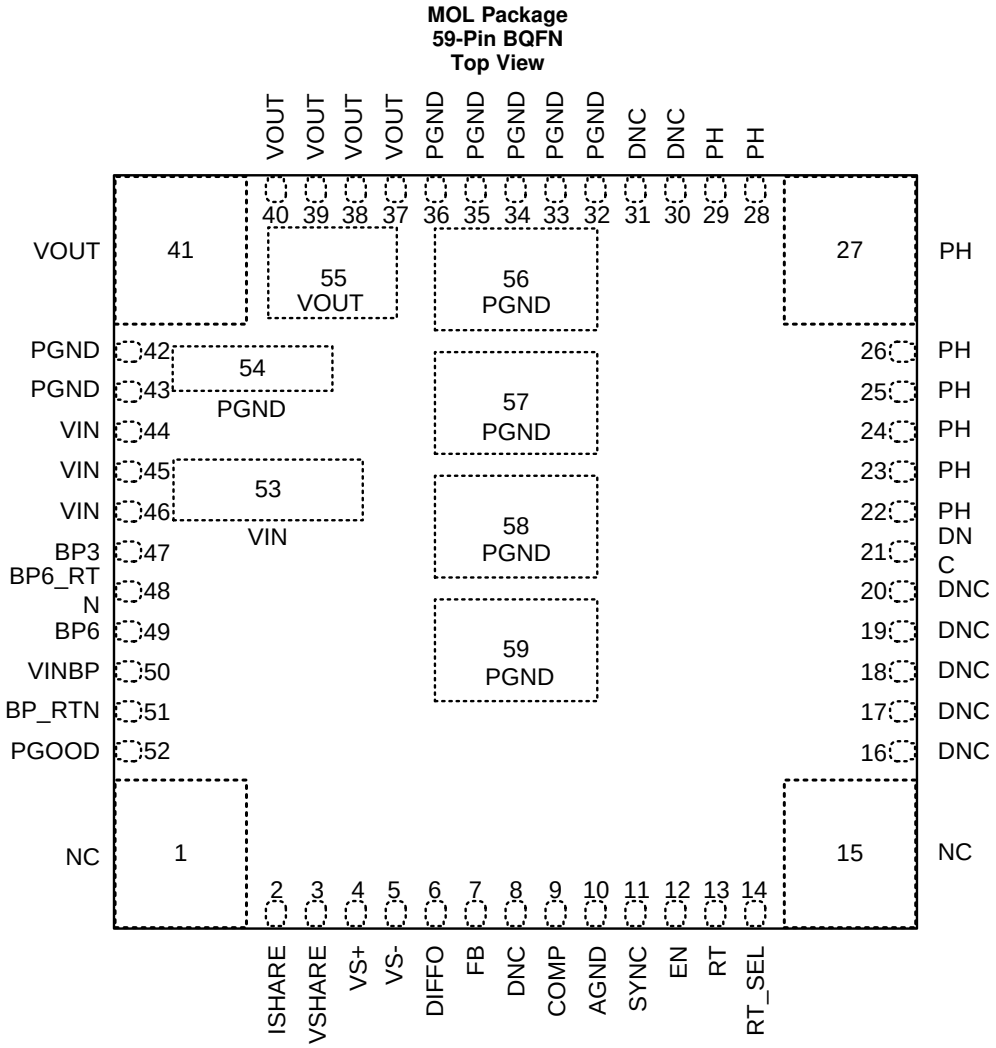
## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision A (August 2018) to Revision B | Page |
|---|---|
| • Changed HBM ESD from 500 to 1000V | 5 |

| Changes from Original (January 2018) to Revision A | Page |
|---|---|
| • Updated PCB Top-side Layout Recommendation figure | 25 |

# 5 Pin Configuration and Functions



## Pin Functions

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| AGND | 10 | G | Analog ground for the controller circuitry. This pin is internally connected to PGND. |
| BP_RTN | 51 | G | Return path for VINBP and BP3. This pin is internally connected to PGND, pad 59. |
| BP3 | 47 | O | Output of the internal 3.3-V regulator. Bypass this pin with a minimum of 2.2-µF to BP_RTN. Can be used as a pullup termination voltage for PGOOD and EN signals. |
| BP6 | 49 | O | Output of the internal 6.5-V regulator that powers the driver stage of the device. Bypass this pin with a minimum of 2.2 µF to BP6_RTN. |
| BP6_RTN | 48 | G | Power ground return path for BP6 bypass cap. |
| COMP | 9 | O | Output of the error amplifier. |
| DIFFO | 6 | O | Output of the remote sense differential amplifier. This provides remote sensing for output voltage reporting and the voltage control loop. |
| DNC | 8, 16, 17, 18, 19, 20, 21, 30, 31 | – | Do Not Connect. Do not connect these pins to AGND, PGND to a different DNC pin or to any other voltage. These pins are connected to internal circuitry. Each pin must be soldered to an isolated pad. |
| EN | 12 | I | EN pin. To enable, pull this pin up to a voltage less than 5.5 V using a 10-kΩ resistor. Pull this pin to AGND to disable the device. |
| FB | 7 | I | Feedback pin for the control loop. |
| ISHARE | 2 | I | Current sharing signal for parallel operation. |
| NC | 1, 15 | – | Not Connected. These pins are internally isolated from any signal and all other pins. Each pin must be soldered to a pad on the PCB. These pins can be left isolated, or connected to AGND or PGND. |
| PGND | 32, 33, 34, 35 36, 42, 43, 54 56, 57, 58, 59 | G | Power ground of the device. This is the return current path for the power stage of the device. Connect these pins to the bypass capacitors associated with VIN and VOUT. Connect pads 56, 57, 58, and 59 to the PCB ground planes using multiple vias for optimal thermal performance. All pins must be connected together externally with a copper plane or pour directly under the device. |
| PGOOD | 52 | O | Power-good indicator. This pin is an open-drain output, which asserts low during any fault conditions. Requires a pullup resistor. |
| PH | 22, 23, 24, 25 26, 27, 28, 29 | O | Phase switch node. Do not connect any external components to these pins or tie them to a pin of a different function. |
| RT | 13 | I | Frequency-setting resistor. To operate the device at its default switching frequency, make no connection to this pin. To operate at a different switching frequency, connect a resistor from this pin to AGND. |
| RT_SEL | 14 | I | RT resistor select. To operate the device at its default switching frequency, connect this pin to AGND. To operate at a different switching frequency, let this pin float. |
| SYNC | 11 | I/O | Frequency synchronization pin. In a stand-alone application or as the Master device in a parallel configuration, the SYNC pin is configured as a SYNC-IN pin and power conversion is synchronized to the rising edge of a 50% duty cycle external clock applied to this pin. For a slave device in a parallel configuration, power conversion is synchronized to the falling edge of the incoming clock. |
| VIN | 44, 45, 46, 53 | I | Input switching voltage pins. These pins supply voltage to the power switches of the converter. |
| VINBP | 50 | I | Input power to the controller circuitry. Bypass this pin with a minimum of 1-µF to BP_RTN. This pin is internally connected to VIN. |
| VOUT | 37, 38, 39, 40, 41, 55 | O | Output voltage. These pins are connected to the internal output inductor. Connect these pins to the output load and connect external bypass capacitors between these pins and PGND. |
| VS+ | 4 | I | Positive input of the remote sense amplifier. Connect this pin to VOUT at the load for best voltage regulation. Do not let this pin float. |
| VS– | 5 | I | Negative input of the remote sense amplifier. Connect this pin to ground at the load for best voltage regulation. Do not let this pin float. |
| VSHARE | 3 | I/O | Voltage sharing signal for parallel operation. |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Input voltage | VIN | –0.3 | 18 | V |
| | VIN < 2-ms transient | | 19 | |
| | VIN–PH (VIN TO PH differentially) | –0.3 | 25 | |
| | FB | –0.3 | 3.6 | |
| | VS+, VS–, RT, EN, SYNC, PGOOD, ISHARE, RT_SEL | –0.3 | 7 | |
| | BP6_RTN, BP_RTN, AGND | –0.3 | 0.3 | |
| Output voltage | PH | –1 | 25 | V |
| | PH < 100-ns transient | –5 | 25 | |
| | BP6, COMP, DIFFO, VSHARE | –0.3 | 7 | |
| | BP3 | –0.3 | 3.6 | |
| Operating IC junction temperature, $T_J$ | | –40 | 150 | °C |
| Storage temperature, $T_{stg}$ | | –55 | 150 | °C |
| Mechanical shock | | | 500 | G |
| Mechanical vibration | | | 10 | G |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±1000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±1500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Input voltage | VIN | 4.5 | 12 | 15 | V |
| | SYNC | | 3.3 | 6.5 | |
| | EN, PGOOD pullup voltage | | 3.3 | 5.5 | |
| Output voltage | $V_{OUT}$ | 0.5 | | 2 | V |
| Output current | $I_{OUT}$ | 0 | | 35 | A |
| Frequency | | 300 | 500 | 1000 | kHz |
| Temperature | Operating ambient temperature | –40 | | 105 | °C |
| | Operating IC junction temperature | –40 | | 125 | °C |

## 6.4 Thermal Information

| THERMAL METRIC[1] | | TPSM846C24 MOL (QFN) 59 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance[2] | 8.7 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter[3] | 0.9 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter[4] | 4.3 | °C/W |

(1) For more information about thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The junction-to-ambient thermal resistance, $R_{\theta JA}$, applies to devices soldered directly to a 100 mm × 100 mm, 6-layer PCB with 2 oz. copper and natural convection cooling. Additional airflow reduces $R_{\theta JA}$.
(3) The junction-to-top characterization parameter, $\psi_{JT}$, estimates the junction temperature, $T_J$, of a device in a real system, using a procedure described in JESD51-2A (section 6 and 7). $T_J = \psi_{JT} \times Pdis + T_T$; where Pdis is the power dissipated in the device and $T_T$ is the temperature of the top of the device.
(4) The junction-to-board characterization parameter, $\psi_{JB}$, estimates the junction temperature, $T_J$, of a device in a real system, using a procedure described in JESD51-2A (sections 6 and 7). $T_J = \psi_{JB} \times Pdis + T_B$; where Pdis is the power dissipated in the device and $T_B$ is the temperature of the board 1mm from the device.

## 6.5 Electrical Characteristics

Over –40°C to 105°C free-air temperature range, $V_{IN}$ = 12 V, $V_{OUT}$ = 1.2 V, $I_{OUT} = I_{OUT(max)}$, $f_{SW}$ = 500 kHz, $C_{IN1}$ = 4 × 22 µF, 25 V, 1210 ceramic; $C_{IN2}$ = 2 × 330 µF, 25 V, electrolytic bulk; $C_{OUT1}$ = 4 × 47 µF, 6.3 V, 1210 ceramic; $C_{OUT2}$ = 2 × 470 µF, 6.3 V, polymer bulk (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **INPUT VOLTAGE ($V_{IN}$)** | | | | | | |
| $V_{IN}$ | Input voltage | Over $I_{OUT}$ range | 4.5 | | 15 | V |
| $V_{IN\_UVLO}$ | $V_{IN}$ undervoltage lock out | $V_{IN}$ rising | | 4.5 | | V |
| | | $V_{IN}$ falling | | 4 | | |
| $I_{VIN}$ | Input operating current | EN = 0 V | | 7.7 | 12 | mA |
| **OUTPUT VOLTAGE ($V_{OUT}$)** | | | | | | |
| $V_{OUT}$ | $V_{OUT}$ adjustable range[1] | Over $I_{OUT}$ range | 0.5 | | 2 | V |
| | Setpoint voltage tolerance | $R_{SET}$ = Not loaded, $T_J$ = 25°C, $I_{OUT}$ = 0 A | –1% | | 1% | |
| | | $R_{SET}$ = 10 kΩ, 1%, $T_J$ = 25°C, $I_{OUT}$ = 0 A[2] | –1.5% | | 1.5% | |
| | Temperature variation | 0°C < $T_J$ < 85°C, $I_{OUT}$ = 0 A[1] | –0.5% | | 0.5% | |
| | | –40°C < $T_J$ < 125°C, $I_{OUT}$ = 0 A[1] | –1% | | 1% | |
| | Line regulation | 4.5 V < $V_{IN}$ < 15 V, $I_{OUT}$ = 0 A | | ±0.05% | | |
| | Load regulation | Over $I_{OUT}$ range, using remote sense | | ±0.2% | | |
| | Output voltage ripple | 20-MHz bandwidth | | 13 | | mV |
| **OUTPUT CURRENT** | | | | | | |
| $I_{OUT}$ | Output current | Natural Convection. See SOA graph for derating over temperature. | 0 | | 35 | A |
| | Overcurrent threshold | | | 42 | | A |
| $I_{OC(acc)}$ | Overcurrent accuracy | | –15% | | 15% | |
| $I_{SH(acc)}$ | Output current share accuracy | ($I_{OUT1}$ – $I_{OUT2}$) ÷ $I_{TOTAL}$, $I_{OUT}$ ≥ 20 A per module[1] | –15% | | 15% | |
| | | ($I_{OUTx}$ – $I_{TOTAL}$) ÷ 2, $I_{OUT}$ < 20 A per module[1] | –3 | | 3 | A |
| **SOFT START / STOP** | | | | | | |
| $t_{SStart}$ | Internal soft-start time | | | 3 | | ms |
| $t_{SStop}$ | Internal soft-stop time | | | 3 | | ms |
| **ENABLE (EN)** | | | | | | |
| $V_{EN}$ | Enable threshold voltage | Enable high voltage | 1.3 | | | V |
| | | Enable low voltage | | | 0.8 | V |
| | Hysteresis on Enable | | | 170 | | mV |

(1) Specified by design.
(2) The stated limit of the set-point tolerance includes the tolernace of both the internal voltage reference and the internal adjustment resistor. The overall output voltage tolerance is affected by the tolerance of the external $R_{SET}$ resistor.

## Electrical Characteristics (continued)

Over –40°C to 105°C free-air temperature range, $V_{IN}$ = 12 V, $V_{OUT}$ = 1.2 V, $I_{OUT}$ = $I_{OUT(max)}$, $f_{SW}$ = 500 kHz, $C_{IN1}$ = 4 × 22 µF, 25 V, 1210 ceramic; $C_{IN2}$ = 2 × 330 µF, 25 V, electrolytic bulk; $C_{OUT1}$ = 4 × 47 µF, 6.3 V, 1210 ceramic; $C_{OUT2}$ = 2 × 470 µF, 6.3 V, polymer bulk (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **POWER GOOD (PGOOD) AND OVERVOLTAGE / UNDERVOLTAGE THRESHOLD**(3) | | | | | | | |
| PGOOD | PGOOD output low voltage | $V_{IN}$ = 4 V, $V_{OUT}$ = 0 V, $I_{PGOOD}$ = 5 mA | | | | 0.3 | V |
| | | $V_{IN}$ = 0 V, $I_{PGOOD}$ = 80 µA | | | | 0.8 | |
| | PGOOD thresholds | $V_{OUT}$ rising | Good | | 95 | | $\%V_O$ |
| | | | Fault | | 112 | | $\%V_O$ |
| | | $V_{OUT}$ falling | Good | | 105 | | $\%V_O$ |
| | | | Fault | | 88 | | $\%V_O$ |
| **PERFORMANCE** | | | | | | | |
| Efficiency(4) | | $V_{IN}$ = 12 V, $I_{OUT}$ = 25 A | $V_{OUT}$ = 0.8 V | | 83% | | |
| | | | $V_{OUT}$ = 1.2 V | | 87% | | |
| | | | $V_{OUT}$ = 1.8 V | | 90% | | |
| | | $V_{IN}$ = 5 V, $I_{OUT}$ = 25 A | $V_{OUT}$ = 0.8 V | | 84% | | |
| | | | $V_{OUT}$ = 1.2 V | | 88% | | |
| | | | $V_{OUT}$ = 1.8 V | | 91% | | |
| Transient response(4) | | 10 A / µs load step from 25% to 75% of $I_{OUT(max)}$, $C_{OUT}$ = 1000 µF, RC = 1 kΩ, CC = 1 nF | $V_{OUT}$ over/undershoot | | 60 | | mV |
| | | | Recovery time | | 60 | | µs |
| | | 10 A / µs load step from 25% to 75% of $I_{OUT(max)}$, $C_{OUT}$ = 2000 µF, RC = 665 Ω, CC = 1.5 nF | $V_{OUT}$ over/undershoot | | 40 | | mV |
| | | | Recovery time | | 60 | | µs |
| | | 10 A / µs load step from 25% to 75% of $I_{OUT(max)}$, $C_{OUT}$ = 4000 µF, RC = 499 Ω, CC = 2.2 nF | $V_{OUT}$ over/undershoot | | 27 | | mV |
| | | | Recovery time | | 60 | | µs |
| **INTERNAL LDO (BP6, BP3)**(3) | | | | | | | |
| $V_{BP6}$ | BP6 regulator output voltage | 7.5V ≤ $V_{IN}$ ≤ 15 V, switching | | 5.85 | 6.4 | 6.95 | V |
| $V_{BP6(DO)}$ | Dropout voltage | ($V_{VIN}$ – $V_{BP6}$), $V_{IN}$ = 4.5 V, switching | | | | 400 | mV |
| $V_{BP3}$ | BP3 regulator output voltage | $V_{IN}$ ≥ 4.5 V | | 3 | 3.2 | 3.4 | V |
| **THERMAL SHUTDOWN** | | | | | | | |
| $T_{SD}$ | Junction thermal shutdown temperature | | | | 145 | 160 | °C |
| $T_{HYST}$ | Thermal shutdown hysteresis | | | | 25 | | °C |
| **CAPACITANCE** | | | | | | | |
| $C_{IN}$ | External input capacitance | ceramic | | 88 | | | µF |
| | | non-ceramic | | | 660 | | |
| $C_{OUT}$ | External output capacitance | ceramic(5) | | 188 | | | µF |
| | | non-ceramic(5) | | 940 | | 4000(6) | |
| | | | ESR (7) | | | 5 | mΩ |

(3) Functionality Verified. Limits specified at internal IC test.
(4) Specified by design.
(5) The minimum required output capacitance consists of 4 × 47-µF ceramic capacitors and 2 × 470-µF, 10-mΩ ESR (5 mΩ equivalent).
(6) The proper frequency compensation network values are determined by the total amount of output capacitance (see Setting the Compensation Network).
(7) The maximum ESR refers to the combined equivalent ESR of all non-ceramic output capacitors. For example, two 10-mΩ ESR capacitors have a combined equivalent ESR of 5 mΩ.

## 6.6 Switching Characteristics

Over –40°C to 105°C free-air temperature range, $V_{IN}$ = 12 V,$V_{OUT}$ = 1.2 V, $I_{OUT}$ = $I_{OUT(max)}$ , $f_{SW}$ = 500 kHz, $C_{IN1}$ = 4 × 22-µF, 25-V, 1210 ceramic; $C_{IN2}$ = 2 × 330-µF, 25-V, electrolytic bulk; $C_{OUT1}$ = 4 × 47-µF, 6.3-V, 1210 ceramic; $C_{OUT2}$ = 2 × 470-µF, 6.3-V, polymer bulk (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **OSCILLATOR** | | | | | | |
| $f_{SW}$ | Switching frequency | Factory default setting. $R_{RT}$ = open; RT_SEL grounded | 425 | 500 | 575 | kHz |
| | | $R_{RT}$ = 68.1 kΩ, 1%; RT_SEL open | 255 | 300 | 345 | |
| | | $R_{RT}$ = 20.0 kΩ, 1%; RT_SEL open | 850 | 1000 | 1150 | |
| | | Adjustment range | 300 | | 1000 | |
| **PWM** | | | | | | |
| $t_{ON-MIN}$ | Minimum on-time(1) | | | 50 | 100 | ns |
| $t_{OFF-MIN}$ | Minimum off-time(1) | $f_{SW}$ = 1 MHz | | 515 | 560 | ns |
| **SYNCHRONIZATION** | | | | | | |
| $V_{IH(sync)}$ | High-level input voltage(2) | | 2.2 | | | V |
| $V_{IL(sync)}$ | Low-level input voltage(2) | | | | 0.8 | V |
| $D_{SYNC}$ | Sync input duty cycle | $f_{SW}$ = 300 kHz to 1 MHz | | 50% | | |
| $f_{SYNC}$ | Sync frequency range | | 300 | | 1000 | kHz |

(1) Specified by design.
(2) Functionality Verified. Limits specified at internal IC test.

## 6.7 Typical Characteristics ($V_{IN}$ = 12 V)

$V_{IN}$ = 12 V, $T_A$ = 25°C, $f_{SW}$ = 500 kHz (unless otherwise specified). Safe operating area curves were measured using a Texas Instruments evaluation module (EVM).

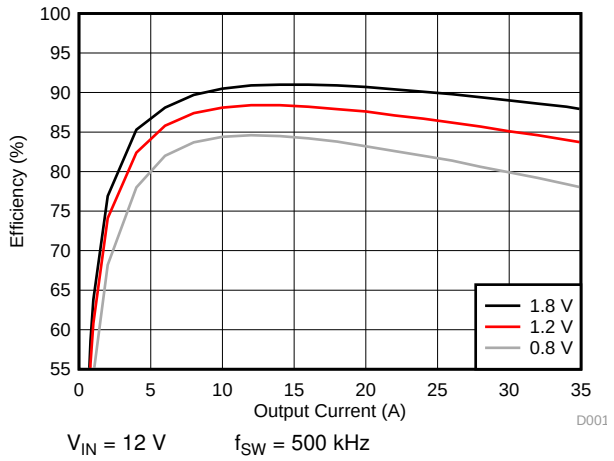



**Figure 1. Efficiency vs Output Current**

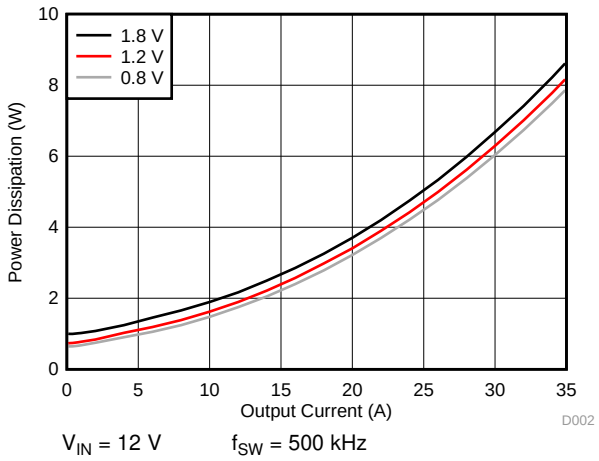



**Figure 2. Power Dissipation vs Output Current**

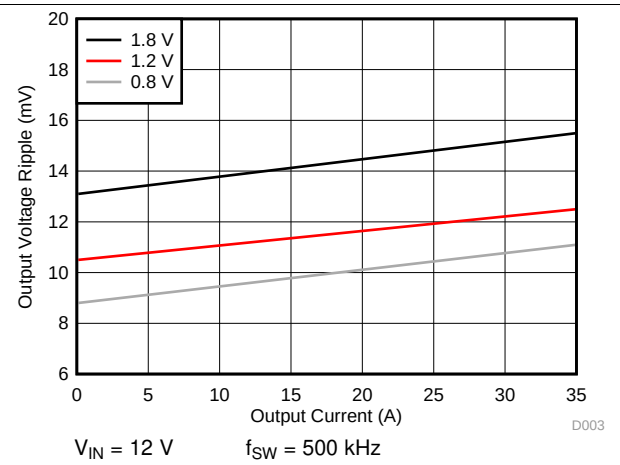



**Figure 3. Voltage Ripple vs Output Current**

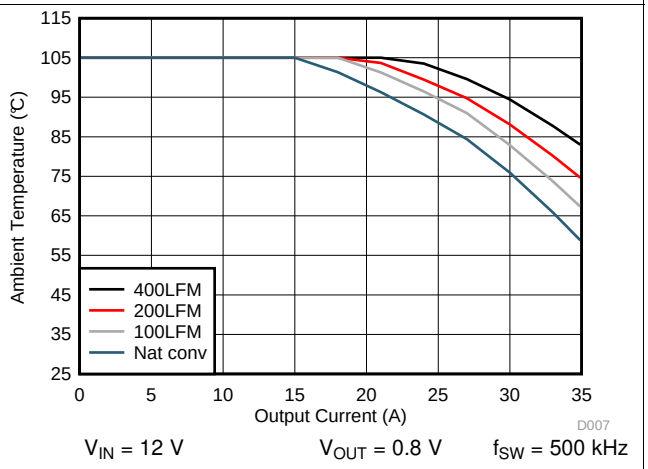



**Figure 4. Safe Operating Area**

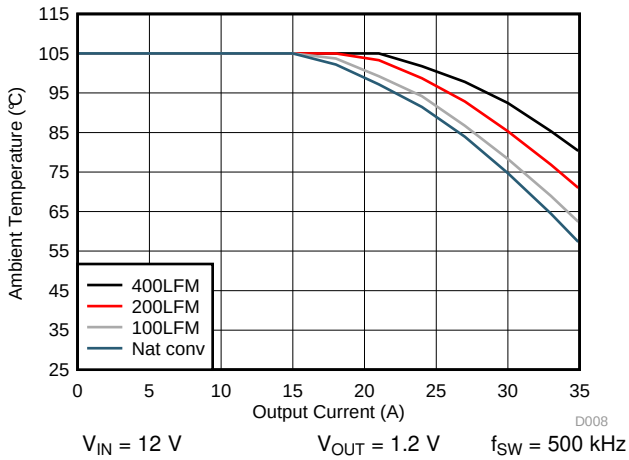



**Figure 5. Safe Operating Area**

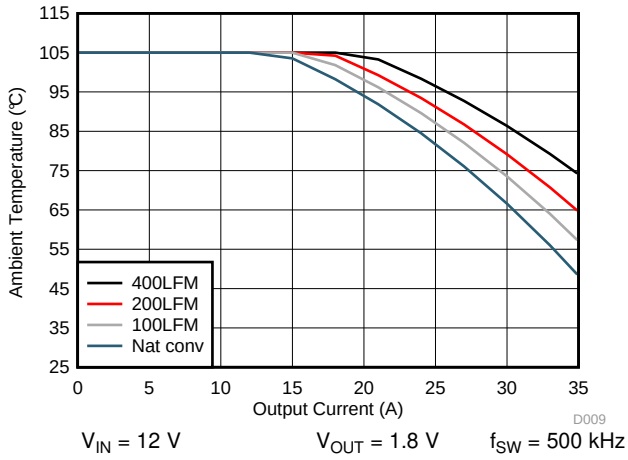



**Figure 6. Safe Operating Area**

## 6.8 Typical Characteristics ($V_{IN}$ = 5 V)

$V_{IN}$ = 5 V, $T_A$ = 25°C, $f_{SW}$ = 500 kHz (unless otherwise specified). Safe operating area curves were measured using a Texas Instruments evaluation module (EVM).

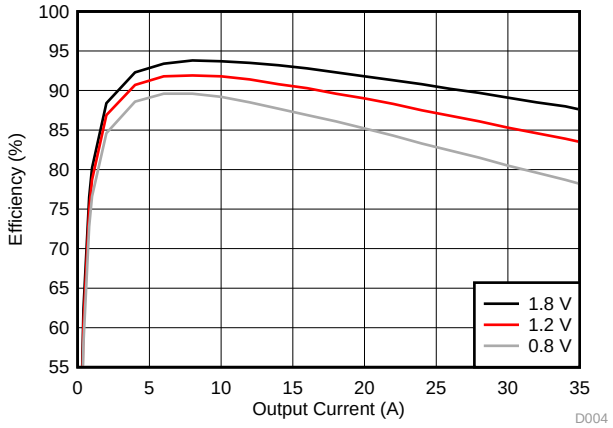



**Figure 7. Efficiency vs Output Current**

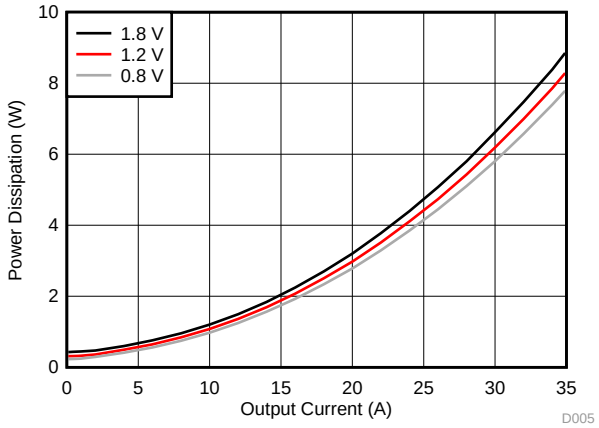



**Figure 8. Power Dissipation vs Output Current**

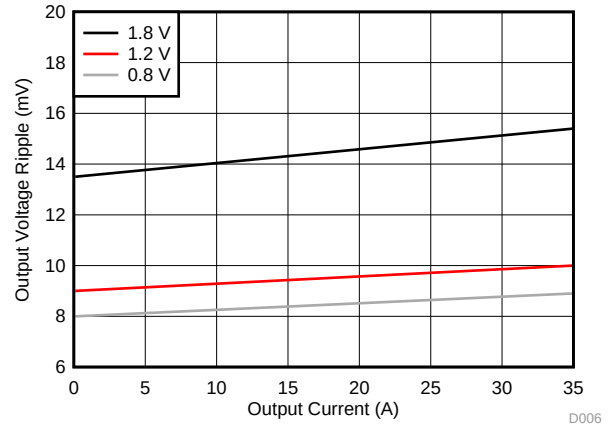



**Figure 9. Voltage Ripple vs Output Current**

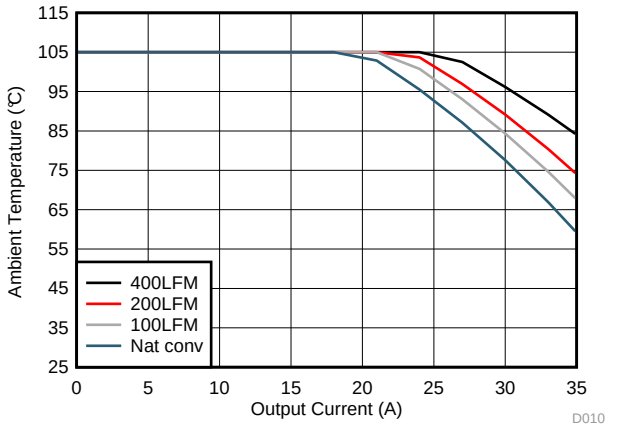



**Figure 10. Safe Operating Area**

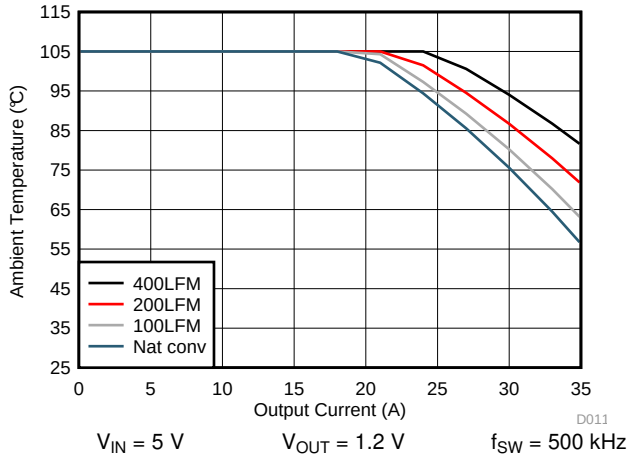



**Figure 11. Safe Operating Area**

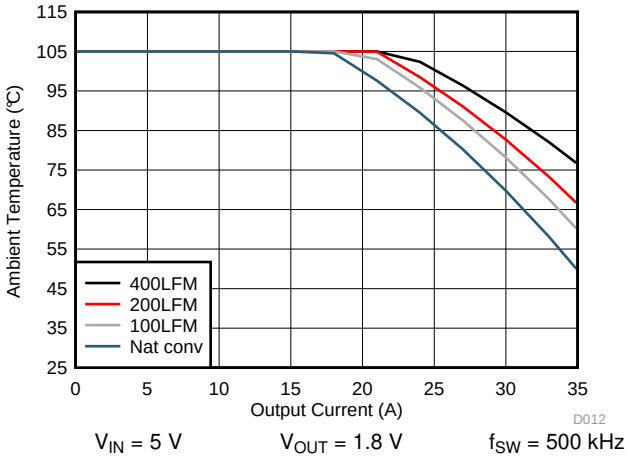


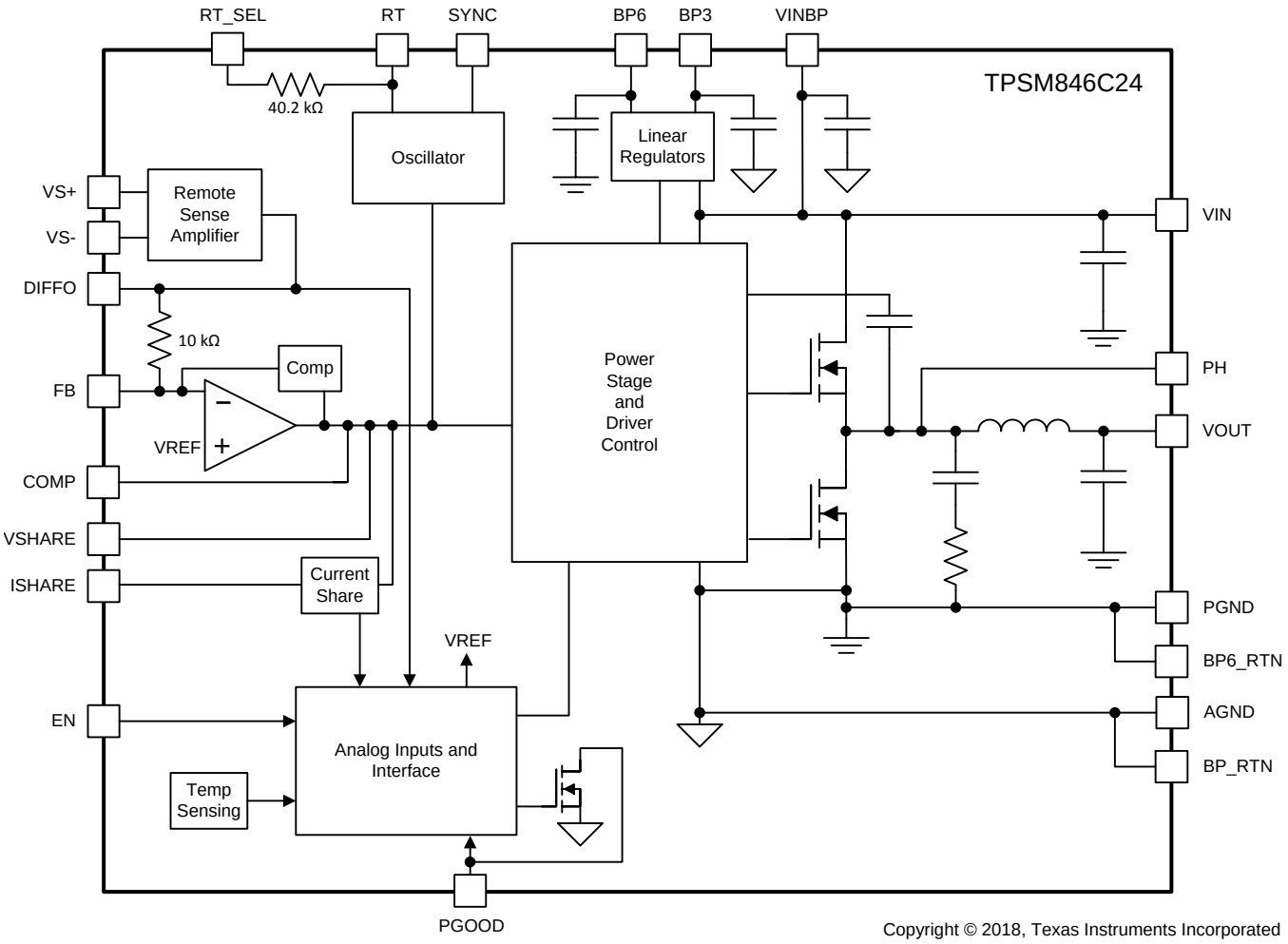

**Figure 12. Safe Operating Area**

# 7 Detailed Description

## 7.1 Overview

The TPSM846C24 device is a 35-A, high-performance, synchronous buck power module, enabling high-power density and minimal PCB area. This device implements the industry-standard fixed switching frequency, voltage-mode control with input feed-forward topology that responds instantly to input voltage change. The TSPM846C24 device can be synchronized to the external clock to eliminate beat noise and reduce EMI and EMC. Monotonic prebias capability eliminates concerns about damaging sensitive loads. Two TPSM846C24 devices can be paralleled together to provide up to 70-A load. Current sensing for overcurrent protection and current sharing between two devices are implemented by sampling a small portion of the power-stage current which provides accurate information independent of the device temperature.

## 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 Minimum Capacitance Requirements

For proper operation, the minimum required input capacitance network consists of four 22-µF (or two 47-µF) ceramic capacitors plus a 330-µF bulk capacitor. See capacitors C1 thru C5 in Figure 13. Place the ceramic capacitors as close as possible to the VIN pins. The ground return path of the capacitors must connect to PGND pins 42, 43, 54, and 59 of the TPSM846C24.

The minimum required output capacitance network consists of four 47-µF (or two 100-µF) ceramic capacitors plus two 470-µF, low-ESR polymer capacitors. See capacitors C10 thru C15 in Figure 13. The combined ESR of the polymer capacitors must not be greater than 5 mΩ. Place the ceramic capacitors as close as possible to the VOUT and PGND pins of the module. This minimum network insures good transient response and minimal ripple amplitude. The total amount of output capacitance determines the values of the frequency compensation network. For more details see the *Setting the Compensation Network* section.

Additionally, the analog power path (VINBP) requires its own bypass network consisting of a 10-nF ceramic capacitor (C8 in Figure 13) and 1-µF ceramic capacitor (C7 in Figure 13) connected directly across pins 50 and 51 of the module. For proper operation, the two internal power supply rails of the module must also be bypassed. The 6.5-V rail (BP6) requires a 4.7-µF ceramic capacitor (C6 in Figure 13) placed across pins 48 and 49 of the module with short, direct traces. The 3.3-V rail (BP3) requires a 2.2-µF ceramic capacitor (C9 in Figure 13) placed very close to pins 47 and 51.

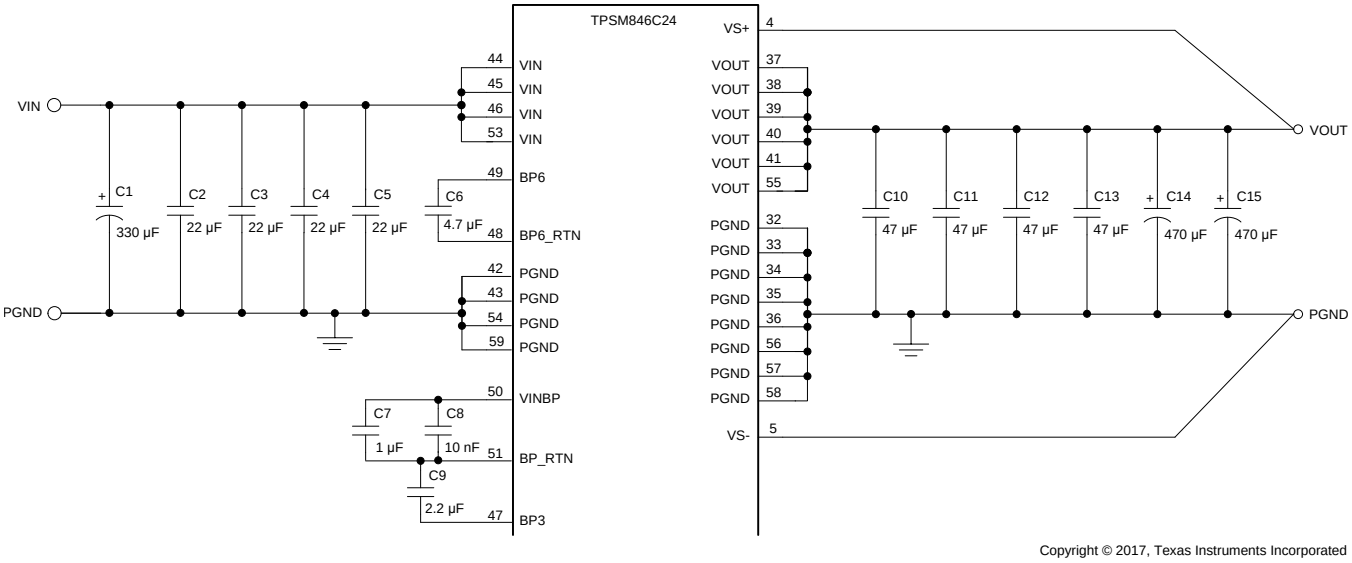





**Figure 13. Required Capacitor Schematic**

## Feature Description (continued)

### 7.3.2 Setting the Compensation Network

The TPSM846C24 requires an external series resistor and capacitor compensation network to be connected between the DIFFO pin (pin 6) and the FB pin (pin 7). These are $R_{COMP}$ and $C_{COMP}$ in Figure 14. The value of these components is determined by the total amount of output capacitance and the switching frequency. TI recommends only ceramic and low-ESR, polymer-type capacitors are. Place these components as close as possible to the module and away from noisy signal traces. Suggested values for $R_{COMP}$ and $C_{COMP}$ for some typical values of output capacitance are given in Table 1. Final values should be determined by testing system stability using standard power supply evaluation techniques.

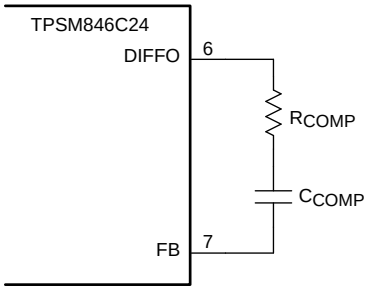




**Figure 14. Compensation Components**

**Table 1. Recommended Compensation Components**

| TOTAL $C_{OUT}$ (µF) | | SWITCHING FREQUENCY | | | | | | TYPICAL $C_{OUT}$ | |
|---|---|---|---|---|---|---|---|---|---|
| | | 300 - 400 kHz | | 400 - 600 kHz | | 600 - 1000 kHz | | | |
| MIN | MAX | $R_{COMP}$ | $C_{COMP}$ | $R_{COMP}$ | $C_{COMP}$ | $R_{COMP}$ | $C_{COMP}$ | Ceramic | Polymer |
| 1000 | 1500 | 1.0 kΩ | 1000 pF | 665 Ω | 1500 pF | 499 Ω | 2200 pF | 4 × 47 µF | 2 × 470 µF |
| 1500 | 3000 | 665 Ω | 1500 pF | 499 Ω | 2200 pF | 249 Ω | 4700 pF | 4 × 47 µF | 4 × 470 µF |
| 3000 | 5000 | 499 Ω | 2200 pF | 249 Ω | 4700 pF | 124 Ω | 6800 pF | 4 × 47 µF | 4 × 1000 µF |

### 7.3.3 Transient Response

The TPSM846C24 is designed to have an exceptional output voltage transient response to output current load steps. Table 2 shows the voltage deviation for several transient conditions.

**Table 2. Output Voltage Transient Response**

| $C_{IN}$ = 4× 22 µF Ceramic, 2x 330 µF Electrolytic | | | | | | | |
|---|---|---|---|---|---|---|---|
| $V_{OUT}$ (V) | $V_{IN}$ (V) | $f_{SW}$ (kHz) | $R_{COMP}$ | $C_{COMP}$ | $C_{OUT}$ | | VOLTAGE (1) DEVIATION (mV) |
| | | | | | CERAMIC | NON-CERAMIC (2) | |
| 0.6 | 5 | 500 | 499 Ω | 2200 pF | 4 × 47 µF | 4 × 470 µF | 33 |
| | | 500 | 249 Ω | 4700 pF | 4 × 47 µF | 4 × 1000 µF | 22 |
| | 12 | 500 | 249 Ω | 4700 pF | 4 × 47 µF | 4 × 470 µF | 24 |
| | | 750 | 124 Ω | 6800 pF | 4 × 47 µF | 4 × 1000 µF | 18 |
| 0.8 | 5 | 500 | 499 Ω | 2200 pF | 4 × 47 µF | 4 × 470 µF | 37 |
| | | 750 | 124 Ω | 6800 pF | 4 × 47 µF | 4 × 1000 µF | 19 |
| | 12 | 500 | 499 Ω | 2200 pF | 4 × 47 µF | 4 × 470 µF | 33 |
| | | 500 | 249 Ω | 4700 pF | 4 × 47 µF | 4 × 1000 µF | 20 |
| 1.0 | 5 | 500 | 665 Ω | 1500 pF | 4 × 47 µF | 2 × 470 µF | 48 |
| | | 500 | 499 Ω | 2200 pF | 4 × 47 µF | 4 × 470 µF | 38 |
| | | 500 | 249 Ω | 4700 pF | 4 × 47 µF | 4 × 1000 µF | 26 |
| | 12 | 500 | 665 Ω | 1500 pF | 4 × 47 µF | 2 × 470 µF | 41 |
| | | 500 | 499 Ω | 2200 pF | 4 × 47 µF | 4 × 470 µF | 32 |
| | | 750 | 499 Ω | 2200 pF | 4 × 47 µF | 2 × 470 µF | 26 |
| 1.2 | 5 | 500 | 665 Ω | 1500 pF | 4 × 47 µF | 2 × 470 µF | 38 |
| | | 750 | 499 Ω | 2200 pF | 4 × 47 µF | 2 × 470 µF | 34 |
| | 12 | 500 | 665 Ω | 1500 pF | 4 × 47 µF | 2 × 470 µF | 39 |
| | | 500 | 499 Ω | 2200 pF | 4 × 47 µF | 4 × 470 µF | 35 |
| 2 | 5 | 300 | 1.0 kΩ | 1000 pF | 4 × 47 µF | 2 × 470 µF | 50 |
| | | 500 | 665 Ω | 1500 pF | 4 × 47 µF | 2 × 470 µF | 38 |
| | 12 | 300 | 1.0 kΩ | 1000 pF | 4 × 47 µF | 2 × 470 µF | 57 |
| | | 500 | 665 Ω | 1500 pF | 4 × 47 µF | 2 × 470 µF | 42 |

(1) 50% load step at 2.5 A/µs.
(2) The combined equivalent ESR of all non-ceramic output capacitance must be ≤ 5 mΩ.

### 7.3.4 Setting the Output Voltage

The TPSM846C24 output voltage adjustment range is 0.5 V to 2 V. The adjustment method requires a resistor, $R_{SET}$, connected between the FB pin and AGND as shown in Figure 15. Equation 1 can be used to calculate the $R_{SET}$ value for a given output voltage, $V_{OUT}$. Additionally, the $R_{SET}$ value can be selected from Table 3.

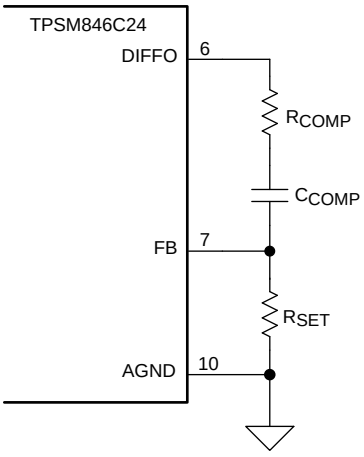





**Figure 15. RSET Resistor**

$$R_{SET} = \frac{5}{(V_{OUT} - 0.5)} \quad (k\Omega) \tag{1}$$

**Table 3. Standard $R_{SET}$ Resistor Values**

| $V_{OUT}$ (V) | $R_{SET}$ (kΩ) | $V_{OUT}$ (V) | $R_{SET}$ (kΩ) |
|---|---|---|---|
| 0.5 | open | 1.3 | 6.19 |
| 0.6 | 49.9 | 1.4 | 5.49 |
| 0.7 | 24.9 | 1.5 | 4.99 |
| 0.8 | 16.5 | 1.6 | 4.53 |
| 0.9 | 12.4 | 1.7 | 4.12 |
| 1 | 10 | 1.8 | 3.83 |
| 1.1 | 8.25 | 1.9 | 3.57 |
| 1.2 | 7.15 | 2.0 | 3.32 |

### 7.3.5 Differential Remote Sense

The TPSM846C24 device implements a differential remote-sense amplifier to provide excellent load regulation by cancelling IR-drop in high-current applications. The VS+ and VS– pins must be Kelvin-connected to the output capacitor bank directly at the load, and routed back to the device as a tightly coupled differential pair. Ensure that these traces are isolated from fast switching signals and high current paths on the final PCB layout, as these can add differential-mode noise.

### 7.3.6 Switching Frequency and Synchronization

#### *7.3.6.1 Setting the Switching Frequency*

The TPSM846C24 is set to a default switching frequency of 500 kHz. To operate the TPSM846C24 at the default switching frequency, connect the RT_SEL pin (pin 14) to AGND and leave the RT pin (pin 13) open. To change the switching frequency, leave the RT_SEL pin open, and connect a resistor from the RT pin ($R_{RT}$) to AGND. Use Equation 2 to calculate the $R_{RT}$ resistor value.

$$R_{RT} = \frac{18290 + (120 \times V_{IN})}{f_{SW}\,(kHZ)}(k\Omega) \quad (2)$$

The TPSM846C24 devices are designed to operate from 300 kHz to 1 MHz.

#### *7.3.6.2 Synchronization*

The TPSM846C24 device can synchronize to an external clock that is ±20% of the free-running frequency set by $R_{RT}$. It is required that the external clock waveform is a square wave with a duty cycle of 50%.

##### 7.3.6.2.1 Stand-Alone Device Synchronization

When power is applied, if no external clocking signal is present on the SYNC pin, the device operates at the switching frequency set by the internal or an external timing resistor. If an external clock signal that meets the specification of the Synchronization section of the *Switching Characteristics* table is applied to the SYNC pin, the device synchronizes to the leading edge of the applied waveform. The rising edge of the PH node lags the rising edge of the clocking waveform by approximately 500 ns. The external clock must be a 50% duty-cycle square wave. The external clock frequency must be with ±20% of the free-running frequency set by the $R_{RT}$ resistor. It is permissible for the SYNC signal to become active after the module has powered-up. If this is done, there is a small disturbance in the output voltage while the module locks to the SYNC clock. If the SYNC signal is lost during operation, the module quickly detects the loss and reverts to switching at the frequency set by the $R_{RT}$ resistor. A disturbance occurs in the output voltage upon loss of SYNC.

##### 7.3.6.2.2 Paralleled Devices Synchronization

When two TPSM846C24 devices are paralleled, the SYNC pins of the master and the slave must be supplied with a 50% duty cycle clock signal at the desired switching frequency. The master device locks to the rising edge of the clock; the slave locks to the falling edge. The 50% duty cycle requirement insures the modules operate 180° out of phase to minimize ripple. Both the master and slave module must have an $R_{RT}$ resistor present whose value sets a switching frequency within ±20% of the SYNC clock frequency. See the *Parallel Application* section of the datasheet for more information when paralleling devices.

### 7.3.7 Prebiased Output Start-Up

The TPSM846C24 devices prevent current from being discharged from the output during start-up when a prebiased output condition exists. If the output is prebiased, no PH pulses occur until the internal soft-start voltage rises above the error-amplifier input voltage (FB pin). As soon as the soft-start voltage exceeds the error-amplifier input, and PH pulses start. The device limits synchronous rectification after each PH pulse with a narrow on-time. The on-time of the low-side MOSFET slowly increases on a cycle-by-cycle basis until 128 pulses have been generated and the synchronous rectifier runs fully complementary to the high-side MOSFET. This approach prevents the sinking of current from a prebiased output, and ensures the output-voltage start-up and ramp-to-regulation sequences are smooth and monotonic.

If the prebias voltage is close to or exceeds the $V_{OUT}$ setpoint voltage, the mandatory 128 switching cycles, as previously described , may induce a non-monotonic dip in the output voltage. The output voltage quickly recovers to the setpoint value once the 128 cycle interval is completed.

These devices respond to a prebiased output overvoltage condition immediately upon VIN powered up and when the BP6 regulator voltage is above the BP6 UVLO of 3.73 V (typical).

### 7.3.8 Power-Good (PGOOD) Indicator

The TPSM846C24 has a built-in power-good signal (PGOOD) which indicates whether the output voltage is within its regulation range. The PGOOD pin is an open drain output that requires a pullup resistor to a voltage source of 5.5 V or less. The recommended pullup resistor value is between 10 kΩ and 100 kΩ. Once the output voltage rises above 95% of the set voltage, the PGOOD pin rises to the pullup voltage level. The PGOOD pin is pulled low when the output voltage drops lower than 88% or rises higher than 112% of the nominal set voltage.

The PGOOD signal can be connected to the EN pin of a different device to provide additional controlled turnon and turnoff sequencing.

The PGOOD signal is pulled low when the FB pin is prebiased to higher than 5% above the regulation level. This level of prebias is unusual and it is beneficial to flag a warning in this situation.

**NOTE**

The presence of a pullup voltage at the PGOOD pin before input voltage is applied, may cause the PGOOD pin to be pulled above a logic low voltage level. This is due to the limited pulldown capability in an un-powered condition. If this is not desired, increase the pullup resistance or reduce the external pullup supply voltage.

### 7.3.9 Linear Regulators BP3 and BP6

The TPSM846C24 device has two onboard linear regulators to provide suitable power for the internal circuitry of the device. Bypass the BP3 and BP6 pins externally for the converter to function properly. The BP3 pin requires a minimum of 2.2 µF of capacitance connected to BP_RTN. The BP6 pin requires a minimum 4.7 µF of capacitance connected to BP6_RTN.

The use of the internal regulators to power other circuits is not recommended because the loads placed on the regulators might adversely affect operation of the controller.

**NOTE**

Place bypass capacitors as close as possible to the device pins, with a minimum return loop back to ground and keep the return loop away from fast switching voltage and main current path. For more information, see the *Layout* section. Poor bypassing can degrade the performance of the regulator.

### 7.3.10 Parallel Application

Two TPSM846C24 devices can be paralleled for increased output current up to 70 A. Multiple connections must be made between the paralleled devices and the component selection is slightly different than for a stand-alone TPSM846C24 device. Figure 16 shows a typical schematic for two TPSM846C24 devices in parallel. Parallel operation can be evaluated using the TPSM846C24DEVM-007 evaluation board.

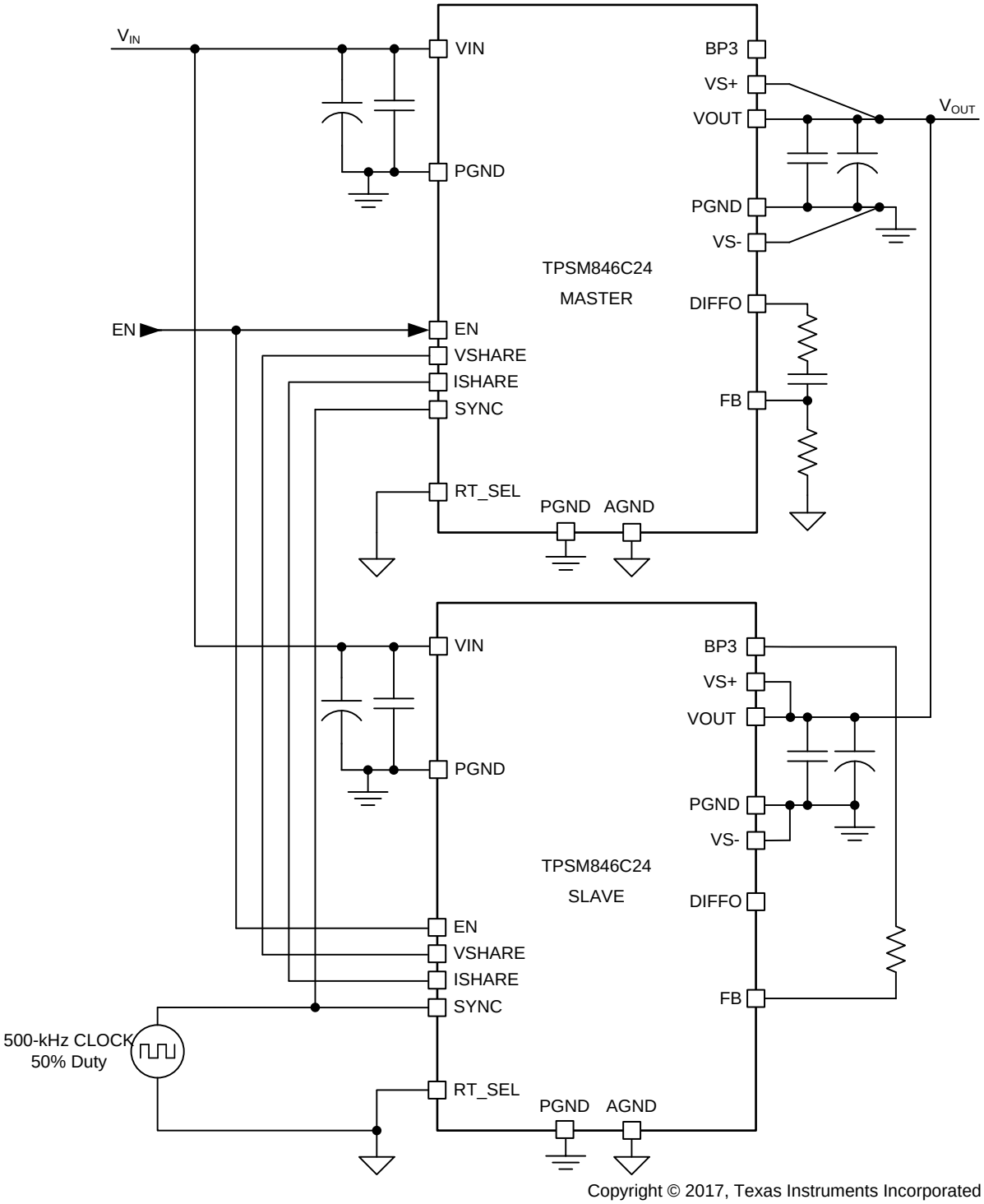



**Figure 16. TPSM846C24 Parallel**

### 7.3.11 Parallel Operation

To operate two TPSM846C24 devices in parallel, one of the devices must act as the master and the other act as a slave. To configure one of the devices as the slave device, connect a 1-kΩ resistor between the device FB pin and BP3 pin. Additionally, the SYNC, VSHARE, and ISHARE pins of both devices must be connected as shown in Figure 16. Both devices share the same VSHARE voltage. Essentially, the internal COMP voltage is shared between the two devices by connecting the VSHARE pin of each device together. By connecting the ISHARE pins of each device, the sensed current in each phase is compared, then the error current is added into the internal COMP. The resulting voltage is compared with the PWM ramp to generate the PWM pulse. This current sharing loop maintains the current balance between devices.

In addition to sharing the same internal COMP voltage, the VSHARE pin is also used for fault communication between the loop master and slave devices. The VSHARE pin voltage is pulled low if any device encounters any fault conditions so that the other device sharing VSHARE pin is alerted and stops switching accordingly.

When configured for parallel operation, the SYNC pins of the master and the slave must be supplied with a 50% duty cycle clock signal at the desired switching frequency. The master device locks to the rising edge of the clock; the slave locks to the falling edge. The 50% duty cycle requirement insures the modules operate 180° out of phase to minimize ripple. Both the master And Slave module must have an $R_{RT}$ resistor present whose value sets a switching frequency within ±20% of the SYNC clock frequency.

An optional high-frequency capacitor can be added between the VSHARE pin and ground in noisy systems, but the capacitance must not exceed 10 pF.

If operating conditions result in an on-time pulse width of ≤ 150 ns, jitter may be observed on the master and slave PH pins. The addition of a 10-kΩ resistor in series with the ISHARE connection between the devices helps to reduce, but may not eliminate, the jitter.

### 7.3.12 Overtemperature Protection

An internal temperature sensor based off the bandgap reference protects the TPSM846C24 device from thermal runaway. The internal thermal shutdown threshold, $T_{SD}$, is fixed at 145°C (typical). When the device senses a temperature above $T_{SD}$, power conversion stops until the sensed junction temperature decreases by the amount of the thermal shutdown hysteresis, $T_{HYST}$ (25°C typical). The response to an over temperature fault is to shut down and then restart.

### 7.3.13 Overcurrent Protection

Both low-side overcurrent and high-side short circuit protection are implemented. The low-side MOSFET average current is compared to the fault threshold. High-side pulses are terminated on a cycle-by-cycle basis whenever the current through the high-side MOSFET exceeds the fixed short-circuit threshold.

When either a low-side overcurrent or high-side short-circuit threshold is exceeded in a switching cycle, a counter is incremented. If no overcurrent condition is detected in a switching cycle, the counter is decremented. If the counter counts to three, an overcurrent fault condition is declared, and the output shuts down and restarts after approximately 21 ms.

### 7.3.14 Output Overvoltage and Undervoltage Protection

The TPSM846C24 device includes both output-overvoltage protection and output undervoltage protection capability by comparing the FB pin voltage to internal pre-set voltages.

If the FB pin voltage rises above the output overvoltage-protection threshold, the device terminates normal switching and turns on the low-side MOSFET to discharge the output capacitor and prevent further increases in the output voltage. The device declares an OV fault and enters continuous-restart-hiccup mode. The TPSM846C24 device responds to the output overvoltage condition immediately upon VIN powered up and BP6 regulator voltage above its own UVLO of 3.73 V (typical).

If the FB pin voltage falls below the undervoltage protection level after soft start has completed, the device terminates normal switching and forces both the high-side and low-side MOSFETs off, and begins a hiccup time-out delay prior to restart.

## 7.4 Device Functional Modes

### 7.4.1 Active Mode

The TPSM846C24 device operates in continuous conduction mode (CCM) at a fixed frequency, regardless of the output current. For the first 128 switching cycles, the low-side MOSFET on-time is slowly increased to prevent excessive current sinking in the event the device is started with a prebiased output. Following the first 128 clock cycles, the low-side MOSFET and the high-side MOSFET on-times are fully complementary.

### 7.4.2 Shutdown Mode

The TPSM846C24 uses the EN pin to enable or disable power conversion. The EN pin must be pulled high to allow power conversion.

The EN pin provides electrical ON and OFF control for the TPSM846C24. When the EN pin voltage is below the EN low threshold, the device is in shutdown mode. In shutdown mode the stand-by current is 7.7 mA typically with $V_{IN}$ = 12 V. The TPSM846C24 also employs undervoltage lockout protection. If $V_{IN}$ is below the UVLO level, the output of the regulator is turned off.

# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Typical Application

The TPSM846C24 is a highly-integrated, synchronous step-down DC-DC power module. The TPSM846C24 converts a higher DC-input voltage to a lower DC-output voltage, with a maximum output current of 35 A. Use the following design procedure to select key component values and select the appropriate features.

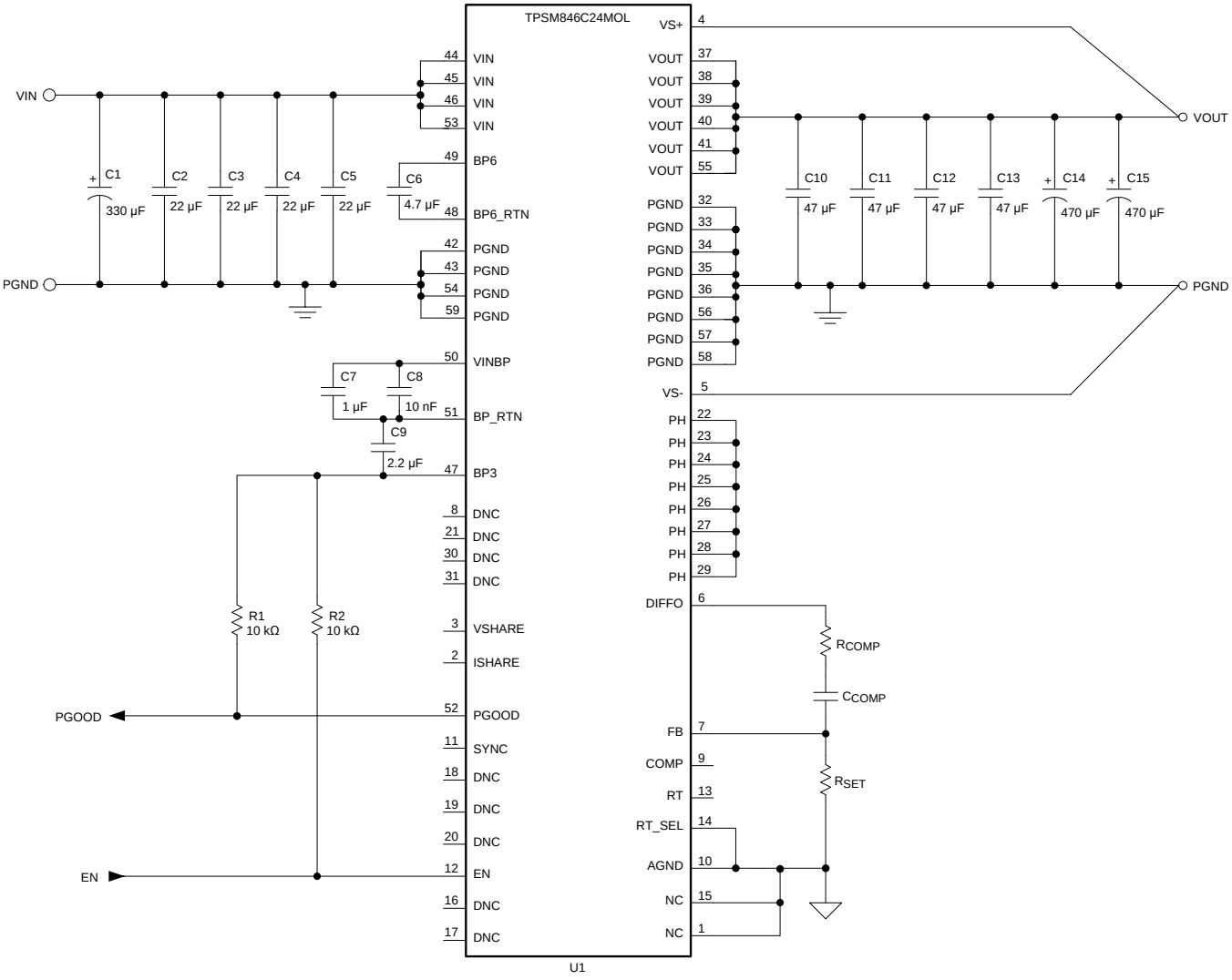





**Figure 17. Typical Application Schematic**

## Typical Application (continued)

### 8.1.1 Design Requirements

For this design example, use the parameters listed in Table 4 and follow the design procedures below.

**Table 4. Design Parameters**

| DESIGN PARAMETER | VALUE |
|---|---|
| Input voltage $V_{IN}$ | 12 V typical |
| Output voltage $V_{OUT}$ | 1.2 V |
| Output current rating | 35 A |
| Key care-abouts | Small footprint, high efficiency, PGOOD signal |

### 8.1.2 Detailed Design Procedure

#### *8.1.2.1 Custom Design With WEBENCH® Tools*

Click here to create a custom design using the TPSM846C24 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage ($V_{IN}$), output voltage ($V_{OUT}$), and output current ($I_{OUT}$) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

#### *8.1.2.2 Setting the Output Voltage*

The output voltage of the TPSM846C24 is designed to be set by the $R_{SET}$ resistor. Use Equation 3 to calculate the $R_{SET}$ resistor value.

$$R_{SET} = \frac{5}{(V_{OUT} - 0.5)} \quad (k\Omega) \tag{3}$$

To set the output voltage to 1.2 V, using Equation 3, the calculated value of $R_{SET}$ is 7.14 kΩ. The nearest E96 resistor value is 7.15 kΩ

#### *8.1.2.3 Input and Output Capacitance*

The minimum required input capacitance network consists of four 22-µF (or two 47-µF) ceramic capacitors plus a 330-µF bulk capacitor. The minimum required output capacitance network consists of four 47-µF (or two 100-µF) ceramic capacitors plus two 470-µF, low ESR polymer capacitors. The combined ESR of the polymer capacitors must not be greater than 5 mΩ. Additional input and output capacitors can be added to improve ripple or transient response.

In this design example, the minimum required input and output capacitance is used.

#### *8.1.2.4 Selecting the Compensation Components*

The TPSM846C24 requires an external series resistor and capacitor compensation network to be connected between the DIFFO pin (pin 6) and the FB pin (pin 7). The value of these components is determined by the total amount of output capacitance.

In this design example, the value of $R_{COMP}$ and $C_{COMP}$ is selected from Table 1 based on the total amount of output capacitance of 1120 µF. $R_{COMP}$ = 1 kΩ and $C_{COMP}$ = 1000 pF.

#### 8.1.2.5 Setting the Switching Frequency

The TPSM846C24 is set to a default switching frequency of 500 kHz. To operate the TPSM846C24 at the default switching frequency, connect the RT_SEL pin (pin 14) to AGND and leave the RT pin (pin 13) open.

In this design example, the switching frequency is selected to operate at the default switching frequency of 500 kHz by connecting RT_SEL pin to AGND and the $R_{RT}$ resistor is left open.

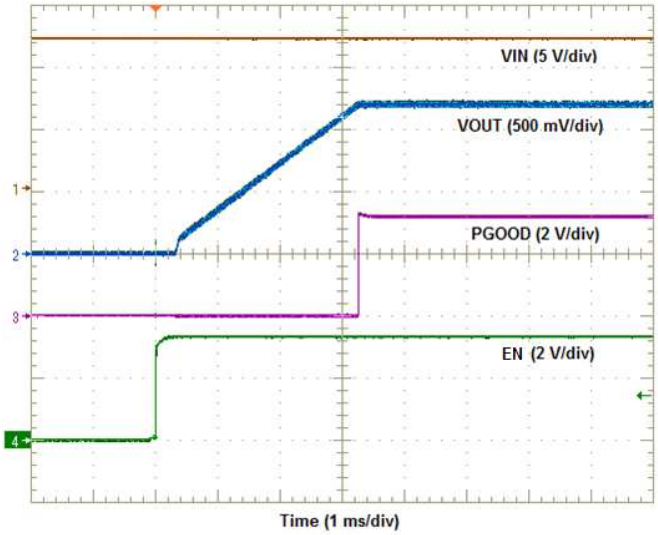
#### 8.1.2.6 Power Good (PGOOD)

Applications requiring voltage rail sequencing can benefit from the PGOOD signal present with the TPSM846C24. The PGOOD pin is an open-drain output. When the output voltage is typically between 95% and 105% of the setpoint, the PGOOD pin pulldown is released and the pin floats, requiring an external pullup resistor for a high signal. A 10-kΩ pullup resistor is placed between the PGOOD pin and the BP3 rail.

#### 8.1.2.7 ON/OFF Control (EN)

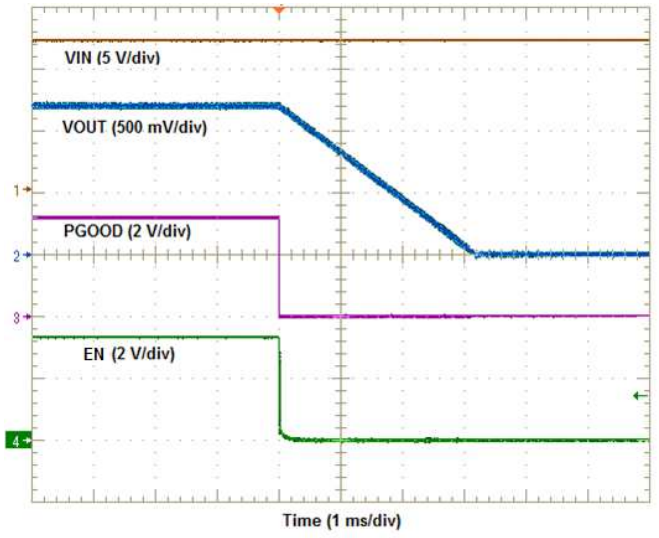
The EN signal is used to turn the power conversion function of the module ON and OFF. The EN signal is an active high signal; that is, the EN pin must be pulled high for power conversion to occur. The EN pin requires an external pullup resistor for a high signal. A 10-kΩ pullup resistor is placed between the EN pin and the BP3 rail

### 8.1.3 Application Curves




$V_{IN}$ = 12 V $V_{OUT}$ = 1.2 V $I_{OUT}$ = 10 A

**Figure 18. Start-up Waveforms**




$V_{IN}$ = 12 V $V_{OUT}$ = 1.2 V $I_{OUT}$ = 10 A

**Figure 19. Shut-down Waveform**

# 9 Power Supply Recommendations

The TPSM846C24 device is designed to operate from an input voltage supply between 4.5 V and 15 V. This supply must be well regulated. These devices are not designed for split-rail operation. Proper bypassing of input supplies and internal regulators is also critical for noise performance, as is PCB layout and grounding scheme. See the recommendations in the *Layout* section.

# 10 Layout

## 10.1 Layout Guidelines

Layout is critical for good power-supply design. Figure 20 and Figure 21 show top-side and bottom-side PCB-layout configuration for recommended component placement. Additional power, ground and signal layers are present in any PCB design. A list of PCB layout considerations using these devices is listed as follows:

- Place the input bypass capacitors as close as physically possible to the VIN and PGND pins. Additionally, a high-frequency bypass capacitor on the VIN pins can help reduce switching spikes. This capacitor can be placed on the bottom side of the PCB directly underneath the device to keep a minimum loop.
- The BP6 bypass capacitor carries a large switching current for the gate driver. Bypassing the BP6 pin to BP6_RTN with a low-impedance path is very critical to the stable operation of the TPSM846C24 device. Place the BP6 high-frequency bypass capacitor as close as possible to the device pins 48 and 49.
- The VINBP and BP3 pins also require good local bypassing. Place bypass capacitors as close as possible to the device pins and BP_RTN. Poor bypassing on the VINBP and BP3 pins can degrade the performance of the device.
- Place signal components as close as possible to the pins to which they are connected. These components include the feedback resistors and the RT resistor. Keep these components away from fast switching voltage and current paths. Terminate these components to AGND with a minimum return loop.
- Route the VS+ and VS– lines from the output capacitor bank at the load back to the device pins as a tightly coupled differential pair. These traces must be kept away from switching or noisy areas which can add differential-mode noise.
- Use caution when routing of the SYNC, VSHARE and ISHARE traces for parallel configurations. The SYNC trace carries a rail-to-rail signal and must be routed away from sensitive analog signals, including the VSHARE, ISHARE, RT, and FB signals. The VSHARE and ISHARE traces must also be kept away from fast switching voltages or currents formed by the VIN, PH, and BP6 pins.

## 10.2 Layout Example

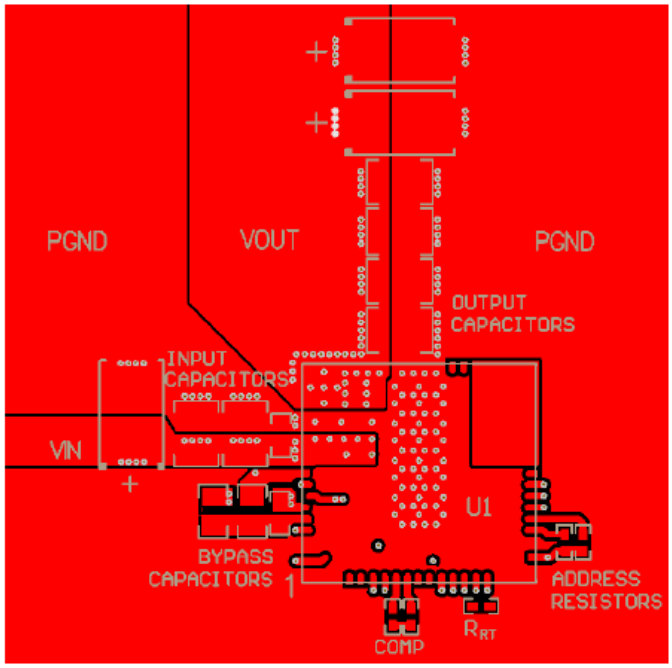



**Figure 20. PCB Top-side Layout Recommendation**

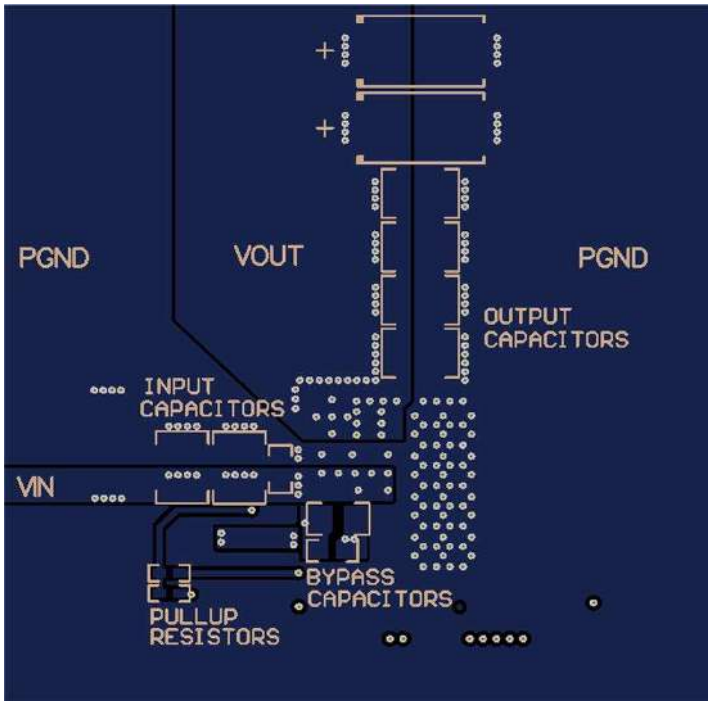



**Figure 21. PCB Bottom-side Layout Recommendation**

## 10.3 Package Specifications

| TPSM846C24 | | VALUE | UNIT |
|---|---|---|---|
| Weight | | 3.92 | grams |
| Flammability | Meets UL 94 V-O | | |
| MTBF Calculated Reliability | Per Bellcore TR-332, 50% stress, $T_A$ = 40°C, ground benign | 26.6 | MHrs |

## 10.4 EMI

The TPSM846C24 is compliant with EN55022 Class A radiated emissions. Figure 22 to Figure 25 show typical examples of radiated emissions plots for the TPSM846C24. The EMI plots were taken using an EVM with a resistive load and input power was provided using a lead acid battery. All graphs show plots of the antenna in the horizontal and vertical positions.

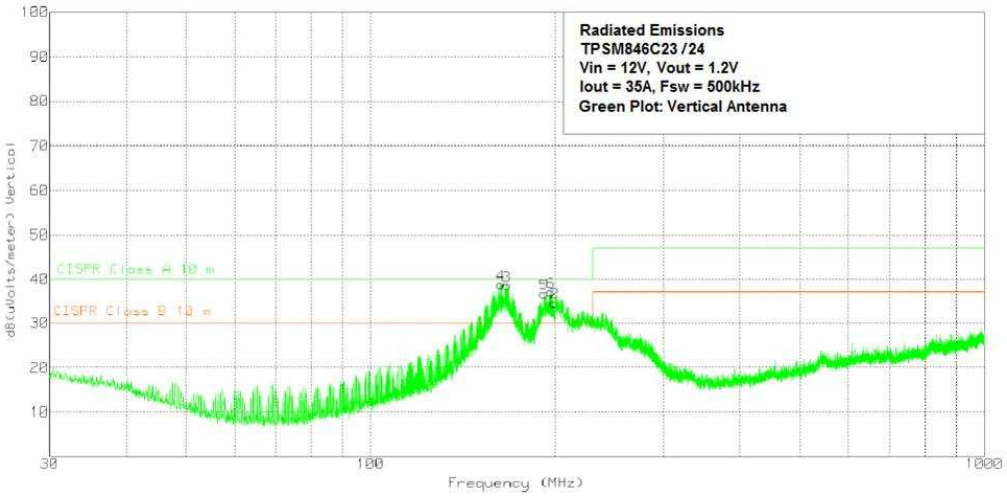



**Figure 22. Radiated Emissions 12-V Input, 1.2-V Output, 35-A Load Vertical Antenna**

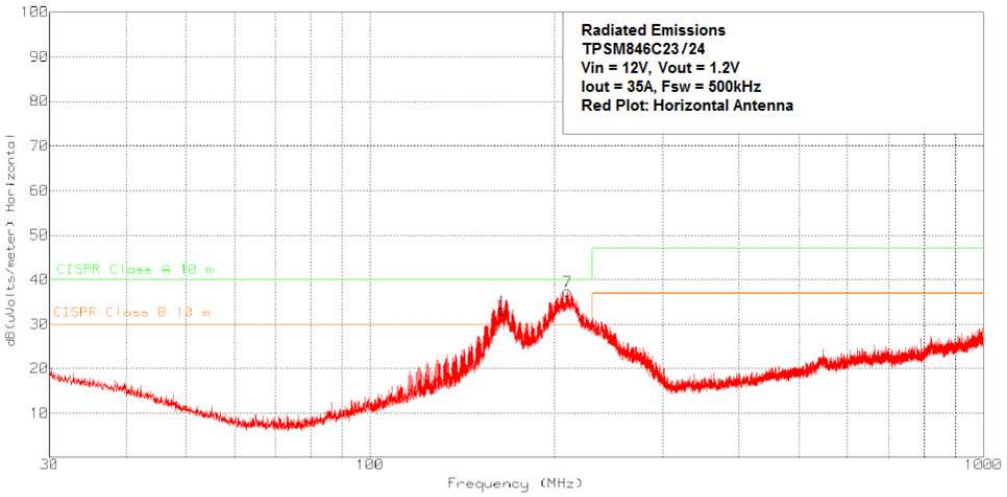



**Figure 23. Radiated Emissions 12-V Input, 1.2-V Output, 35-A Load Horizontal Antenna**

## EMI (continued)

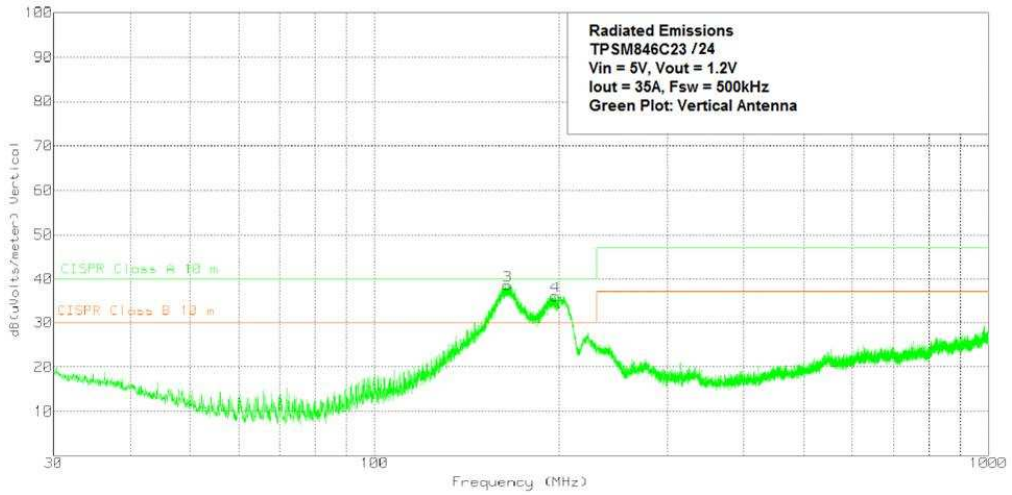



**Figure 24. Radiated Emissions 5-V Input, 1.2-V Output, 35-A Load Vertical Antenna**

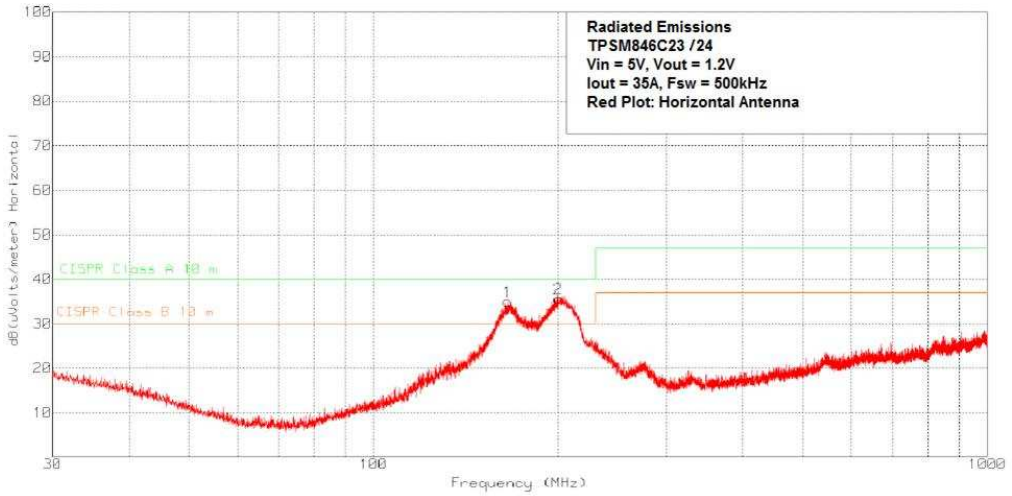



**Figure 25. Radiated Emissions 5-V Input, 1.2-V Output, 35-A Load Horizontal Antenna**

## 10.5 Mounting and Thermal Profile Recommendation

Proper mounting technique adequately covers the exposed thermal pad with solder. Excessive heat during the reflow process can affect electrical performance. Figure 26 shows the recommended reflow-oven thermal profile. Proper post-assembly cleaning is also critical to device performance. Refer to *Power Module MSL Ratings and Reflow Ratings* for more information.

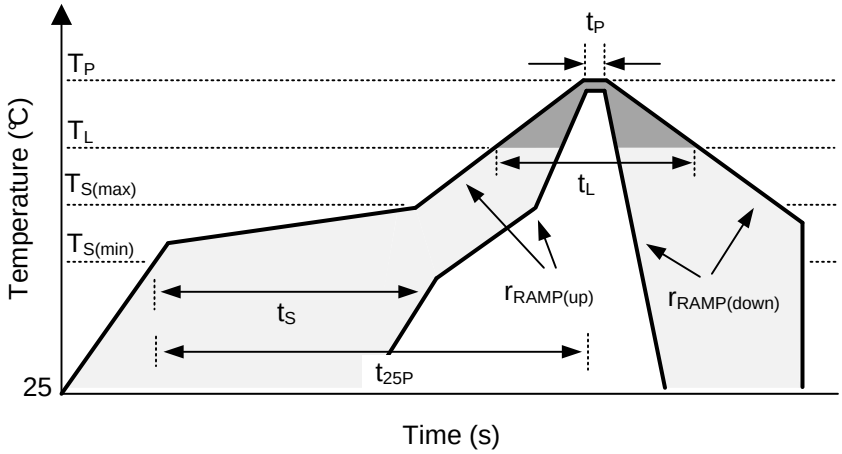



**Figure 26. Recommended Reflow-Oven Thermal Profile**

**Table 5. Recommended Thermal Profile Parameters**

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **RAMP UP AND RAMP DOWN** | | | | | |
| $r_{RAMP(up)}$ | Average ramp-up rate, $T_{S(max)}$ to $T_P$ | | | 3 | °C/s |
| $r_{RAMP(down)}$ | Average ramp-down rate, $T_P$ to $T_{S(max)}$ | | | 6 | °C/s |
| **PRE-HEAT** | | | | | |
| $T_S$ | Preheat temperature | 150 | | 200 | °C |
| $t_S$ | Preheat time, $T_{S(min)}$ to $T_{S(max)}$ | 60 | | 120 | s |
| **REFLOW** | | | | | |
| $T_L$ | Liquidous temperature | | 217 | | °C |
| $T_P$ | Peak temperature | | | 260 | °C |
| $t_L$ | Time maintained above liquidous temperature, $T_L$ | 60 | | 150 | s |
| $t_P$ | Time maintained within 5°C of peak temperature, $T_P$ | 20 | | 30 | s |
| $t_{25P}$ | Total time from 25°C to peak temperature, $T_P$ | | | 480 | s |

# 11 Device and Documentation Support

## 11.1 Device Support

### 11.1.1 Development Support

#### *11.1.1.1 Custom Design With WEBENCH® Tools*

Click here to create a custom design using the TPSM846C24 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage ($V_{IN}$), output voltage ($V_{OUT}$), and output current ($I_{OUT}$) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

## 11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 11.4 Trademarks

E2E is a trademark of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 11.6 Glossary

SLYZ022 — *TI Glossary*.

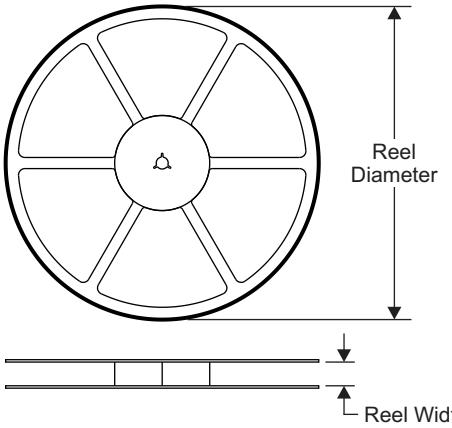
This glossary lists and explains terms, acronyms, and definitions.

# 12 Mechanical, Packaging, and Orderable Information

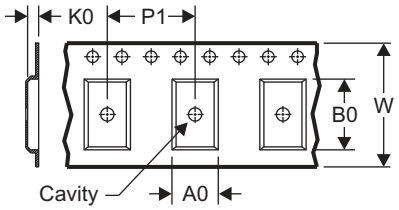
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## 12.1 Tape and Reel Information

**REEL DIMENSIONS**

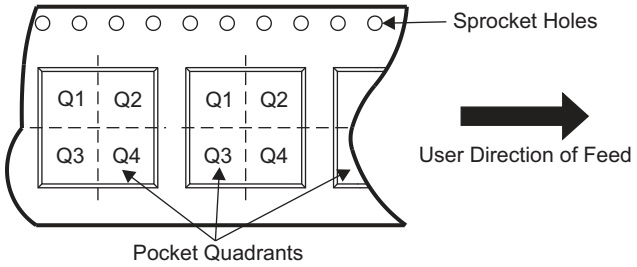



**TAPE DIMENSIONS**



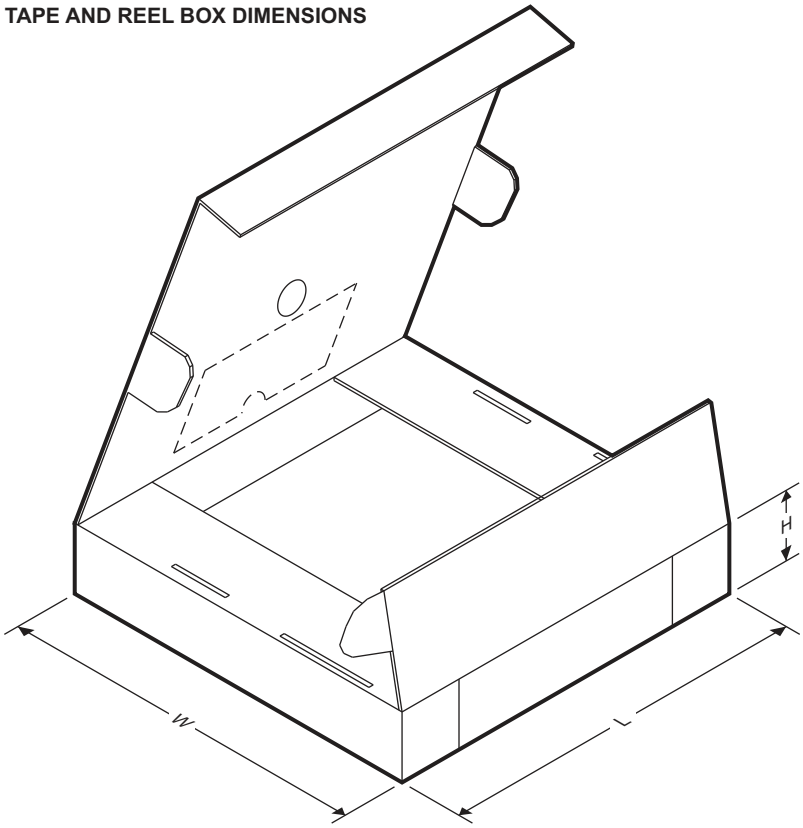

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPSM846C24MOLR | QFM | MOL | 59 | 350 | 330.0 | 32.4 | 15.35 | 16.35 | 6.1 | 24.0 | 32.0 | Q1 |

**TAPE AND REEL BOX DIMENSIONS**




| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPSM846C24MOLR | QFM | MOL | 59 | 350 | 383.0 | 353.0 | 58.0 |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPSM846C24MOLR | ACTIVE | QFM | MOL | 59 | 350 | RoHS Exempt & Green | NIAU | Level-3-260C-168 HR | -40 to 105 | TPSM846C24 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

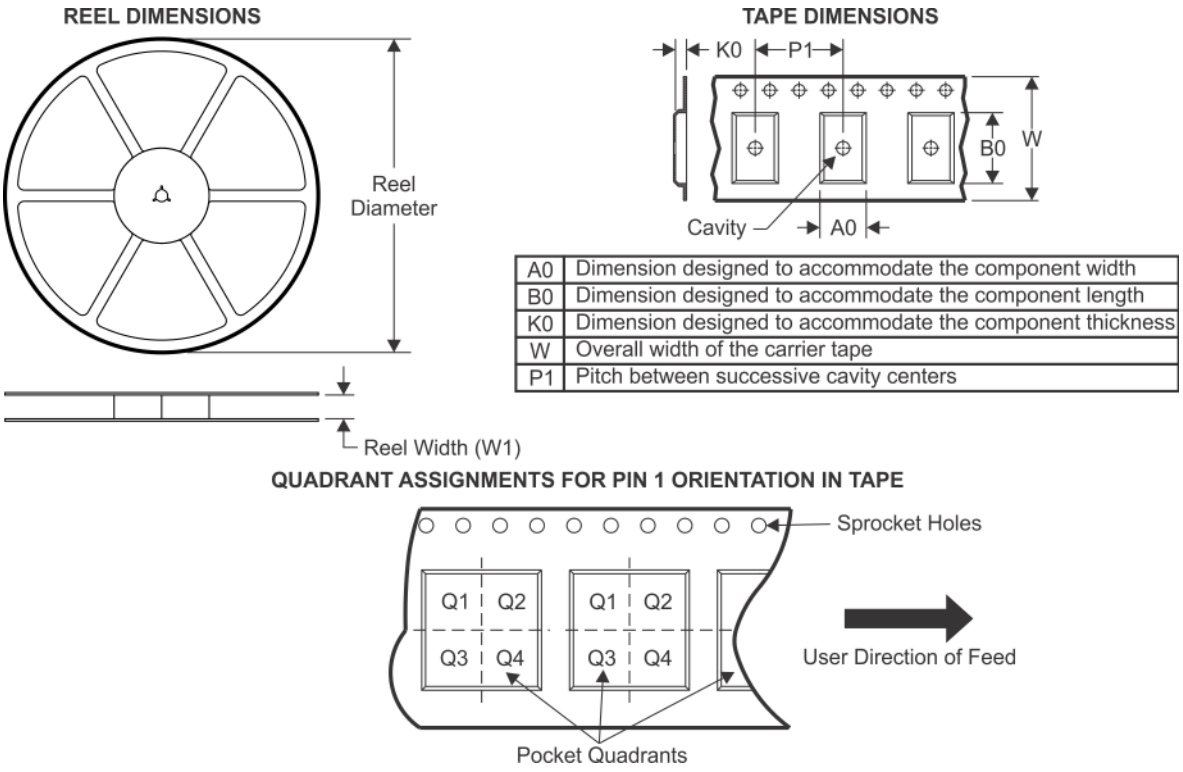
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

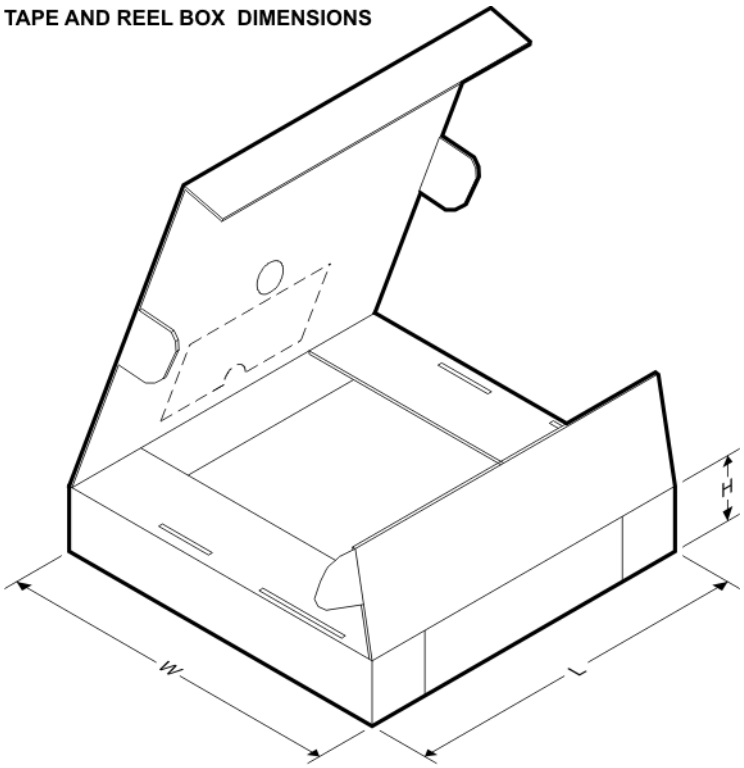



| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPSM846C24MOLR | QFM | MOL | 59 | 350 | 330.0 | 32.4 | 15.35 | 16.35 | 6.1 | 24.0 | 32.0 | Q1 |

**TAPE AND REEL BOX DIMENSIONS**




*All dimensions are nominal

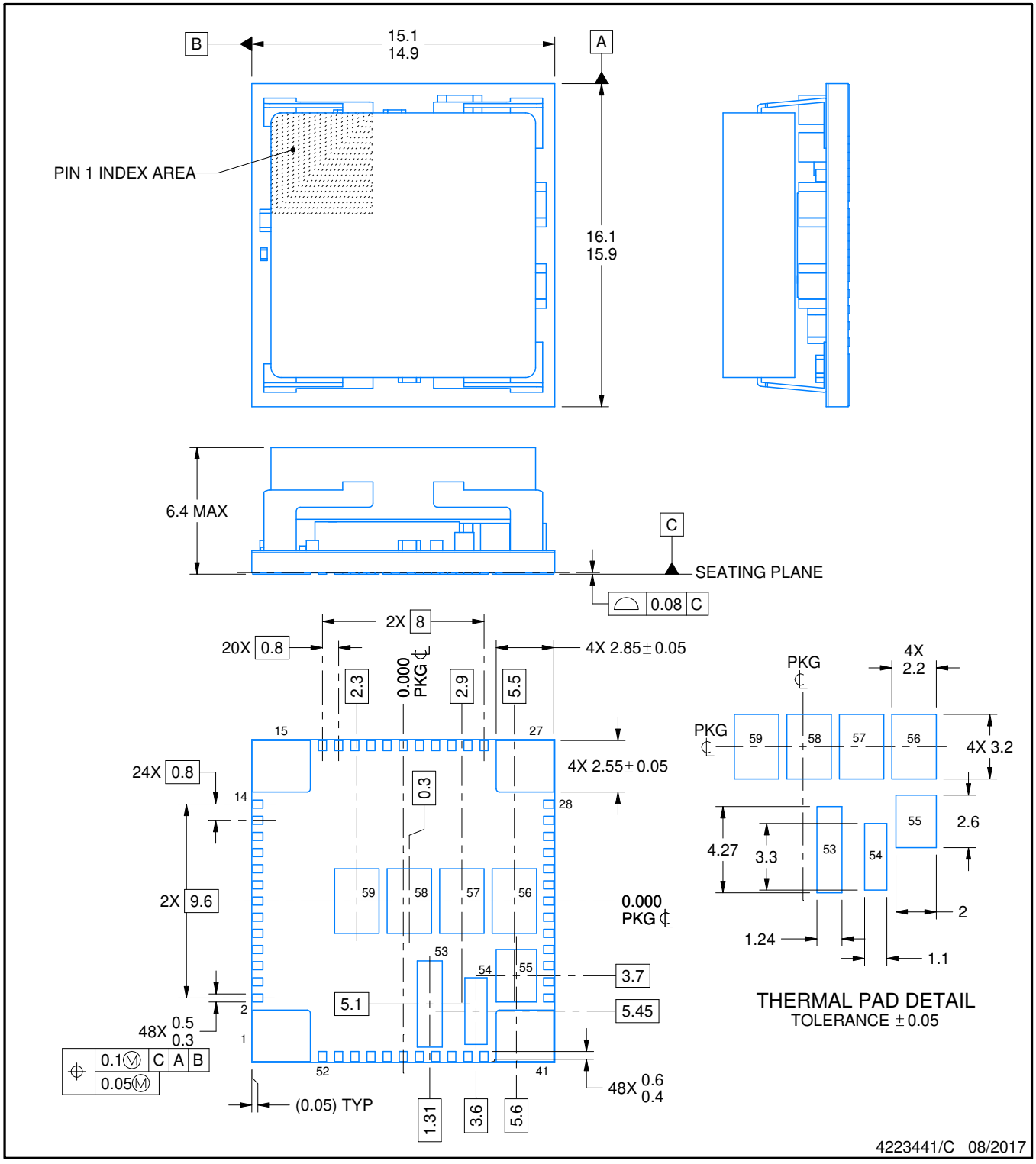
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPSM846C24MOLR | QFM | MOL | 59 | 350 | 383.0 | 353.0 | 58.0 |

# MOL0059A

# PACKAGE OUTLINE

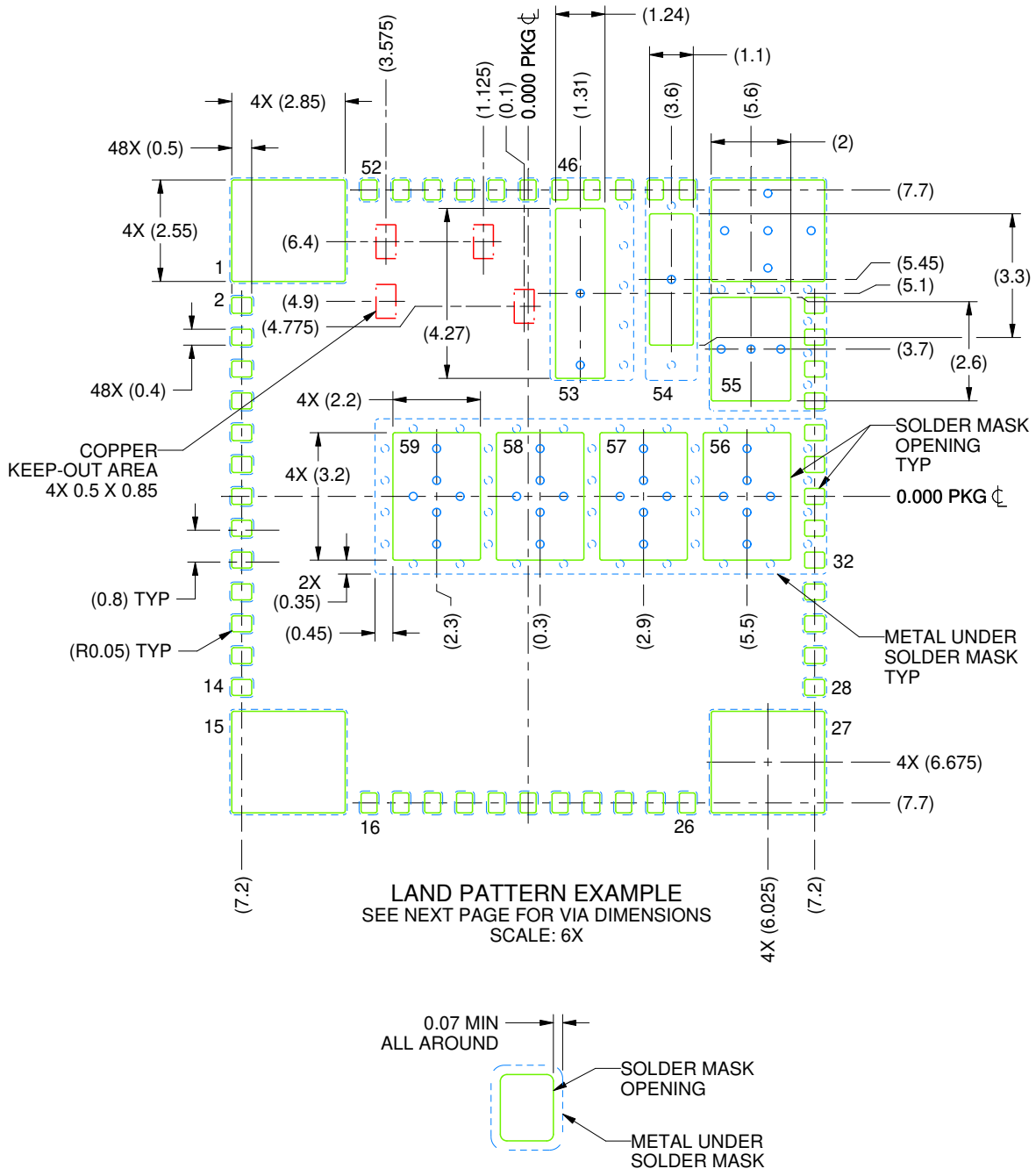
## QFM - 6.4 mm max height

PLASTIC QUAD FLAT MODULE




NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pads must be soldered to the printed circuit board for optimal thermal and mechanical performance.




LAND PATTERN EXAMPLE
SEE NEXT PAGE FOR VIA DIMENSIONS
SCALE: 6X




SOLDER MASK DETAILS
SOLDER MASK DEFINED PADS

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NOTES: (continued)

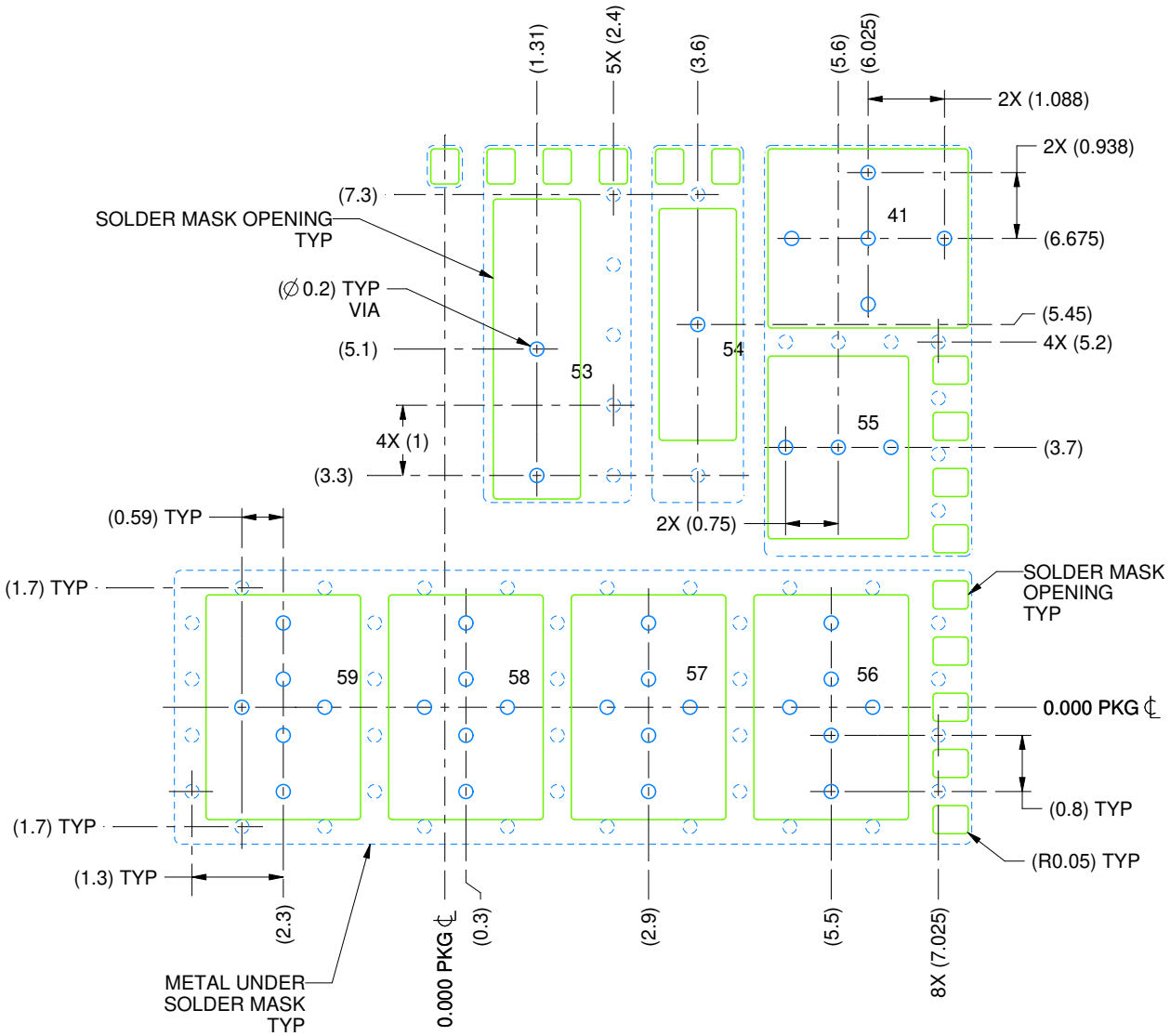
4. This package is designed to be soldered to the thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE BOARD LAYOUT

## MOL0059A

## QFM - 6.4 mm max height

PLASTIC QUAD FLAT MODULE




LAND PATTERN EXAMPLE
VIA DETAIL
SCALE: 10X

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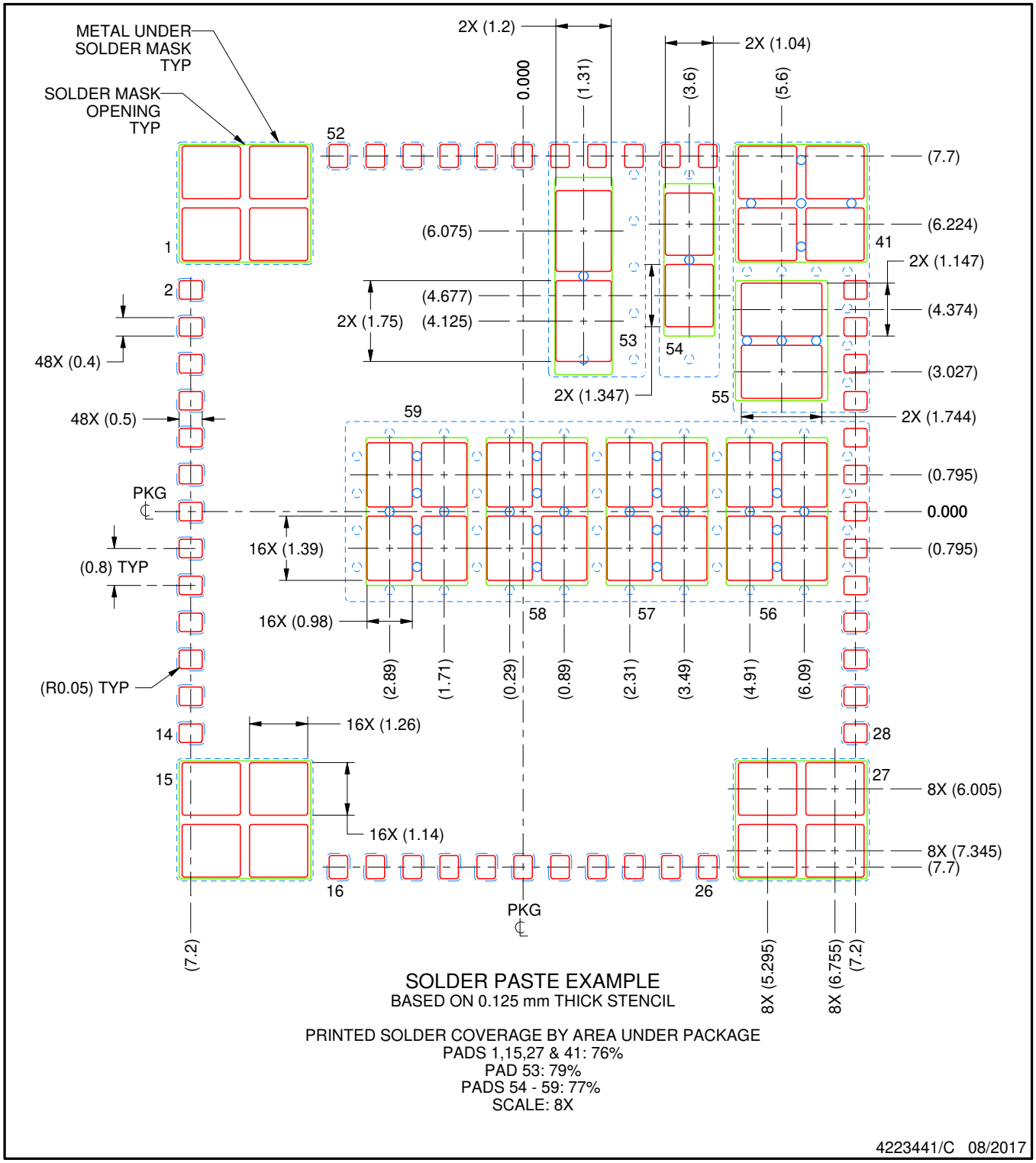
# EXAMPLE STENCIL DESIGN

## MOL0059A

### QFM - 6.4 mm max height

PLASTIC QUAD FLAT MODULE




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 1,15,27 & 41: 76%
PAD 53: 79%
PADS 54 - 59: 77%
SCALE: 8X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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