

April 1984 Revised March 2000

DM74AS74

Dual D-Type Positive-Edge-Triggered Flip-Flop with Preset and Clear

General Description

The AS74 is a dual edge-triggered flip-flops. Each flip-flop has individual D, clock, clear and preset inputs, and also complementary Q and \overline{Q} outputs.

Information at input D is transferred to the Q output on the positive going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. When the clock input is at either the HIGH or LOW level, the D input signal has no effect.

Asynchronous preset and clear inputs will set or clear Q output respectively upon the application of LOW level sig-

Features

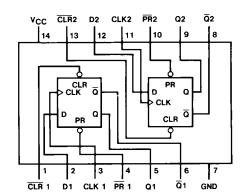
- Switching specifications at 50 pF
- \blacksquare Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin-for-pin compatible with Schottky and LS TTL counterpart
- Improved AC performance over S74 at approximately half the power

Ordering Code:

Order Number	Package Number	Package Description
DM74AS74M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM74AS74SJX	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74AS74N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



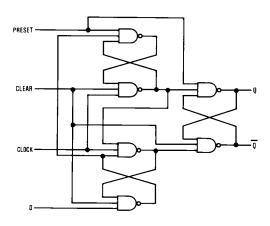
Function Table

Inputs				Outputs			
PR	CLR	CLK	D	Q	Q		
L	Н	Χ	Χ	Н	L		
Н	L	Χ	Χ	L	Н		
L	L	Χ	Χ	H (Note 1)	H (Note 1)		
Н	Н	\uparrow	Н	Н	L		
Н	Н	\uparrow	L	L	Н		
Н	Н	L	Χ	Q_0	\overline{Q}_0		

- L = LOW State
- H = HIGH State
- X = Don't Care
- Positive Edge Transition
 Provious Condition of Condition
- $Q_0 = Previous Condition of Q$

Note 1: This condition is nonstable; it will not persist when preset and clear inputs return to their inactive (HIGH) level. The output levels in this condition are not guaranteed to meet the V_{OH} specification.

Logic Diagram



Absolute Maximum Ratings(Note 2)

Supply Voltage 7V
Input Voltage 7V

Operating Free Air Temperature Range 0°C to +70°C Storage Temperature Range -65°C to +150°C

Typical θ_{JA}

 N Package
 76.0°C/W

 M Package
 107.0°C/W

Note 2: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V _{CC}	Supply Voltage		4.5	5	5.5	V
V _{IH}	HIGH Level Input Voltage		2			V
V _{IL}	LOW Level Input Voltage	LOW Level Input Voltage			0.8	V
I _{OH}	HIGH Level Output Current				-2	mA
I _{OL}	LOW Level Output Current				20	mA
f _{CLK}	Clock Frequency		0		105	MHz
t _{W(CLK)}	Width of Clock Pulse	HIGH	4			ns
		LOW	5.5			ns
t _W	Pulse Width Preset & Clear LOW		4			ns
t _{SU}	Data Setup Time (Note 3)		4.5↑			ns
t _{SU}	PRE or CLR Setup-Time (Note 3)		2↑			ns
t _H	Data Hold Time (Note 3)		0↑			ns
T _A	Free Air Operating Temperature		0		70	°C

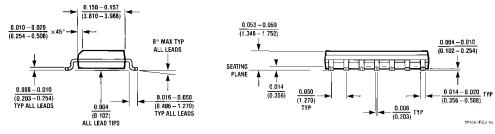
Note 3: The (1) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics

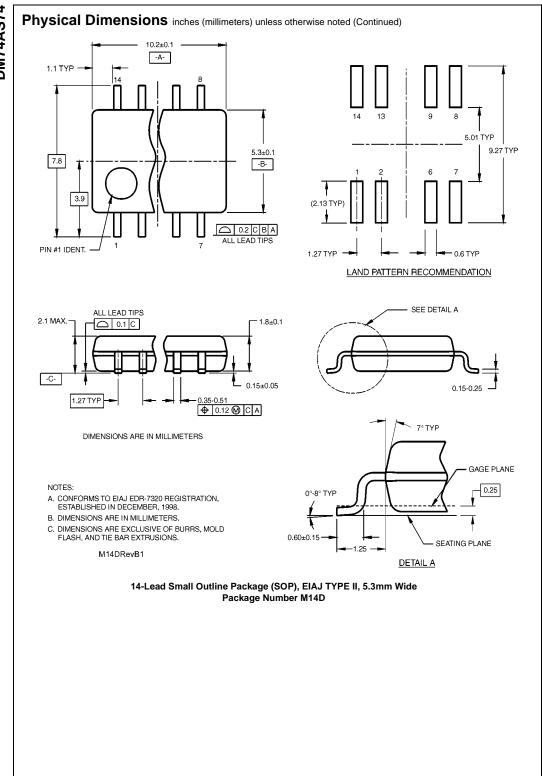
over recommended operating free air temperature range. All typical values are measured at $V_{CC} = 5V$, $T_A = 25^{\circ}C$.

Symbol	Parameter	Conditions		Min	Тур	Max	Units
V _{IK}	Input Clamp Voltage	$V_{CC} = 4.5V, I_I = -18 \text{ mA}$				-1.2	V
V _{OH}	HIGH Level	V _{CC} = 4.5V to 5.5V,	V _{CC} - 2				
	Output Voltage	$I_{OH} = -2 \text{ mA}$				V	
V _{OL}	LOW Level	$V_{CC} = 4.5V$, $V_{IH} = Max$,		0.35	0.5	V	
	Output Voltage	I _{OL} = 20 mA		0.33	0.5	V	
I	Input Current @ Max Input Voltage	$V_{CC} = 5.5V, V_{IH} = 7V$				0.1	mA
I _{IH}	HIGH Level Input Current	V _{CC} = 5.5V,	Clock, D			20	μΑ
		$V_{IH} = 2.7V$	Preset, Clear			40	μΑ
I _{IL}	LOW Level Input Current	$V_{CC} = 5.5V$,	Clock, D			-0.5	mA
		$V_{IL} = 0.4V$	Preset, Clear			-1.8	mA
Io	Output Drive Current	$V_{CC} = 5.5V, V_{O} = 2.25V$	•	-30		-112	mA
I _{CC}	Supply Current	V _{CC} = 5.5V			10.5	16	mA

Switching Characteristics over recommended operating free air temperature range Symbol Conditions Units Parameter From То Min Max $V_{CC} = 4.5V \text{ to } 5.5V$ Maximum Clock Frequency 105 MHz t_{PLH} Propagation Delay Time $R_L=500\Omega$ Preset Q or 7.5 3 LOW-to-HIGH Level Output or Clear $C_L = 50 pF$ Q Propagation Delay Time Preset Q or t_{PHL} 10.5 3.5 ns HIGH-to-LOW Level Output or Clear Q Propagation Delay Time Clock Q or t_{PLH} 3.5 8 ns LOW-to-HIGH Level Output Q Propagation Delay Time Clock Q or t_{PHL} 4.5 9 ns HIGH-to-LOW Level Output Q



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow Package Number M14A



Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 0.740 - 0.770(18.80 - 19.56)0.090 (2.286) 14 13 12 11 10 9 8 14 13 12 0.250 ± 0.010 PIN NO. 1 IDENT PIN NO. 1 IDENT 1 2 3 4 5 6 7 1 2 3 $\frac{0.092}{(2.337)}$ DIA 0.030 MAX (0.762) DEPTH OPTION 1 OPTION 02 $\frac{0.135 \pm 0.005}{(3.429 \pm 0.127)}$ 0.300 - 0.320 $\overline{(7.620 - 8.128)}$ 0.065 $\frac{0.145 - 0.200}{(3.683 - 5.080)}$ 0.060 4° TYP Optional (1.524) (1.651) $\frac{0.008 - 0.016}{(0.203 - 0.406)}$ TYP 0.020 (0.508) 0.125 - 0.150 0.075 ± 0.015 $\overline{(3.175 - 3.810)}$ 0.280 (1.905 ± 0.381) (7.112) MIN 0.014 - 0.023 $\frac{0.100 \pm 0.010}{(2.540 \pm 0.254)} \text{ TYP}$ TYP (0.356 - 0.584) $\frac{0.050\pm0.010}{(1.270-0.254)}$ TYP 0.325 ^{+0.040} -0.015 $8.255 + 1.016 \\ -0.381$ N144 (REV.E)

14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N14A

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