Automotive High Performance Logic Gates

NLV18SZxx, NLV28WZxx

The NLV18SZxx are automotive−grade High Performance single CMOS logic gates. The NLV28WZxx are automotive−grade high Performance Dual CMOS logic gates.

Features

- High Speed: t_{PD} = 3.7 ns (Typ) at V_{CC} = 3.0 V
- Low Power Dissipation: I_{CC} = 1 μA (Max) at T_A = 25°C
- High Noise Immunity
- Balanced Propagation Delays ($t_{PLH} = t_{PHL}$)
- Symmetrical Output Impedance ($I_{OH} = I_{OL}$ = 24 mA @ V_{CC} = 3.0 V)
- Operating Temperature: −55°C to +125°C
  AEC Grade 1−Compliant: −40°C to +125°C
- Tiny SC−88A and SC−88 Packages (other package offerings may be available upon request)
- AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and RoHS Compliant

FUNCTION LIST

xx	Function
00	2−Input NAND
02	2−Input NOR
04	Inverter
06	Open−Drain Inverter
07	Open−Drain Buffer
08	2−Input AND
14	Schmitt−Trigger Inverter
17	Schmitt−Trigger Buffer
32	2−Input OR
16	Buffer
86	2−Input XOR
125	Tri−State Buffer
126	Tri−State Buffer
U04	Unbuffered Inverter

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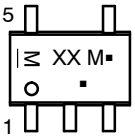
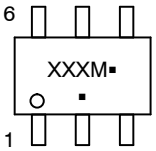
SC−88A
DF SUFFIX
CASE 419A



MARKING DIAGRAM

SC−88
CASE 419B



XX = Device Code
M = Date Code*
▪ = Pb−Free Package

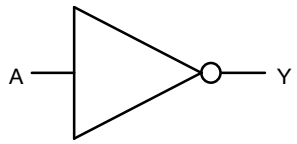
(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

ORDERING INFORMATION

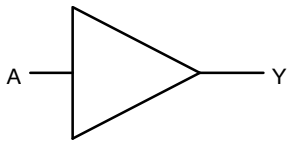
See detailed ordering and shipping information on page 9 of this data sheet.

Functions and Function Tables – Buffers and Inverters



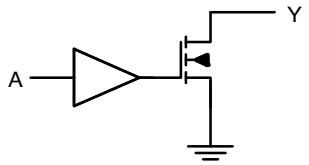
04 – Inverter
U04 – Unbuffered Inverter

A	Y
0	1
1	0



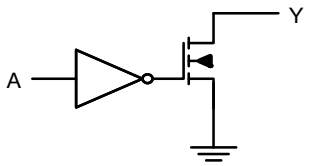
16 – Buffer

A	Y
0	0
1	1



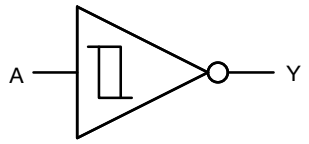
06 – Open–Drain Inverter

A	Y
0	Hi–Z
1	0



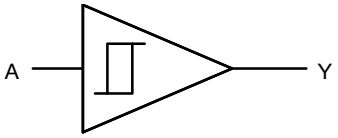
07 – Open–Drain Buffer

A	Y
0	0
1	Hi–Z



14 – Schmitt–Trigger Inverter

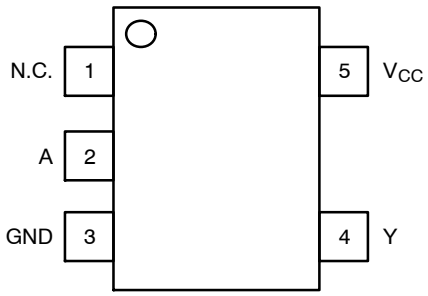
A	Y
0	1
1	0



17 – Schmitt–Trigger Buffer

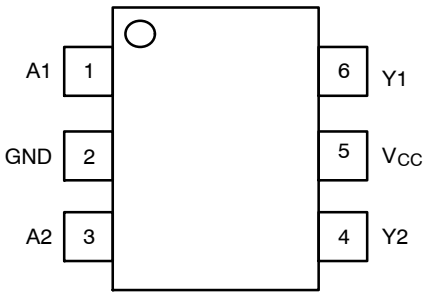
A	Y
0	0
1	1

Pin Assignment



Pinout (Buffers and Inverters)

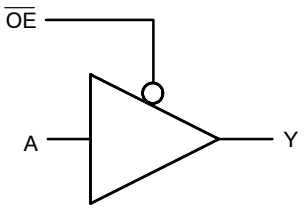
Pin	Name	Description
1	N.C.	No Connection
2	A	Input
3	GND	Ground
4	Y	Output
5	V_{CC}	Supply



Pinout (Buffers and Inverters)

Pin	Name	Description
1	A1	Input 1
2	GND	Ground
3	A2	Input 2
4	Y	Output 2
5	V_{CC}	Supply
6	Y1	Output 1

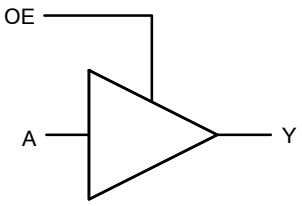
Functions and Function Tables – Tri−State Buffers and Bus Drivers



125 − Tri−State Buffer

$\overline{OE}$	A	Y
0	0	0
0	1	1
1	X	Hi−Z

X = Don't Care

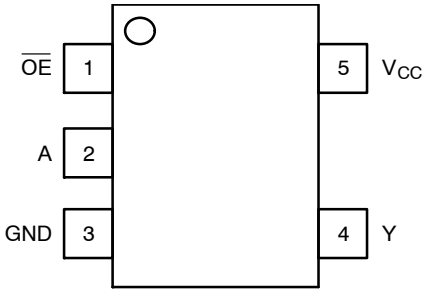


126 − Tri−State Buffer

OE	A	Y
0	X	Hi−Z
1	0	0
1	1	1

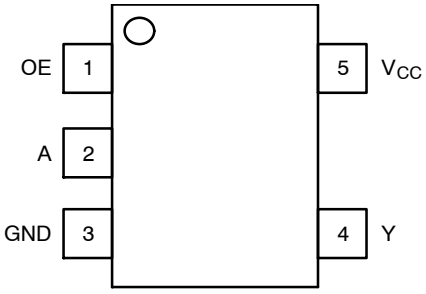
X = Don't Care

Pin Assignments



Pinout (125)

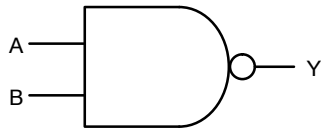
Pin	Name	Description
1	$\overline{OE}$	Enable (Active−Low)
2	A	Input
3	GND	Ground
4	Y	Output
5	V_{CC}	Supply



Pinout (126)

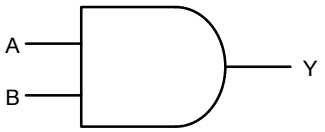
Pin	Name	Description
1	OE	Enable (Active−High)
2	A	Input
3	GND	Ground
4	Y	Output
5	V_{CC}	Supply

Functions and Function Tables – Gates



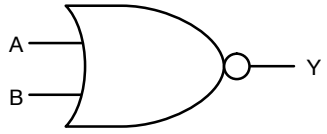
00 – NAND

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0



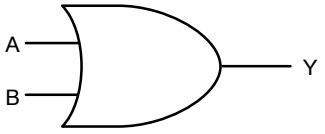
08 – AND

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1



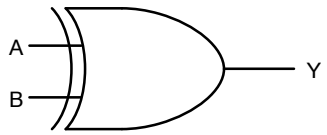
02 – NOR

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0



32 – OR

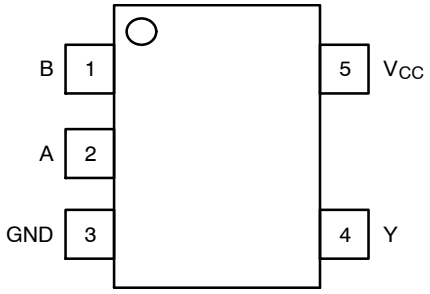
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1



86 – XOR

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Pin Assignment



Pinout (Gates)

Pin	Name	Description
1	B	Input
2	A	Input
3	GND	Ground
4	Y	Output
5	V_{CC}	Supply

Table 1. MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +6.5	V
V_{IN}	DC Input Voltage		−0.5 to +6.5	V
V_{OUT}	DC Output Voltage (U04)		−0.5 to V_{CC}+0.5	V
	DC Output Voltage (Other functions)	Active−Mode (High or Low State) Tri−State Mode (Note 1) Power−Down Mode (V_{CC} = 0 V)	−0.5 to V_{CC}+0.5 −0.5 to +6.5 −0.5 to +6.5	
I_{IK}	DC Input Diode Current		−50	mA
I_{OK}	DC Output Diode Current		−50	mA
I_{OUT}	DC Output Source/Sink Current		±50	mA
I_{CC} or I_{GND}	DC Supply Current Per Supply Pin or Ground Pin		±100	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature Under Bias		+150	°C
θ_{JA}	Thermal Resistance (Note 2)		659	°C/W
P_D	Power Dissipation in Still Air at 85°C		190	mW
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage (Note 3)	Human Body Model Charged Device Model	2000 1000	V
$I_{LATCHUP}$	Latchup Performance (Note 4)		±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Applicable to devices with outputs that may be tri−stated.
2. Measured with minimum pad spacing on an FR4 board, using 10 mm−by−1 inch, 20 ounce copper trace with no air flow.
3. HBM tested to EIA / JESD22−A114−A. CDM tested to JESD22−C101−A. JEDEC recommends that ESD qualification to EIA/JESD22−A115A (Machine Model) be discontinued.
4. Tested to EIA/JESD78 Class II.

Table 2. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Positive DC Supply Voltage		1.65	5.5	V
V_{IN}	Digital Input Voltage		0	5.5	V
V_{OUT}	DC Output Voltage (U04)		0	V_{CC}	V
	DC Output Voltage (Other functions)	Active−Mode (High or Low State) Tri−State Mode (Note 1) Power−Down Mode (V_{CC} = 0 V)	0 0 0	V_{CC} 5.5 5.5	
T_A	Operating Free−Air Temperature		−55	+125	°C
t_r, t_f	Input Transition Rise or Fall Rate				ns/V
	Functions 14 and 17		0	No Limit	
	All Other Functions	V_{CC} = 1.65 V to 1.95 V	0	20	
		V_{CC} = 2.3 V to 2.7 V	0	20	
		V_{CC} = 3.0 V to 3.6 V	0	10	
		V_{CC} = 4.5 V to 5.5 V	0	5	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 3. DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V_{CC} (V)	T_A = 25°C			−55°C ≤ T_A ≤ 125°C		Units
				Min	Typ	Max	Min	Max	
V_T+	Positive Input Threshold Voltage		1.65	–	1.0	1.4	–	1.4	V
			2.3	–	1.5	1.8	–	1.8	
			2.7	–	1.7	2.0	–	2.0	
			3.0	–	1.9	2.2	–	2.2	
			4.5	–	2.7	3.1	–	3.1	
			5.5	–	3.3	3.6	–	3.6	
V_T-	Negative Input Threshold Voltage		1.65	0.2	0.5	–	0.2	–	V
			2.3	0.4	0.75	–	0.4	–	
			2.7	0.5	0.87	–	0.5	–	
			3.0	0.6	1.0	–	0.6	–	
			4.5	1.0	1.5	–	1.0	–	
			5.5	1.2	1.9	–	1.2	–	
V_H	Input Hysteresis Voltage		1.65	0.1	0.48	0.9	0.1	0.9	V
			2.3	0.25	0.75	1.1	025	1.1	
			2.7	0.3	0.83	1.15	0.3	1.15	
			3.0	0.4	0.93	1.2	0.4	1.2	
			4.5	0.6	1.2	1.5	0.6	1.5	
			5.5	0.7	1.4	1.7	0.7	1.7	
NLV18SZU04 (Under Development)									
V_{IH}	High−Level Input Voltage		1.65 to 1.95	0.85 V_{CC}	–	–	0.85 V_{CC}	–	V
			2.3 to 5.5	0.80 V_{CC}	–	–	0.80 V_{CC}	–	
V_{IL}	Low−Level Input Voltage		1.65 to 1.95	–	–	0.15 V_{CC}	–	0.15 V_{CC}	V
			2.3 to 5.5	–	–	0.20 V_{CC}	–	0.20 V_{CC}	
ALL OTHER PARTS									
V_{IH}	High−Level Input Voltage		1.65 to 1.95	0.65 V_{CC}	–	–	0.65 V_{CC}	–	V
			2.3 to 5.5	0.70 V_{CC}	–	–	0.70 V_{CC}	–	
V_{IL}	Low−Level Input Voltage		1.65 to 1.95	–	–	0.35 V_{CC}	–	0.35 V_{CC}	V
			2.3 to 5.5	–	–	0.30 V_{CC}	–	0.30 V_{CC}	
ALL PARTS									
V_{OH}	High−Level Output Voltage	V_{IN} = V_{IH} or V_{IL}							V
		I_{OH} = −100 μA	1.65 to 5.5	V_{CC} − 0.1	V_{CC}	–	V_{CC} − 0.1	–	
		I_{OH} = −4 mA	1.65	1.29	1.4	–	1.29	–	
		I_{OH} = −8 mA	2.3	1.9	2.1	–	1.9	–	
		I_{OH} = −12 mA	2.7	2.2	2.4	–	2.2	–	
		I_{OH} = −16 mA	3.0	2.4	2.7	–	2.4	–	
		I_{OH} = −24 mA	3.0	2.3	2.5	–	2.3	–	
		I_{OH} = −32 mA	4.5	3.8	4.0	–	3.8	–	
V_{OL}	Low−Level Output Voltage	V_{IN} = V_{IH} or V_{IL}							V
		I_{OL} = 100 μA	1.65 to 5.5	–		0.1	–	0.1	
		I_{OL} = 4 mA	1.65	–	0.08	0.24	–	0.24	
		I_{OL} = 8 mA	2.3	–	0.2	0.3	–	0.3	
		I_{OL} = 12 mA	2.7	–	0.22	0.4	–	0.4	
		I_{OL} = 16 mA	3.0	–	0.28	0.4	–	0.4	
		I_{OL} = 24 mA	3.0	–	0.38	0.55	–	0.55	
		I_{OL} = 32 mA	4.5	–	0.42	0.55	–	0.55	
I_{IN}	Input Leakage Current	V_{IN} = 5.5 V or GND	1.65 to 5.5	–	–	±0.1	–	±1.0	μA
I_{OZ}	3−State Output Leakage Current	V_{OUT} = 0 V to 5.5 V	1.65 to 5.5	–	–	±0.5	–	±5.0	μA

Table 3. DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V_{CC} (V)	T_A = 25°C			−55°C ≤ T_A ≤ 125°C		Units
				Min	Typ	Max	Min	Max	
ALL PARTS									
I_{OFF}	Power Off Leakage Current	V_{IN} = 5.5 V or V_{OUT} = 5.5 V	0	–	–	1.0	–	10	μA
I_{CC}	Quiescent Supply Current	V_{IN} = V_{CC} or GND	5.5	–	–	1.0	–	10	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. The V_{OH} parameter does not apply to devices with open−drain output, NLV18SZ06, NLV18SZ07, NLV18SZT05 and NLV18SZT07.

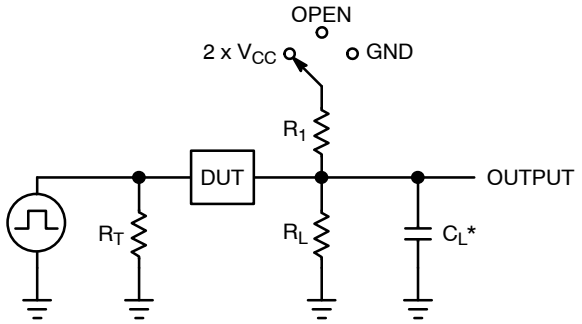
Table 4. AC ELECTRICAL CHARACTERISTICS (t_R = t_F = 3.0 ns)

Symbol	Parameter	Condition	V_{CC} (V)	T_A = 25°C			−55°C ≤ T_A ≤ 125°C		Units
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay, (A or B) to Y (Figures 1 and 2)	R_L = 1 MΩ, C_L = 15 pF	1.65 to 1.95	–	9.1	15	–	15.6	ns
		R_L = 1 MΩ, C_L = 15 pF	2.3 to 2.7	–	5.0	9.0	–	9.5	
		R_L = 1 MΩ, C_L = 15 pF	3.0 to 3.6	–	3.7	6.3	–	6.5	
		R_L = 500 Ω, C_L = 50 pF		–	4.4	7.2	–	7.5	
		R_L = 1 MΩ, C_L = 15 pF	4.5 to 5.5	–	3.1	5.2	–	5.5	
		R_L = 500 Ω, C_L = 50 pF		–	3.7	5.9	–	6.2	
t_{PZH} t_{PZL}	Output Enable Time, (A or $\overline{OE}$ or OE) to Y (Figures 1 and 2)		1.65 to 1.95	–	6.5	9.5	–	10	ns
			2.3 to 2.7	–	3.6	8.5	–	9.0	
			3.0 to 3.6	–	2.8	6.2	–	6.5	
			4.5 to 5.5	–	2.0	5.5	–	5.8	
t_{PHZ} t_{PLZ}	Output Disable Time, (A or $\overline{OE}$ or OE) to Y (Figures 1 and 2)		1.65 to 1.95	–	5.0	10	–	10.5	ns
			2.3 to 2.7	–	3.3	8.0	–	8.5	
			3.0 to 3.6	–	2.7	5.7	–	6.0	
			4.5 to 5.5		2.6	4.7	–	5.0	

Table 5. CAPACITIVE CHARACTERISTICS (t_R = t_F = 3.0 ns)

Symbol	Parameter	Condition	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = 5.5 V, V_{IN} = 0 V or V_{CC}	2.5	pF
C_{OUT}	Output Capacitance	V_{CC} = 5.5 V, V_{IN} = 0 V or V_{CC}	2.5	pF
C_{PD}	Power Dissipation Capacitance (Note 6)	10 MHz, V_{CC} = 3.3 V, V_{IN} = 0 V or V_{CC} 10 MHz, V_{CC} = 5.5 V, V_{IN} = 0 V or V_{CC}	9 11	pF

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no−load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.



C_L includes probe and jig capacitance
R_T is Z_{OUT} of pulse generator (typically 50 Ω)
f = 1 MHz

Figure 1. Test Circuit

Test	Switch Position	C_L, pF	R_L, Ω	R_1, Ω
t_{PLH} / t_{PHL}	Open	See AC Characteristics Table		
t_{PLZ} / t_{PZL}	2 x V_{CC}	50	500	500
t_{PHZ} / t_{PZH}	GND	50	500	500

X = Don't Care

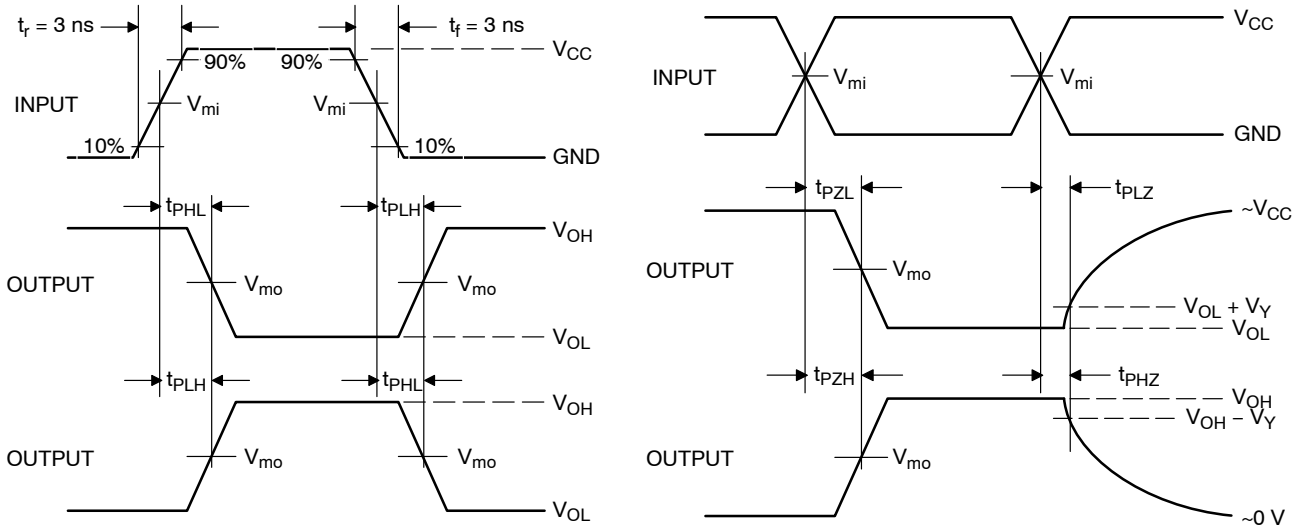


Figure 2. Switching Waveforms

V_{CC}, V	V_{mi}, V	V_{mo}, V		V_Y, V
		t_{PLH}, t_{PHL}	t_{PZL}, t_{PLZ}, t_{PZH}, t_{PHZ}	
1.65 to 1.95	V_{CC}/2	(V_{OH} – V_{OL})/2	V_{CC}/2	0.15
2.3 to 2.7	V_{CC}/2	(V_{OH} – V_{OL})/2	V_{CC}/2	0.15
3.0 to 3.6	V_{CC}/2	(V_{OH} – V_{OL})/2	V_{CC}/2	0.3
4.5 to 5.5	V_{CC}/2	(V_{OH} – V_{OL})/2	V_{CC}/2	0.3

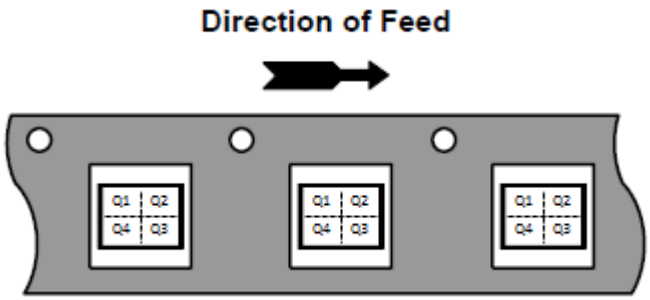
ORDERING INFORMATION

Device	Package	Marking	Pin 1 Orientation (See below)	Shipping†
NLV18SZ00DFT2G	SC−88A	L1	Q4	3000 / Tape & Reel
NLV18SZ02DFT2G	SC−88A	L3	Q4	3000 / Tape & Reel
NLV18SZ04DFT2G	SC−88A	L5	Q4	3000 / Tape & Reel
NLV18SZ06DFT2G (in development)	SC−88A	LF	Q4	3000 / Tape & Reel
NLV18SZ07DFT2G	SC−88A	L7	Q4	3000 / Tape & Reel
NLV18SZ08DFT2G	SC−88A	L2	Q4	3000 / Tape & Reel
NLV18SZ14DFT2G	SC−88A	LA	Q4	3000 / Tape & Reel
NLV18SZ17DFT2G	SC−88A	LX	Q4	3000 / Tape & Reel
NLV18SZ32DFT2G	SC−88A	L4	Q4	3000 / Tape & Reel
NLV18SZ16DFT2G (in development)	SC−88A	LR	Q4	3000 / Tape & Reel
NLV18SZ86DFT2G (in development)	SC−88A	L8	Q4	3000 / Tape & Reel
NLV18SZ125DFT2G	SC−88A	M0	Q4	3000 / Tape & Reel
NLV18SZ126DFT2G (in development)	SC−88A	M2	Q4	3000 / Tape & Reel
NLV18SZU04DFT2G (in development)	SC−88A	L6	Q4	3000 / Tape & Reel
NLV28WZ16DFT2G	SC−88	MR	Q4	3000 / Tape & Reel
NLV28WZU04DFT2G	SC−88	M6	Q4	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

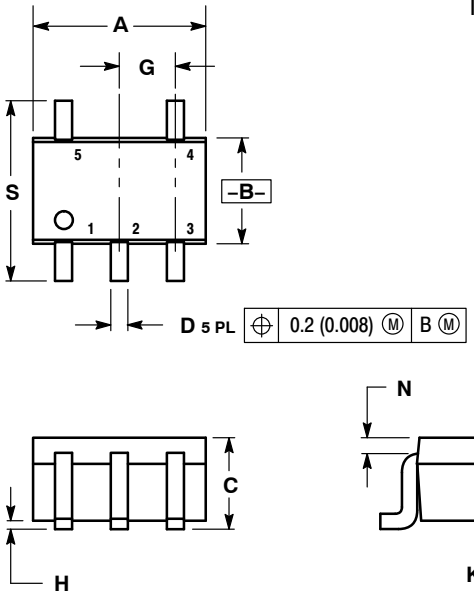
*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

Pin 1 Orientation in Tape and Reel



PACKAGE DIMENSIONS

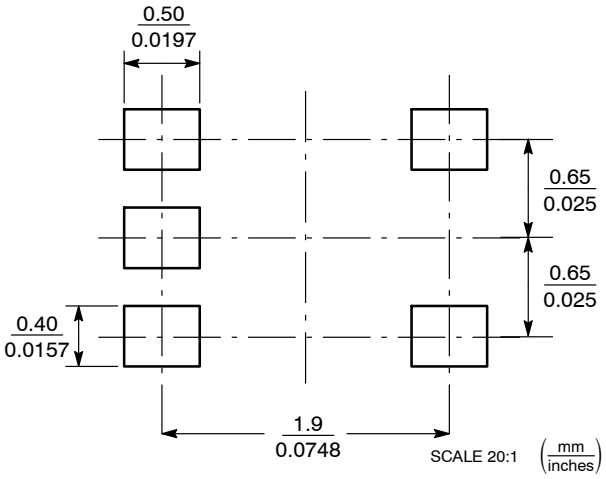
SC−88A (SC−70−5/SOT−353)
CASE 419A−02
ISSUE L



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A−01 OBSOLETE. NEW STANDARD 419A−02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

SOLDER FOOTPRINT

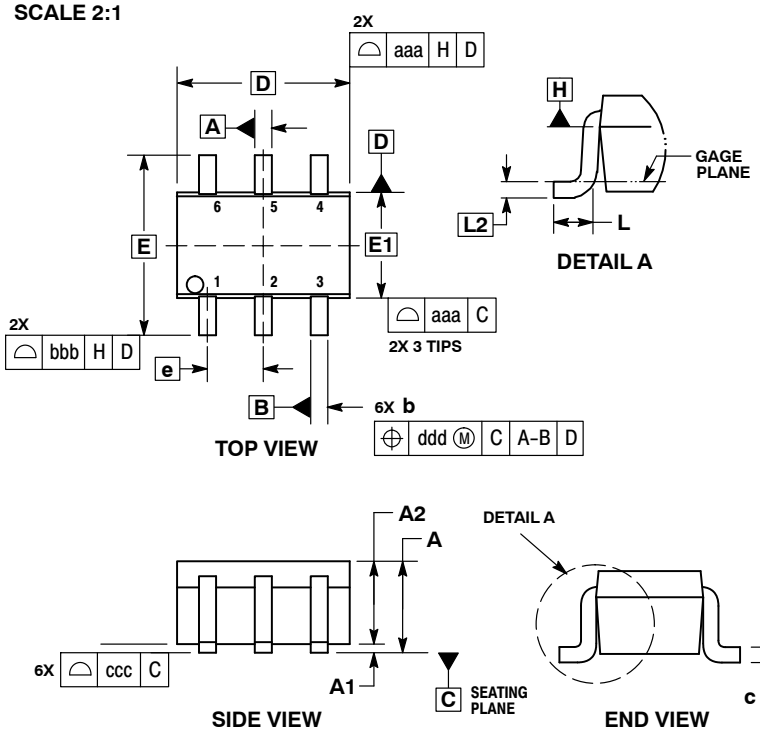


PACKAGE DIMENSIONS

SC−88/SC70−6/SOT−363
CASE 419B−02
ISSUE Y

DATE 11 DEC 2012

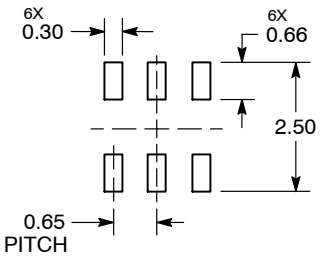
1
SCALE 2:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.10	---	---	0.043
A1	0.00	---	0.10	0.000	---	0.004
A2	0.70	0.90	1.00	0.027	0.035	0.039
b	0.15	0.20	0.25	0.006	0.008	0.010
C	0.08	0.15	0.22	0.003	0.006	0.009
D	1.80	2.00	2.20	0.070	0.078	0.086
E	2.00	2.10	2.20	0.078	0.082	0.086
E1	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65 BSC			0.026 BSC		
L	0.26	0.36	0.46	0.010	0.014	0.018
L2	0.15 BSC			0.006 BSC		
aaa	0.15			0.006		
bbb	0.30			0.012		
ccc	0.10			0.004		
ddd	0.10			0.004		

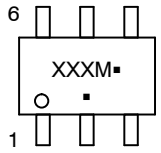
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

PUBLICATION ORDERING INFORMATION

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Phone: 011 421 33 790 2910

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For additional information, please contact your local Sales Representative

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