TEXAS INSTRUMENTS

GC1115 Daughterboard EVM

User's Guide

December 2005

SLWU024

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GC1115 Daughterboard Description

The GC1115 Daughterboard and GC101 EVM comprise a two-part daughterboard and motherboard used for demonstrating the GC1115 CFR. The GC1115 Daughterboard hardware is a plug-in board to the GC101 EVM.

The GC1115 is a flexible, programmable, wideband crest factor reduction (CFR) processor with a maximum composite bandwidth of 20 MHZ. The GC1115 selectively reduces the peak-to-average ratio (PAR) of wideband digital signals provided in quadrature (I & Q) format, such as those used in third-generation (3G) code division multiple access (CDMA) wireless applications. Reducing the PAR of digital signals can improve the efficiency of follow-on power amplifiers (PAs), ease the D/A converter requirements and eliminate the out-of-band spectral regrowth caused by simple hard limiting.

This document will describe the hardware portion of the GC1115 and its interface to the GC101 EVM. More information about the GC101 EVM can be found in the GC101 EVM User's Guide. Figure 1-1 is a high level block diagram of the GC101 and the interface it provides to the GC1115. Figure 1-2 is a block diagram of the GC1115 Daughterboard.

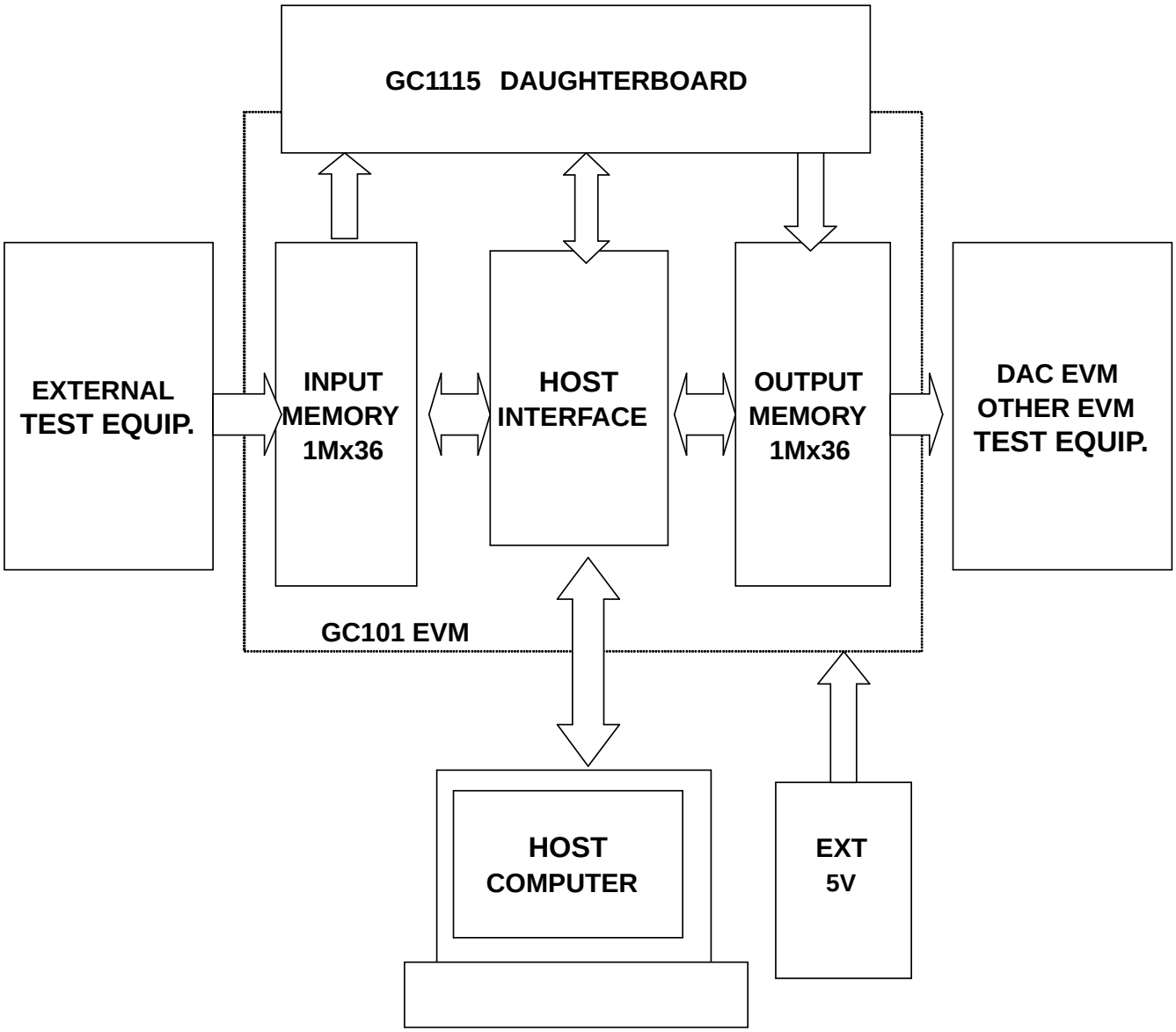

Figure 1-1. GC101 EVM and GC1115 Daughterboard

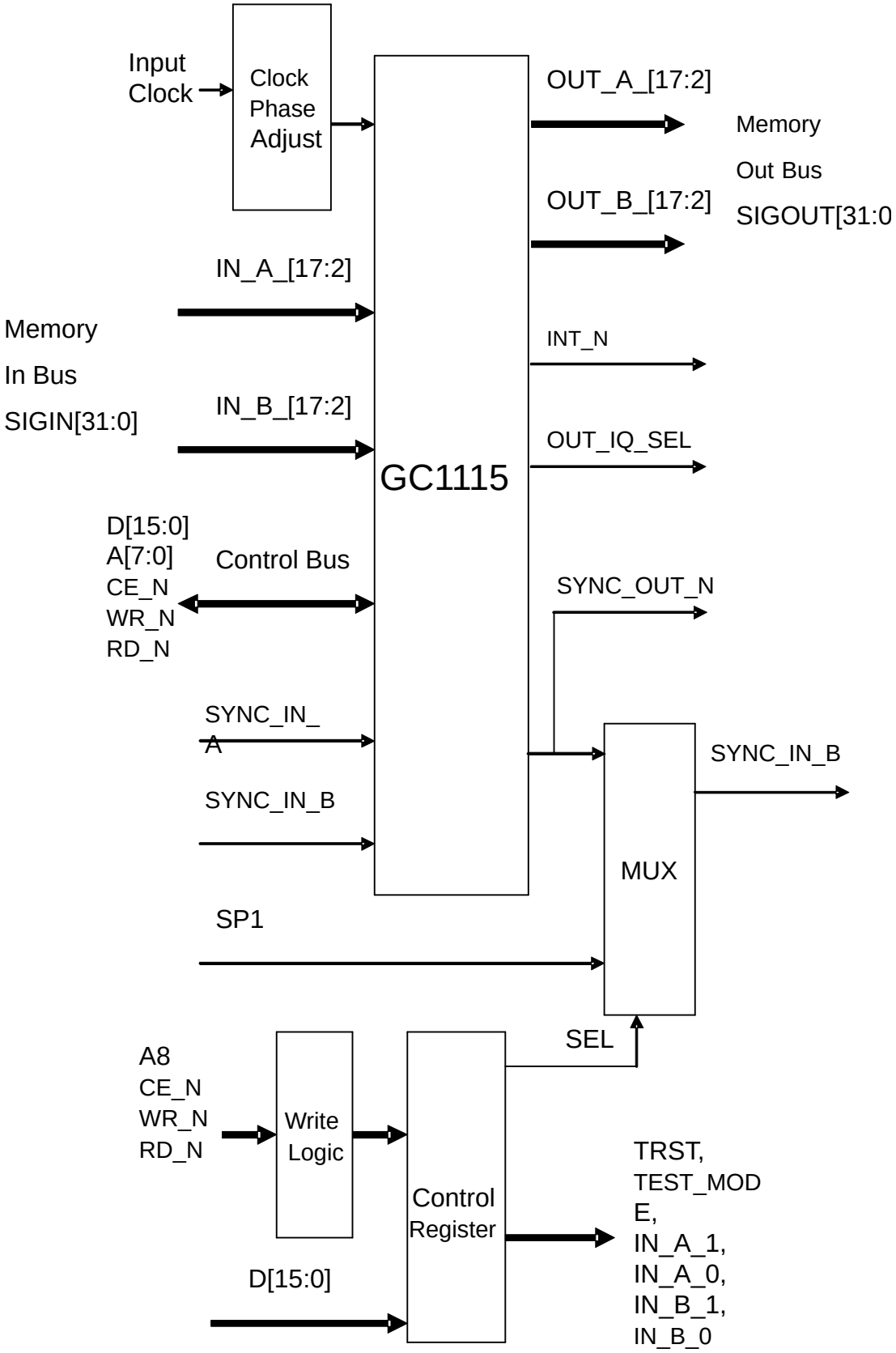

Figure 1-2. GC1115 Daughterboard Block Diagram

1.1 GC1115 Daughterboard to GC101 EVM I/O Description

The GC1115 Daughterboard has a PC-133 form-factor that utilizes the 168-pin DIMM memory connector. The 168 pin interface signals are divided into several groups:

- CLK+: Input Clock for GC1115
- Memory Input Bus: 36 inputs used to stimulate the GC1115 inputs
  - SIGIN[15..0]: Memory Input Bus A
  - SIGIN[31..16]: Memory Input Bus B
  - SYNCIN+: SYNC_A_N Input. Used to synchronize the GC1115
  - SP1: Option for providing a SYNC_B_N signal from GC101
  - SP2-SP4: Unused spare inputs
- Memory Output Bus: 36 outputs from the two GC1115 output busess, sent back to the GC101 EVM for recording and/or output
  - SIGOUT[15..0]: Memory Output Bus A
  - SIGOUT[31..16]: Memory Output Bus B
  - SYNCOUT+: Sync Output. Used to output synchronization signal from GC1115
  - SP5: OUT_IQ_SEL. Used to identify I and Q data during multiplexed I/Q output mode
  - SP6: INT_N. Active low interrupt
  - SP7, SP8: Unused spare outputs
- Control Bus: Bus to program the internal registers
  - 16 Bidirectional data lines
  - 8 Address lines for GC1115
  - 1 Address line for board control register
  - Controls $\overline{CE}$, $\overline{RD}$, $\overline{WR}$, and $\overline{RST}$
- JTAG: 5 pin JTAG Test Port for GC1115
  - $\overline{TRST}$, TCLK, TMS, TDI, TDO
- Power: Input power to Daughterboard
  - VDUT1: 3.3 VDC power from GC101 EVM
  - GND: 3.3 VDC return from GC101 EVM

See the GC101 EVM User's Guide for the 168-pin DIMM connector pin description. The pins used for the GC1115 Daughterboard are shown in the schematic at the end of this document.

1.2 GC1115 Daughterboard Memory Input and Output

The Memory Input Bus and Special Input Bus connect through the GC101 36-bit Memory Input Bus. The Memory Input Bus is mapped to the GC1115 and one bit (SP1) of the Special Input Bus is mapped to an input of a sync multiplexer. The GC101 EVM data input formats are based on input files from the PC-supplied software. The data buses between the boards map as follows:

GC101 DID[15..0] -> maps to GC1115 IN_A[17..2]. Inputs IN_A[1..0] are set by the control register.

GC101 DID[31..16] -> maps to GC1115 IN_B[17..2]. Inputs IN_B[1..0] are set by the control register.

GC101 DID[32] -> SP1.

GC101 D[33-35] -> Unused

The GC1115 data input ports can either be 2's complement or unsigned format.

The Memory Output Bus, and Special Output Bus pins are used to monitor data from the GC1115 Daughterboard.

Memory Output Bus:

GC101 DOD[15..0] -> maps to GC1115 OUT_A[17..2]. OUT_A[1..0] go to test points to allow for measuring signal timing and levels.

GC101 DOD[31..16] -> maps to GC1115 OUT_B[17..2]. OUT_B[1..0] go to test points to allow for measuring signal timing and levels.

The Special Output Bus has several additional signals:

GC1115 SP5 -> maps to GC101 DOD[32] . This is the OUT_IQ_SEL from the GC1115.

GC1115 SP6 -> maps to GC101 DOD[33]. This is the INT_N signal from the GC1115.

GC1115 SP7 and SP8 are not used

1.3 Input Clock

The GC1115 Daughterboard operates with a single-ended CMOS input clock. The clock enters the daughterboard on pin 34, and has pullup and pulldown termination resistors located near U5 (CDCVF25081). U5 is a Phase-Lock Loop Clock Driver, which provides the clock to the GC1115. With the use of delay module U10, the user can adjust the phase of the clock. The board default setup is with this part removed and an output of U5 connected to the feedback input. This provides a zero delay clock source to the GC1115 with respect to the input clock from the GC101. The input clock phase and frequency can also by changed by an adjustable clock skew buffer device on the GC101. See the GC101 EVM User's Guide for more information on this.

1.4 Input Sync

The GC1115 has two input sync pins, SYNC_A_N and SYNC_B_N. The GC1115 Daughterboard routes an input sync from pin 37 to the SYNC_A_N input of the GC1115. This signal has a test point to allow for easy monitoring. The board also contains a sync multiplexer that allows the user to send either the GC1115 output sync (SYNC_OUT_N) or SP1 from the input connector to the SYNC_B_N signal of the GC1115. The sync signals are used to provide a hardware event for the GC1115 internal sync registers. See the data sheet for more information on the operation of these sync signals.

1.5 Output Clock

The GC1115 Daughterboard provides a test point to allow monitoring of the output clock. This signal does not go to the output connector. There are several internal registers that effects the frequency and relationship of the output clock with respect to the core clock. See the data sheet for more information on this.

1.6 Output Sync

The GC1115 Daughterboard routes the output sync signal (OUT_SYNC_N) to both the output connector and a sync multiplexer. The multiplexer output is routed to the SYNC_B_N input of the GC1115. If selected by the control register, this signal can be used to syncronize the GC1115. SYNC_OUT_N trace has a test point to allow for monitoring.

1.7 Output Interrupt

The GC1115 Daughterboard routes an active low interrupt signal (INT_N) to pin 124 of the output connector. This signal is useful when interfacing a GC1115 with a DSP or microprocessor.

1.8 Output I Q Select

The GC1115 Daughterboard routes an I/Q select signal (OUT_IQ_SEL) to pin 124 of the output connector. This signal indicates whether the data present at the output is I (low) or Q (high). This signal is only active in multiplexed I/Q output modes.

1.9 Control Bus

The GC1115 has a 16-bit data Microprocessor port. The $\overline{CE}$, $\overline{RD}$, $\overline{WR}$, and $\overline{RST}$ control signals are active low and map directly from the GC101 EVM. The Address Bus A[8..0] is static when the control signals are asserted.

The Bidirectional Control Data D[15..0] provides the data path between the GC101 EVM and the GC1115 Daughterboard.

The $\overline{CE}$, $\overline{RD}$, $\overline{WR}$, and $\overline{RST}$ signals have test points for monitoring.

1.10 JTAG Bus

The GC1115 JTAG Bus is connected through the GC101 EVM connector. The serial chain resistors are on the GC101 EVM. The JTAG is not currently used.

1.11 Power Supplies

The 3.3-V input power is supplied from the GC101 EVM power supplies. The 1.2-V core and 1.2V PLL power for the GC1115 are supplied from regulators on the daughterboard. The board provides options to provide these two sources from two seperate regulators, combined from one regulator, or from external sources. On-board jumpers allow the user to bypass the regulators and use an external power source, if desired. The function of the power supply jumpers are as follows:

Table 1-1. Power Supply Jumper List

JUMPER	FUNCTION	PINS 1-2	PINS 2-3	PINS 2-4	DEFAULT
W1	Selects regulator or external power for core supply	External power provided from connector J2	Power provided from regulator U8	N/A	2-3
W2	Selects regulator or external power for PLL supply	Power provided from regulator U9	External power provided from connector J3	Power provided from core supply	1-2
W3	Regulator enable	Disables both regulators	Enables both regulators	N/A	2-3

GC1115 Daughterboard Operational Procedure

This chapter describes the operation of the GC1115 Daughterboard with the GC101 EVM. The following sections are overviews of the hardware specifications for the GC101 EVM and GC1115 Daughterboard. For more information, the user is encouraged to read the GC101 User's Guide, and the GC Studio documentation, which is included with this software package.

2.1 GC101 EVM Hardware Features

The GC101 EVM provides the following features:

- A complete digital data path which allows the loading, processing, and analysis of a stream of digital data. The loading and analysis is performed through 1Meg Input and Output memory banks.
- Signal processing is performed through a 168-pin expansion slot which is designed to accommodate the GC1115 Daughterboard.
- Digitally controlled internal clocks and output clocks capable of synchronizing the daughterboard, the EVM capture memories, and external test and measurement equipment.
- The EVM communicates to input memory, output memory, and the GC1115 Daughterboard over an IEEE 1284 EPP or ECP parallel port. The GC1115 internal registers are programmed through this interface.

2.2 Hardware Requirements

Required Elements before Installation:

- GC101 EVM, external 5V power supply, high-speed parallel port cable, and GC1115 Software CDROM.
- GC1115 Daughterboard
- Computer with:
  - Administrator privileges
  - Supported OS of Win98 Rel.2, WinME, Win2000 SP1, WinXP, or WinXP Prof.
  - Parallel port operating in ECP for LPT1 (BIOS)

2.3 EVM Setup

2.3.1 Deliverables List

The following items should be delivered and comprise the GC1115SEK:

- GC101 Motherboard
- GC101 Motherboard power cable and power supply
- High performance parallel port cable
- GC1115 Daughtercard
- A current copy of the GC Studio application, including the GC1115 plug-in
- A current copy of the GC Scripter application, for advanced setup and use

2.3.2 Installation Instructions

The software should be installed before connecting the boards to the computer. GCStudio_Setup.exe should have been provided either through the web, or on a CD with this package. Double-click on the icon for the GCStudio_Setup.exe program. This will launch an installshield wizard. See the GC Studio Documentation for instructions on how to operate the GC1115 with a GC101 EVM.

Physical Description

This chapter describes the physical characteristics and PCB layout of the EVM and lists the components used on the module.

3.1 PCB Layout

The EVM is constructed on a 8-layer, 3.3-inch x 5.25-inch, 0.056-inch thick PCB using FR-4 material. Figure 3-1 through Figure 3-6 show the PCB layout for the EVM.

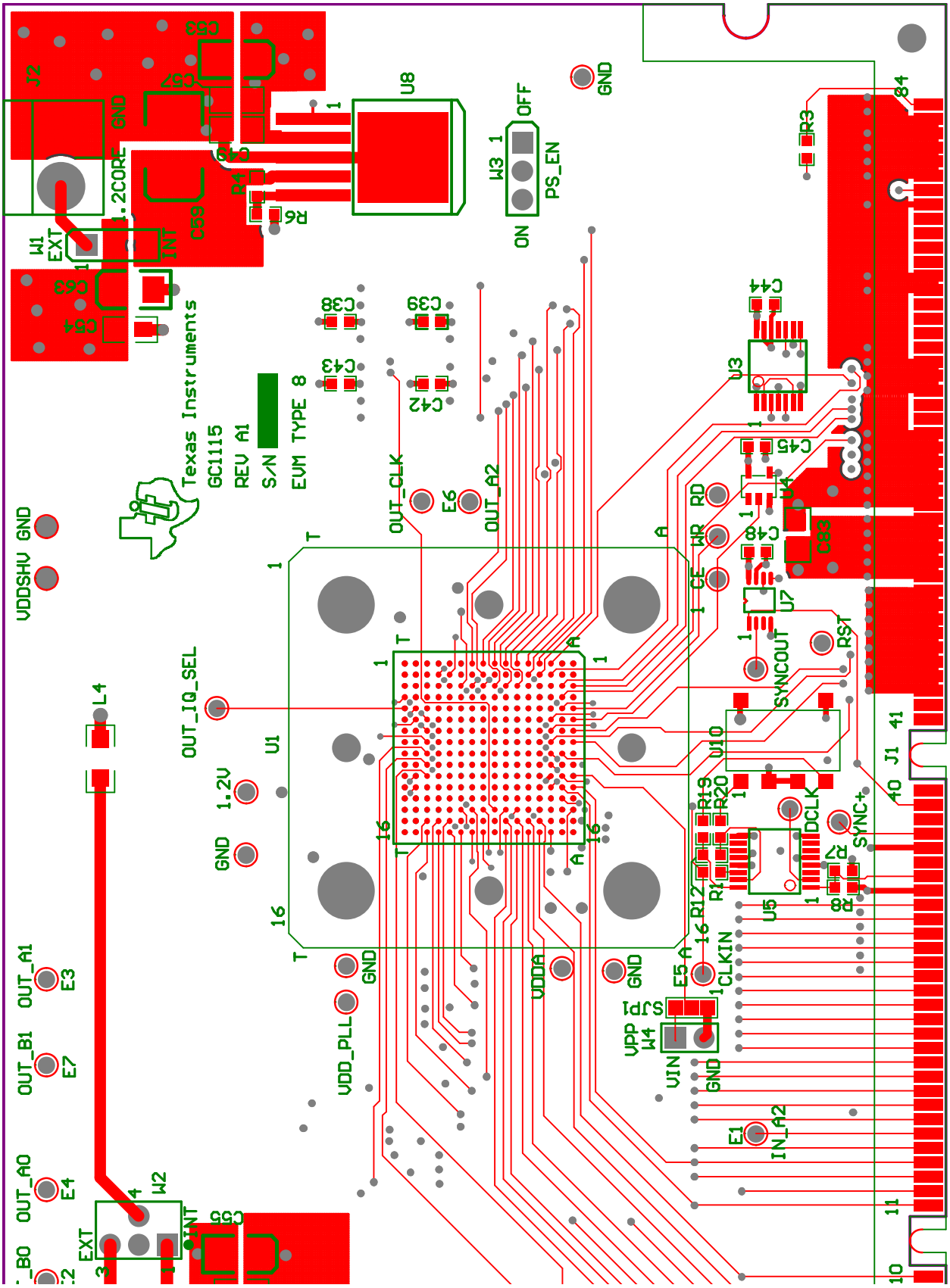

Figure 3-1. Top Layer 1

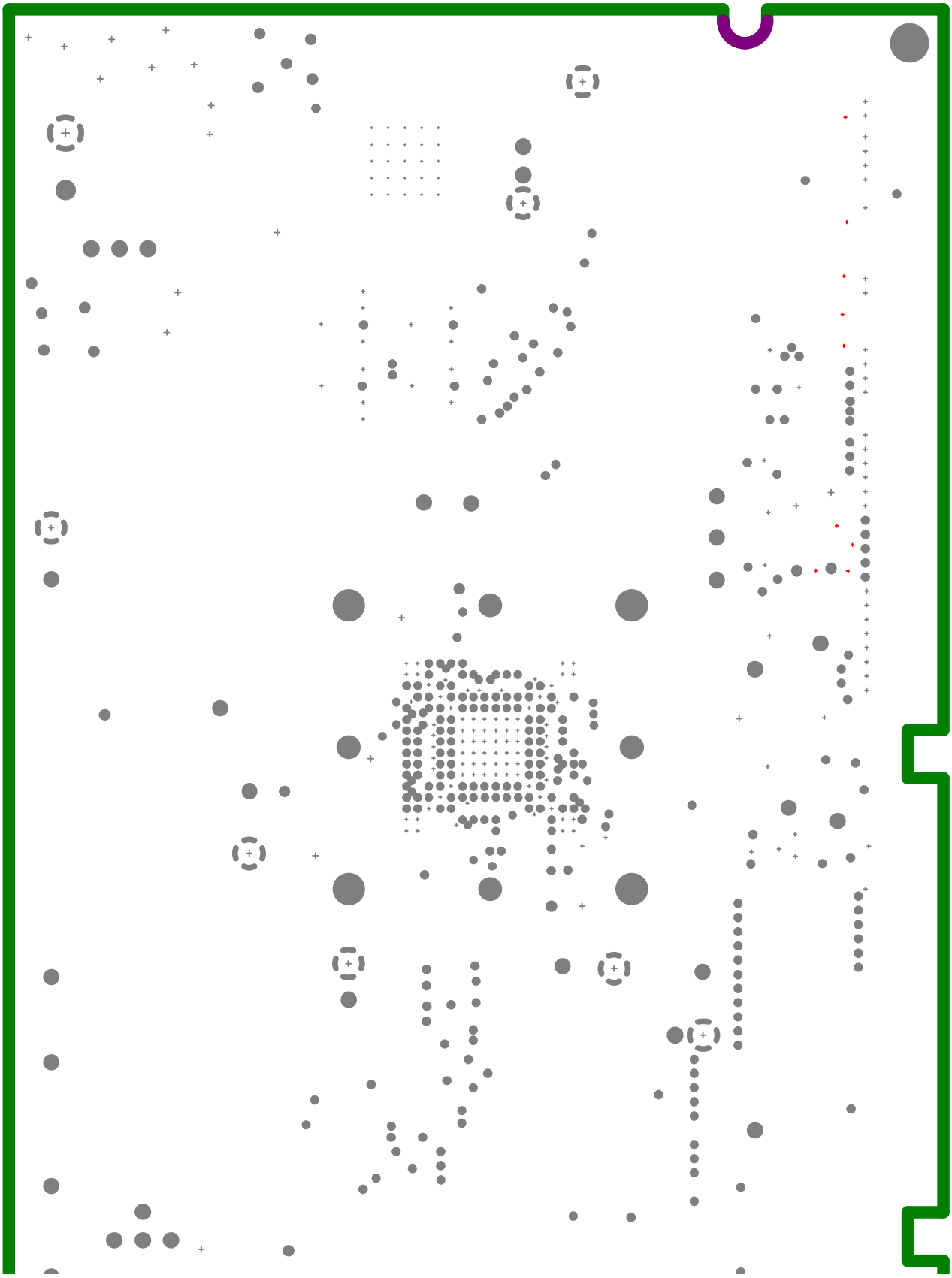

Figure 3-2. Ground Plane Layer 2

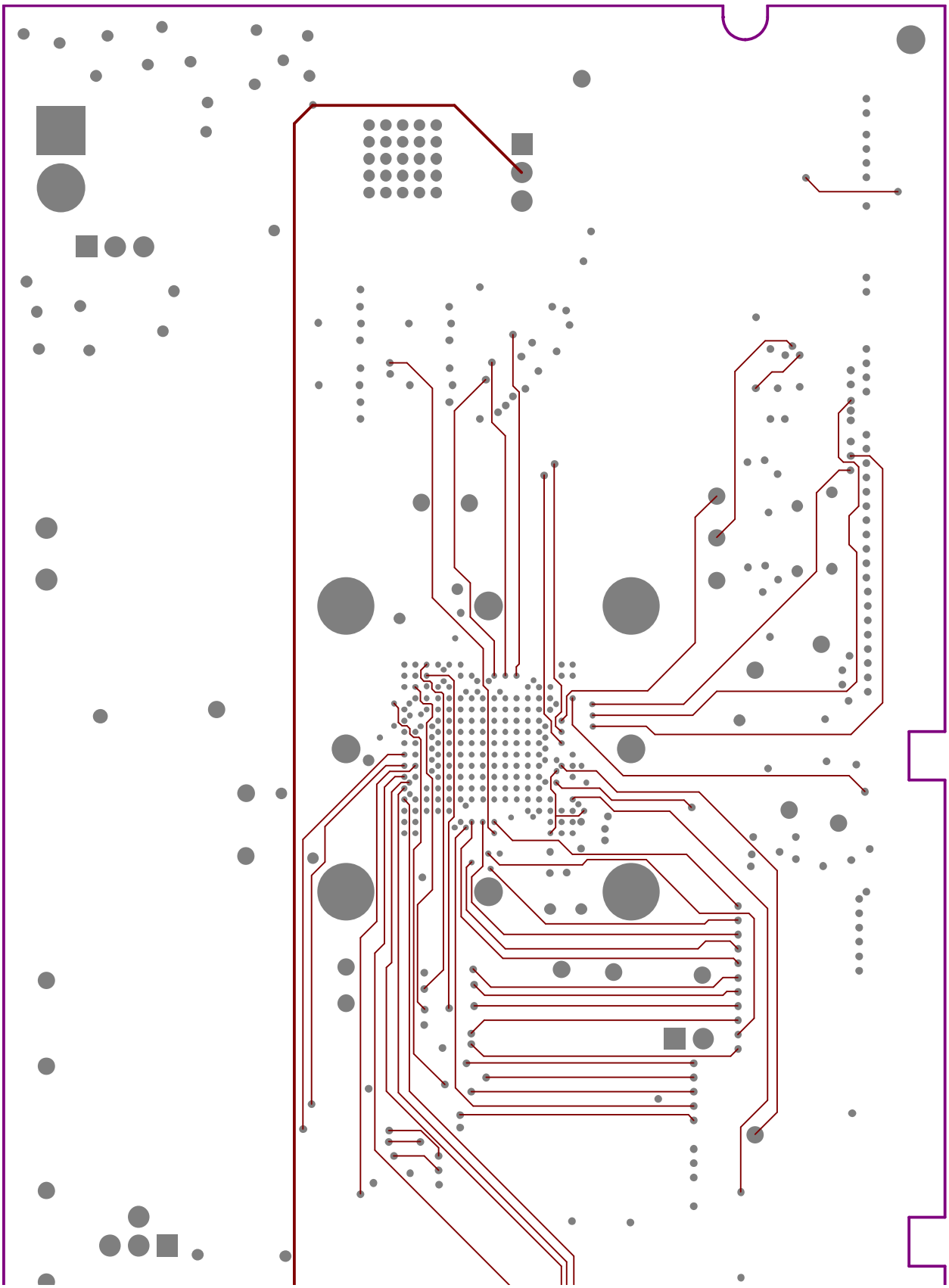

Figure 3-3. Signal Layer 3

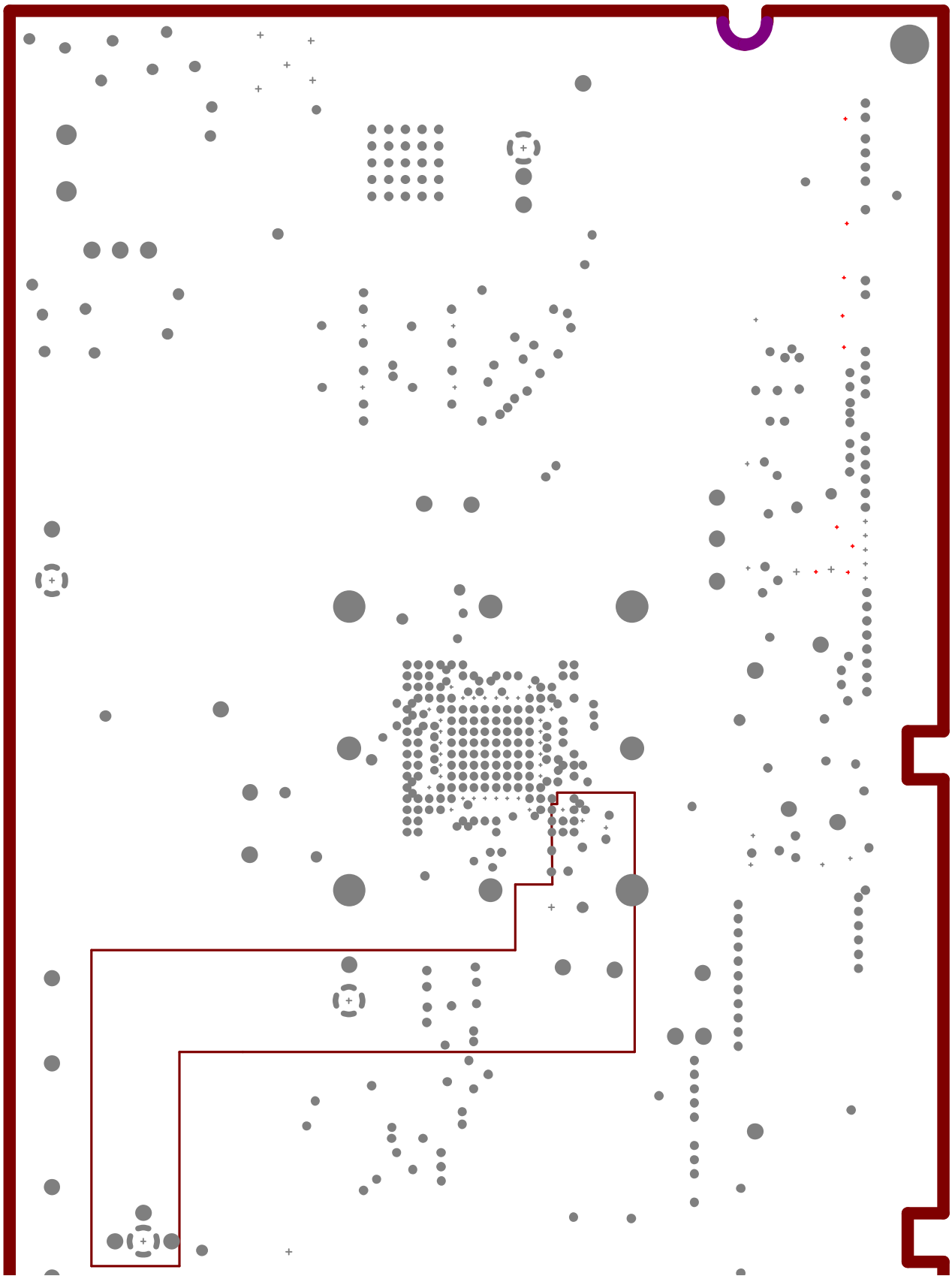

Figure 3-4. Signal Layer 4

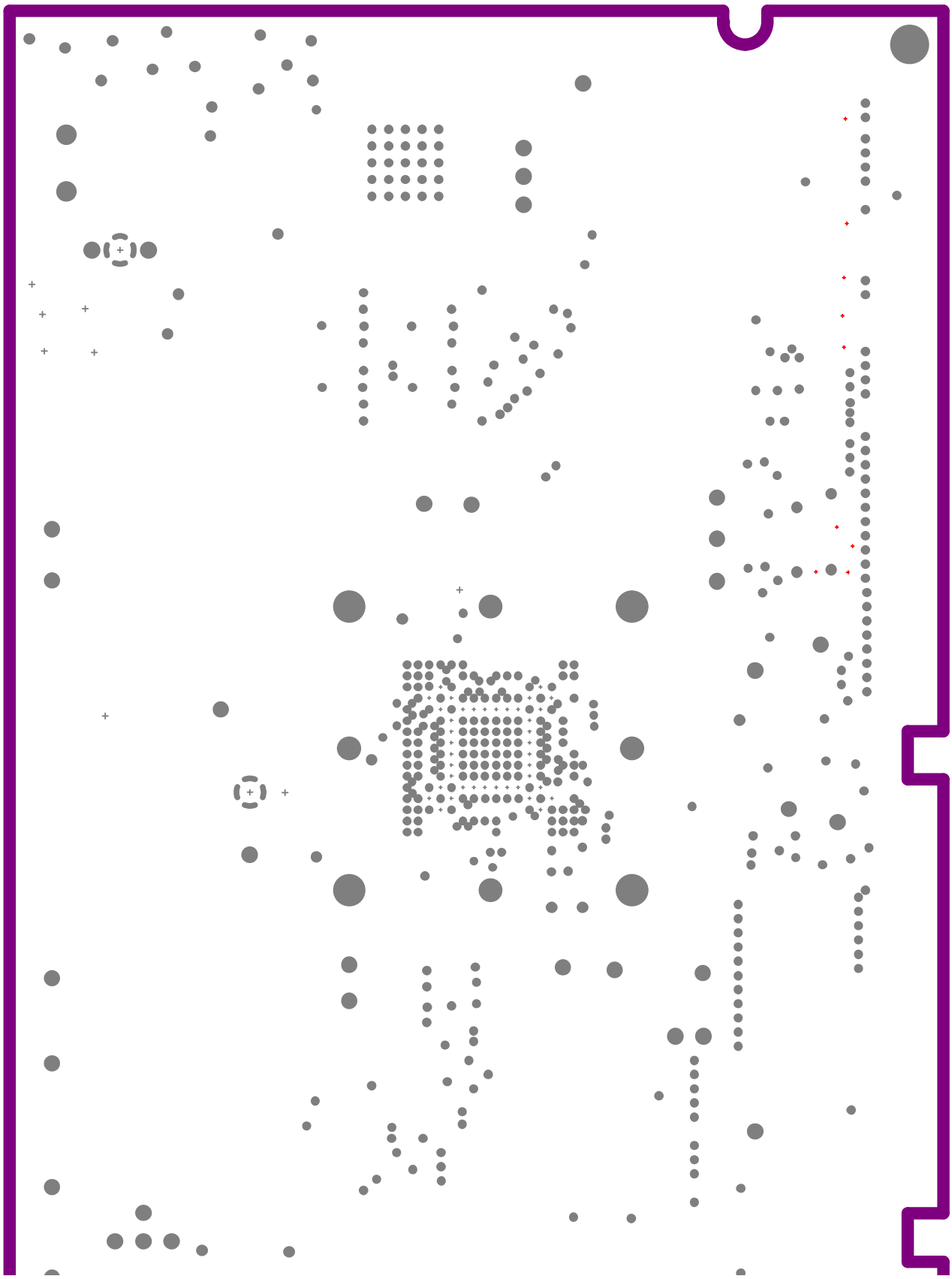

Figure 3-5. Power Plane Layer 5

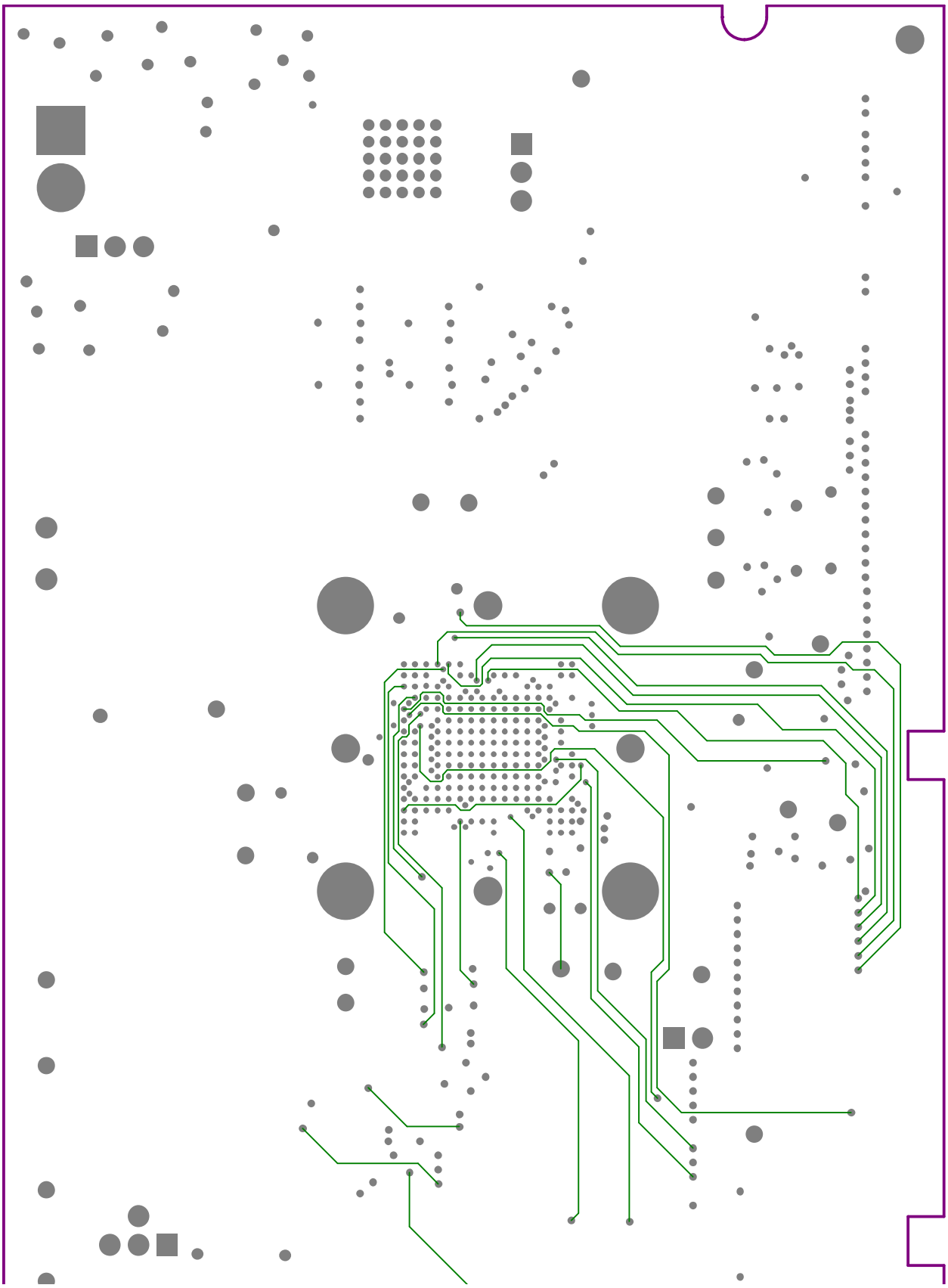

Figure 3-6. Layer 6

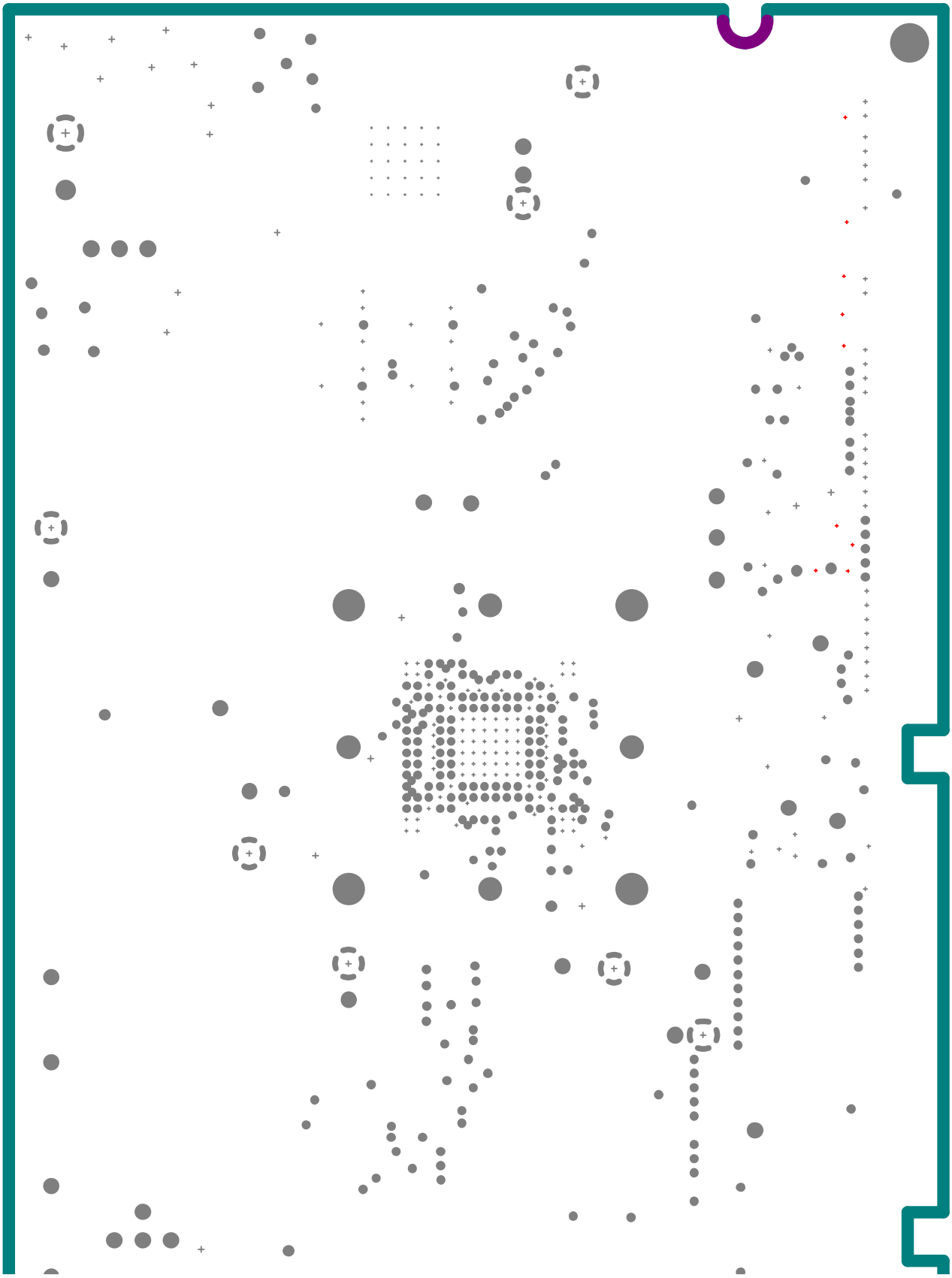

Figure 3-7. Layer 7

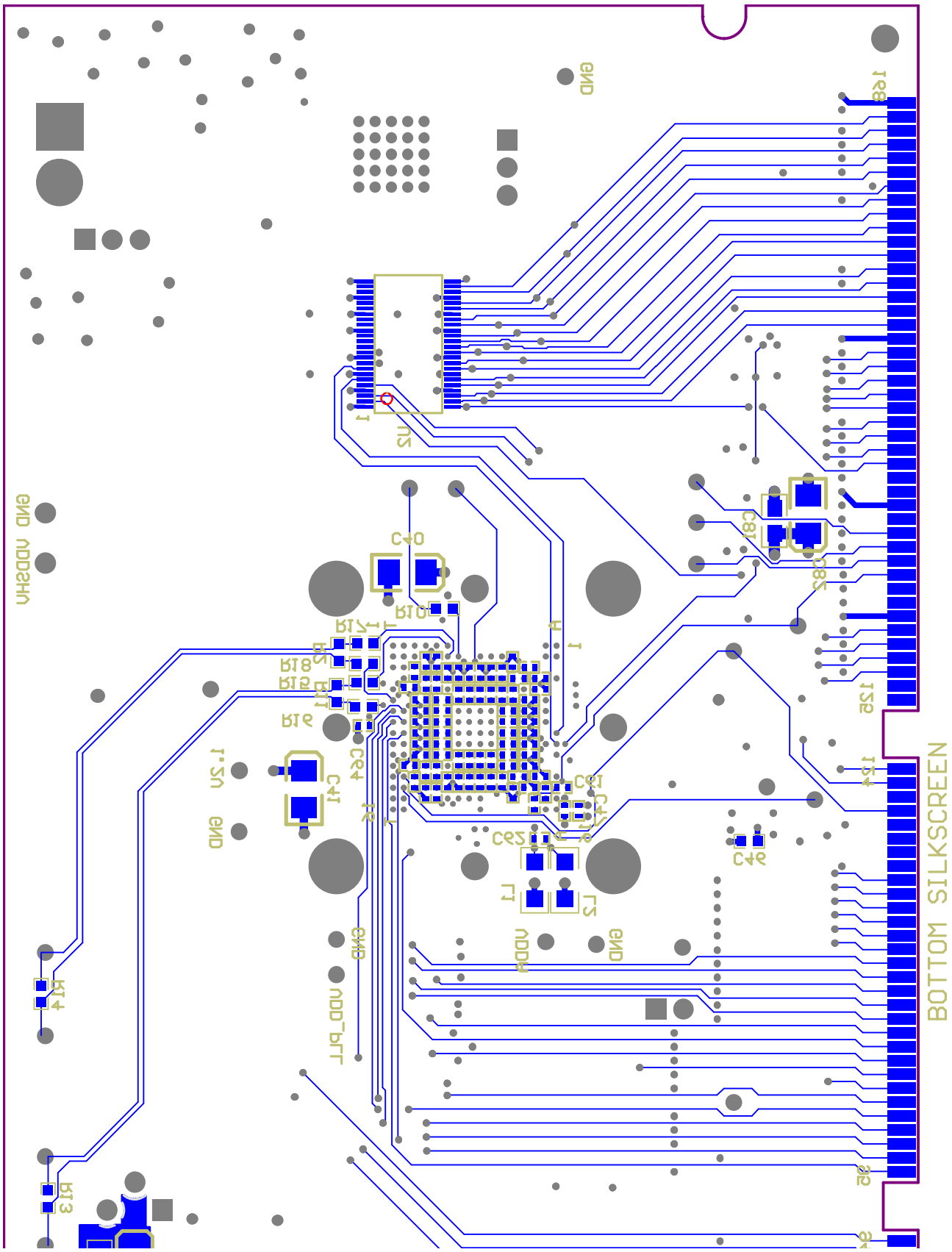

Figure 3-8. Bottom Layer 8

3.2 Parts List

Table 3-1 lists the parts used in constructing the EVM.

Table 3-1. Bill of Materials for GC1115 EVM

VALUE	QTY	PART NUMBER	MANUFACTURER	REF DES	NOT INSTALLED
CAPACITORS					
47uF, 20V, 10%, Capacitor	2	ECS-T1AD476R	PANASONIC	C59 C60	
2.2 µF, 20 V, 10%, Capacitor	1	ECS-T1DX225R	PANASONIC	C40	
10 µF, 20 V, 10%, Capacitor	6	ECS-T1DX106R	PANASONIC	C41 C53 C55 C56 C63 C82	
1uF, 16V, 10%, Capacitor	3		PANASONIC	C57 C58 C83	
0.1 µF, 16 V, 10%, Capacitor	5	ECJ-2VB1C104K	PANASONIC	C49 C51 C52 C54 C81	
0.1 µF, 16 V, 10%, Capacitor	8	ECJ-1VB1C104K	PANASONIC	C38 C39 C42-C46 C48	
0.01 µF, 16 V, 10%, Capacitor	2	ECJ-0EF1C103Z	PANASONIC	C61 C99	C64
0.1 µF, 16 V, 10%, Capacitor	70	ECJ-0EF1C104Z	PANASONIC	C1-C37 C47 C50 C65-C80 C84-C98	
47pF,50V,+/- 5%, Capacitor	0	ECJ-OEC1H470J	PANASONIC		C61 C100
RESISTORS					
100 Ω resistor, 1/16 W, 1%	3	ERJ-3EKF1000V	PANASONIC	R3 R13 R14	
130 Ω resistor, 1/16 W, 1%	3	ERJ-3EKF1300V	PANASONIC	R7 R8 R10	
140 Ω resistor, 1/16 W, 1%	2	ERJ-3EKF1400V	PANASONIC	R2 R11	
165 Ω resistor, 1/16 W, 1%	4	ERJ-3EKF1650V	PANASONIC	R15 R16 R17 R18	
0 Ω Resistor, 1/16 W, 1%	3	ERJ-3GEY0R00V	PANASONIC	R4 R5 R12	R19 R20
30.1 kΩ Resistor, 1/16 W, 1%	0	ERJ-3EKF3012V	PANASONIC		R6 R9
22.1 Ω resistor, 1/16 W, 1%	1	ERJ-3EKF22R1V	PANASONIC	R1	
CONNECTORS, HEADERS, FERRITE BEADS and TEST POINTS					
Red test point	13	5000k	KEYSTONE	TP4 TP5 TP7-TP16 TP18	
Black test point	6	5001k	KEYSTONE	TP1 TP2 TP3 TP6 TP17 TP19	
TESTPOINT	0				E1-E7
3POS-JUMPER SURFACE MOUNT	1			SJP1	
CON_2TERM_SCREW	2	KRMZ3	LUMBERG	J2 J3	
2POS-HEADER	1	TWS-150-07-L-S	SAMTEC	W4	
3POS-HEADER	2	TWS-150-07-L-S	SAMTEC	W1 W3	
4POS-HEADER	1		SAMTEC	W2	
FERRITE BEADS	3	EXC-ML32A680U		L1 L2 L4	
ICs					
GC1115_PBGA	1	GC1115IZDJ	Texas Instruments	U1	

Table 3-1. Bill of Materials for GC1115 EVM (continued)

VALUE	QTY	PART NUMBER	MANUFACTURER	REF DES	NOT INSTALLED
SN74LVC08APWR	1	SN74LVC08APWR	Texas Instruments	U3	
SN74ALVTH16374	1	SN74ALVTH16374GR	Texas Instruments	U2	
SN74LVC2G157	1	SN74LVC2G157DCTR	Texas Instruments	U7	
SN74LVC1G04	1	SN74LVC1G04DBVR	Texas Instruments	U4	
TPS75701	2	TPS75701KTTT	Texas Instruments	U8 U9	
DELAY LINE	0	CDA1005	ELMEC		U10
CDCVF25081	1	CDCVF25081PW	Texas Instruments	U5	

3.3 Schematics

This chapters contains the schematics for the EVM.

Revision History		
REV	ECN Number	Approved

J1A
168-CONN-AMP-RA-TH

SIGIN[31]	1	IN_A_17	
SIGIN[30]	2	IN_A_16	
SIGIN[29]	3	IN_A_15	
SIGIN[28]	4	IN_A_14	
SIGIN[27]	5	IN_A_13	
SIGIN[26]	6	IN_A_12	
SIGIN[25]	7	IN_A_11	
SIGIN[24]	8	IN_A_10	
SIGIN[23]	9	IN_A_9	
SIGIN[22]	10	IN_A_8	
SIGIN[21]	11	IN_A_7	
SIGIN[20]	12	IN_A_6	
SIGIN[19]	13	IN_A_5	
SIGIN[18]	14	IN_A_4	
SIGIN[17]	15	IN_A_3	
SIGIN[16]	16	IN_A_2	
SIGIN[15]	17	IN_B_17	
SIGIN[14]	18	IN_B_16	
SIGIN[13]	19	IN_B_15	
SIGIN[12]	20	IN_B_14	
SIGIN[11]	21	IN_B_13	
SIGIN[10]	22	IN_B_12	
SIGIN[9]	23	IN_B_11	
SIGIN[8]	24	IN_B_10	
SIGIN[7]	25	IN_B_9	
SIGIN[6]	26	IN_B_8	
SIGIN[5]	27	IN_B_7	
SIGIN[4]	28	IN_B_6	
SIGIN[3]	29	IN_B_5	
SIGIN[2]	30	IN_B_4	
SIGIN[1]	31	IN_B_3	
SIGIN[0]	32	IN_B_2	
GND	33		
CLK+	34		
CLK-	35		
GND	36		
SYNCIN+	37		
SYNCIN-	38		
SP1	39	SP1	
SP2	40		
SP3	41		
SP4	42		

IN_A [2..17]
IN_B [2..17]
E1

U1A
GC1115_PBGA

IN_A_17	G16	IN_A_17	
IN_A_16	G15	IN_A_16	
IN_A_15	F16	IN_A_15	
IN_A_14	G14	IN_A_14	
IN_A_13	F15	IN_A_13	
IN_A_12	E16	IN_A_12	
IN_A_11	F14	IN_A_11	
IN_A_10	E15	IN_A_10	
IN_A_9	D16	IN_A_9	
IN_A_8	D15	IN_A_8	
IN_A_7	B12	IN_A_7	
IN_A_6	A13	IN_A_6	
IN_A_5	B11	IN_A_5	
IN_A_4	A12	IN_A_4	
IN_A_3	C9	IN_A_3	
IN_A_2	B10	IN_A_2	
IN_A_1	A10	IN_A_1	
IN_A_0	A9	IN_A_0	
IN_B_17	P15	IN_B_17	
IN_B_16	L14	IN_B_16	
IN_B_15	P16	IN_B_15	
IN_B_14	K14	IN_B_14	
IN_B_13	N15	IN_B_13	
IN_B_12	N16	IN_B_12	
IN_B_11	J14	IN_B_11	
IN_B_10	M15	IN_B_10	
IN_B_9	M16	IN_B_9	
IN_B_8	L15	IN_B_8	
IN_B_7	L16	IN_B_7	
IN_B_6	K15	IN_B_6	
IN_B_5	K16	IN_B_5	
IN_B_4	J15	IN_B_4	
IN_B_3	J16	IN_B_3	
IN_B_2	H15	IN_B_2	
IN_B_1	H16	IN_B_1	
IN_B_0	H14	IN_B_0	
SYNC_B_N	T14	SYNC_B_N	(Sh 2) SYNC_B_N
IN_CLK	C12	IN_CLK	(Sh 2) CLK1
SYNC_A_N	R14	SYNC_A_N	SYNC+
D15	D2	D15	
D14	D1	D14	
D13	F3	D13	
D12	E2	D12	
D11	E1	D11	
D10	F2	D10	
D9	G3	D9	
D8	F1	D8	
D7	H3	D7	
D6	G2	D6	
D5	G1	D5	
D4	H2	D4	
D3	H1	D3	
D2	J1	D2	
D1	J2	D1	
D0	K1	D0	
A0	C2	A0	
A1	C1	A1	
A2	C6	A2	
A3	B3	A3	
A4	A3	A4	
A5	B4	A5	
A6	C7	A6	
A7	B5	A7	
RD_N	B6	RD_N	
WR_N	A5	WR_N	
CS_N	A6	CS_N	
RESET_IN	B13	RESET_IN	
TCK	C8	TCK	
TDO	A7	TDO	
TDI	A8	TDI	
TMS	B9	TMS	
TRST	B8	TRST	
TEST_MODE	B7	TEST_MODE	

OUT_A_17	R5	OUT_A_17	
OUT_A_16	P7	OUT_A_16	
OUT_A_15	T4	OUT_A_15	
OUT_A_14	R4	OUT_A_14	
OUT_A_13	P6	OUT_A_13	
OUT_A_12	T3	OUT_A_12	
OUT_A_11	R3	OUT_A_11	
OUT_A_10	P2	OUT_A_10	
OUT_A_9	P1	OUT_A_9	
OUT_A_8	N2	OUT_A_8	
OUT_A_7	L3	OUT_A_7	
OUT_A_6	N1	OUT_A_6	
OUT_A_5	M2	OUT_A_5	
OUT_A_4	K3	OUT_A_4	
OUT_A_3	M1	OUT_A_3	
OUT_A_2	J3	OUT_A_2	
OUT_A_1	L2	OUT_A_1	OUT_A_1 (Sh 2)
OUT_A_0	L1	OUT_A_0	OUT_A_0 (Sh 2)
OUT_B_17	T13	OUT_B_17	
OUT_B_16	P11	OUT_B_16	
OUT_B_15	R12	OUT_B_15	
OUT_B_14	T12	OUT_B_14	
OUT_B_13	R11	OUT_B_13	
OUT_B_12	P10	OUT_B_12	
OUT_B_11	T11	OUT_B_11	
OUT_B_10	R10	OUT_B_10	
OUT_B_9	P9	OUT_B_9	
OUT_B_8	T10	OUT_B_8	
OUT_B_7	R9	OUT_B_7	
OUT_B_6	T9	OUT_B_6	
OUT_B_5	T8	OUT_B_5	
OUT_B_4	R8	OUT_B_4	
OUT_B_3	T7	OUT_B_3	
OUT_B_2	R7	OUT_B_2	
OUT_B_1	T6	OUT_B_1	OUT_B_1 (Sh 2)
OUT_B_0	R6	OUT_B_0	OUT_B_0 (Sh 2)
SYNC_OUT_N	R13	SYNC_OUT_N	SYNCOUT
INT_N	A4	INT_N	
VPP	A11	VPP	VPP (Sh 3)
OUT_IQ_SEL	T5	OUT_IQ_SEL	
OUT_CLK	K2	R10 130	TP15
LOOP	P8	LOOP	

E6
TP10
TP14

J1C
168-CONN-AMP-RA-TH

OUT_B_17	85	SIGOUT[31]	
OUT_B_16	86	SIGOUT[30]	
OUT_B_15	87	SIGOUT[29]	
OUT_B_14	88	SIGOUT[28]	
OUT_B_13	89	SIGOUT[27]	
OUT_B_12	90	SIGOUT[26]	
OUT_B_11	91	SIGOUT[25]	
OUT_B_10	92	SIGOUT[24]	
OUT_B_9	93	SIGOUT[23]	
OUT_B_8	94	SIGOUT[22]	
OUT_B_7	95	SIGOUT[21]	
OUT_B_6	96	SIGOUT[20]	
OUT_B_5	97	SIGOUT[19]	
OUT_B_4	98	SIGOUT[18]	
OUT_B_3	99	SIGOUT[17]	
OUT_B_2	100	SIGOUT[16]	
OUT_A_17	101	SIGOUT[15]	
OUT_A_16	102	SIGOUT[14]	
OUT_A_15	103	SIGOUT[13]	
OUT_A_14	104	SIGOUT[12]	
OUT_A_13	105	SIGOUT[11]	
OUT_A_12	106	SIGOUT[10]	
OUT_A_11	107	SIGOUT[9]	
OUT_A_10	108	SIGOUT[8]	
OUT_A_9	109	SIGOUT[7]	
OUT_A_8	110	SIGOUT[6]	
OUT_A_7	111	SIGOUT[5]	
OUT_A_6	112	SIGOUT[4]	
OUT_A_5	113	SIGOUT[3]	
OUT_A_4	114	SIGOUT[2]	
OUT_A_3	115	SIGOUT[1]	
OUT_A_2	116	SIGOUT[0]	
	117	GND	
	118	CLKOUT+	
	119	CLKOUT-	
	120	GND	
SYNCOUT	121	SYNCOUT+	(Sh 2) SYNCOUT
	122	SYNCOUT-	
	123	SP5	
	124	SP6	
	125	SP7	
	126	SP8	

J1B
168-CONN-AMP-RA-TH

GND	43		
GND	44		
GND	45		
GND	46		
GND	47		
GND	48		
GND	49		
GND	50		VDUT1
VDUT1	51		
VDUT1	52		
VDUT1	53		
VDUT1	54		
VDUT1	55		
GND	56		
GND	57		
GND	58		
GND	59		
GND	60		
GND	61		
GND	62		
VDUT3	63		
VDUT3	64		
GND	65		
GND	66		
GND	67		
VDUT2	68		
VDUT2	69		
VDUT2	70		
VDUT2	71		
GND	72		
GND	73		
VDUT4	74		
VDUT4	75		
AGND	76		
AGND	77		
EVM-Type4	78		R3 100
EVM-Type3	79		
EVM-Type2	80		
EVM-Type1	81		
EVM-Type0	82		
GND	83		
GND	83		
3P3V	84		

J1D
168-CONN-AMP-RA-TH

GND	168		
D[15]	167	D15	
D[14]	166	D14	
D[13]	165	D13	
D[12]	164	D12	
D[11]	163	D11	
D[10]	162	D10	
D[9]	161	D9	
D[8]	160	D8	
D[7]	159	D7	
D[6]	158	D6	
D[5]	157	D5	
D[4]	156	D4	
D[3]	155	D3	
D[2]	154	D2	
D[1]	153	D1	
D[0]	152	D0	
GND	151		
A[0]	150	A0	
A[1]	149	A1	
A[2]	148	A2	
A[3]	147	A3	
A[4]	146	A4	
A[5]	145	A5	
A[6]	144	A6	
A[7]	143	A7	
A[8]	142		
A[9]	141		
A[10]	140		
GND	139		
CNTLSP	138		
RD#	137		
WR#	136		
CE#	135		
RST#	134		
SCDATA	133		
SCL	132		
GND	131		
TCLK	130	TCLK	
TDO	129	TDO	
TDI	128	TDI	
TMS	127	TMS	

TP4
TP8
TP9
TP11
TP12
E5

U2
SN74ALVTH16374

	1	1 OE	
SEL	2	1Q1	
	3	1Q2	
	4	GND	
	5	1Q3	
	6	1Q4	
	7	VCC	
	8	1Q5	
	9	1Q6	
	10	GND	
	11	1Q7	
	12	1Q8	
	13	2Q1	
	14	2Q2	
	15	GND	
	16	2Q3	
	17	2Q4	
	18	VCC	
	19	2Q5	
	20	2Q6	
	21	GND	
	22	2Q7	
	23	2Q8	
	24	2 OE	
	48	1CLK	
D0	47	1D1	
D1	46	1D2	
	45	GND	
D2	44	1D3	
D3	43	1D4	
	42	VCC	
D4	41	1D5	
D5	40	1D6	
	39	GND	
D6	38	1D7	
D7	37	1D8	
D8	36	2D1	
D9	35	2D2	
	34	GND	
D10	33	2D3	
D11	32	2D4	
	31	VCC	
D12	30	2D5	
D13	29	2D6	
	28	GND	
D14	27	2D7	
D15	26	2D8	
	25	2CLK	

C38 .1uF
C39 .1uF
C42 .1uF
C43 .1uF
C64 .01uF (Note 1)
C44 .1uF
C45 .1uF

U3A SN74LVC08A(PW)
U3B SN74LVC08A(PW)
U3C SN74LVC08A(PW)
U3D SN74LVC08A(PW)
U4 SN74LVC1G04

D(0..15)
A8
CE_N
WR_N

NOTE 1. PART NOT INSTALLED

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Title: GC1115			
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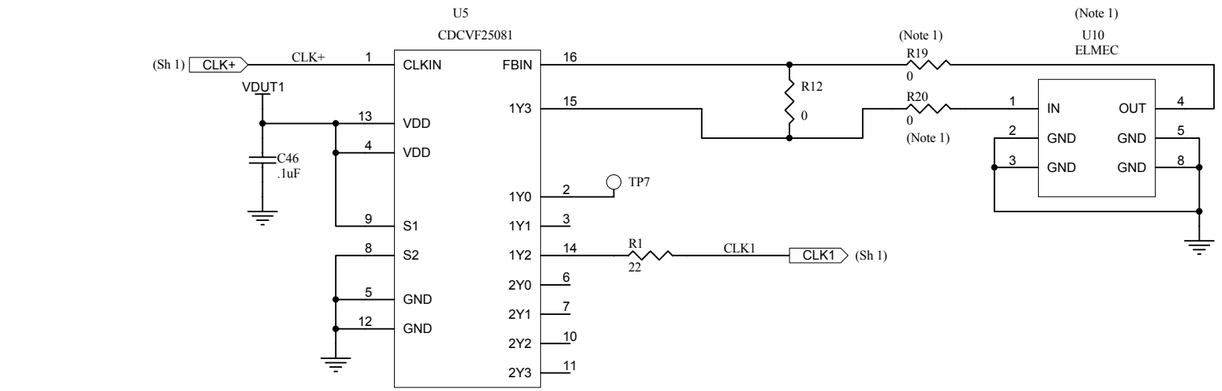

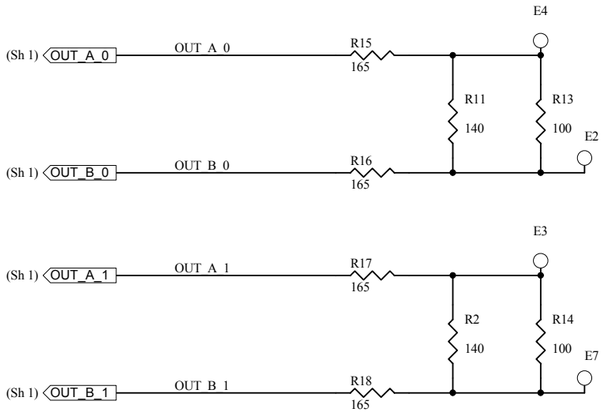

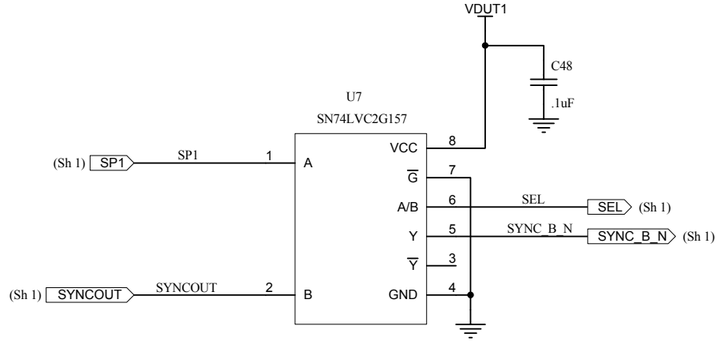

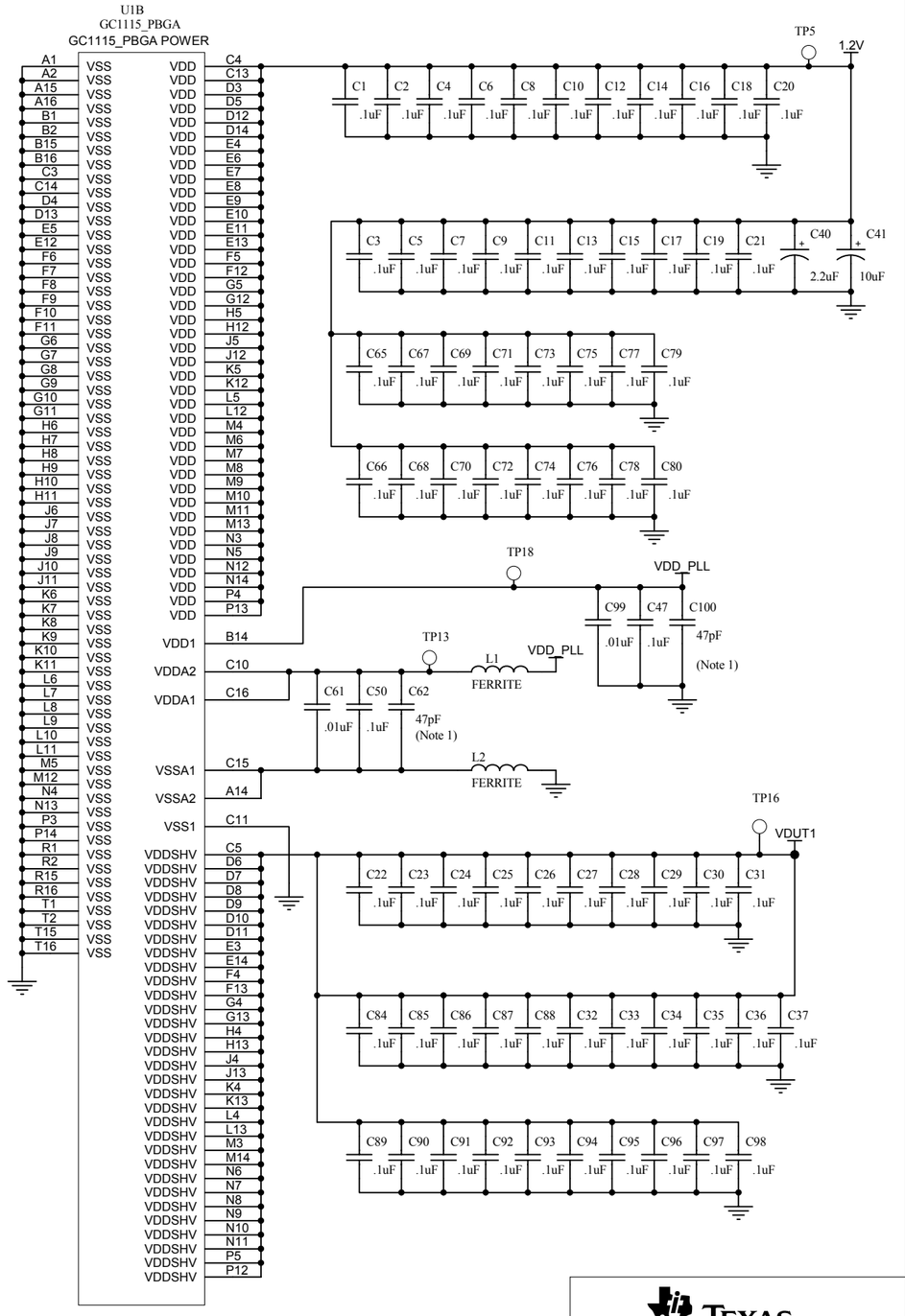

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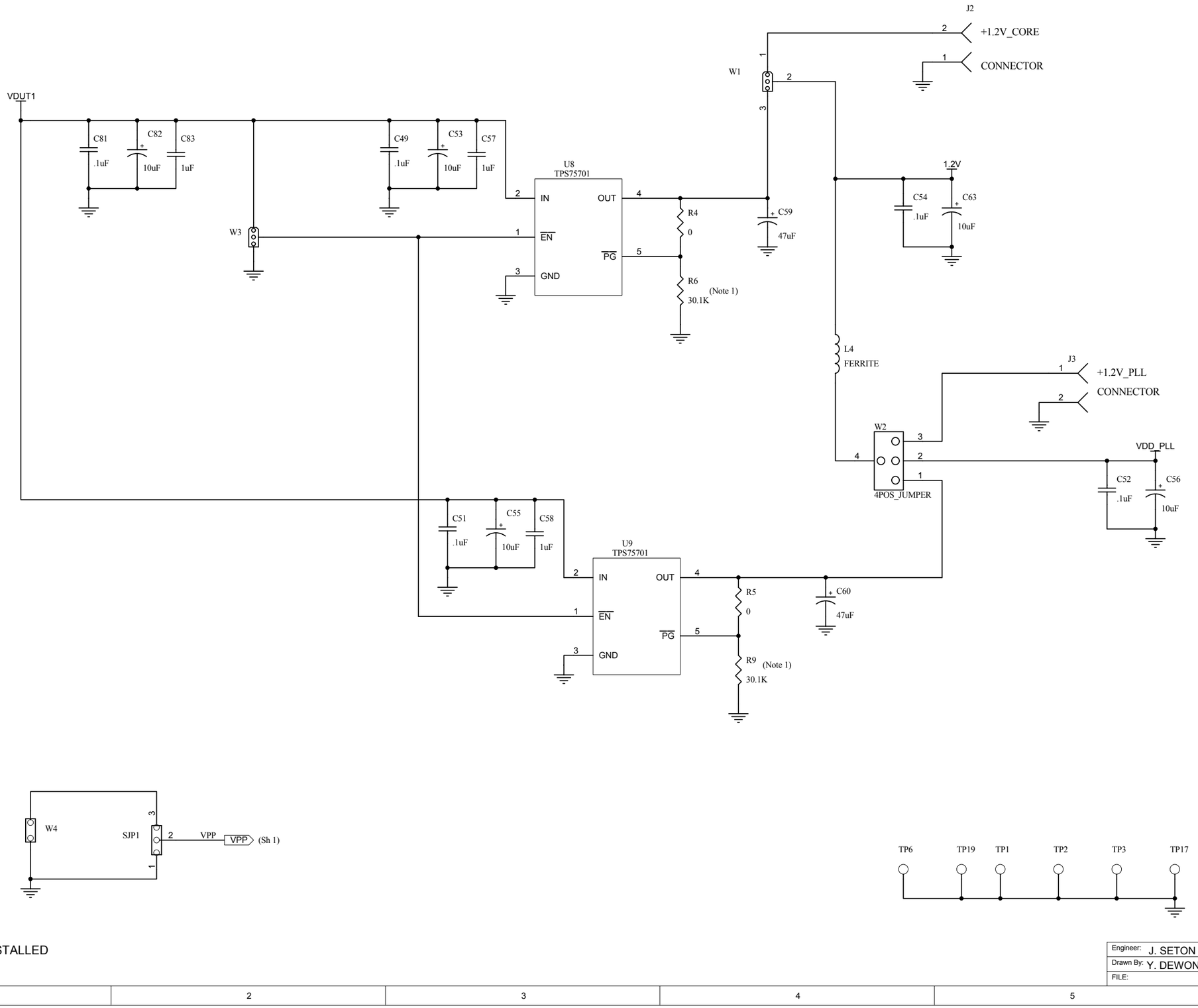

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