CS51033

Fast P-Ch FET Buck Controller

The CS51033 is a switching controller for use in DC−DC converters. It can be used in the buck topology with a minimum number of external components. The CS51033 consists of a 1.0 A power driver for controlling the gate of a discrete P−Channel transistor, fixed frequency oscillator, short circuit protection timer, programmable Soft−Start, precision reference, fast output voltage monitoring comparator, and output stage driver logic with latch.

The high frequency oscillator allows the use of small inductors and output capacitors, minimizing PC board area and systems cost. The programmable Soft−Start reduces current surges at start up. The short circuit protection timer significantly reduces the P−Ch FET duty cycle to approximately 1/30 of its normal cycle during short circuit conditions.

Features

- 1.0 A Totem Pole Output Driver
- High Speed Oscillator (700 kHz max)
- No Stability Compensation Required
- Lossless Short Circuit Protection
- 2.0% Precision Reference
- Programmable Soft−Start
- Wide Ambient Temperature Range:
  - Industrial Grade: −40°C to 85°C
  - Commercial Grade: 0°C to 70°C
- Pb−Free Packages are Available

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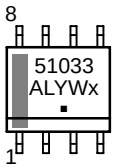
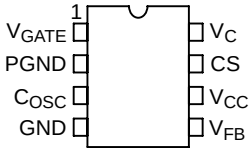
SOIC−8
D SUFFIX
CASE 751

MARKING DIAGRAM



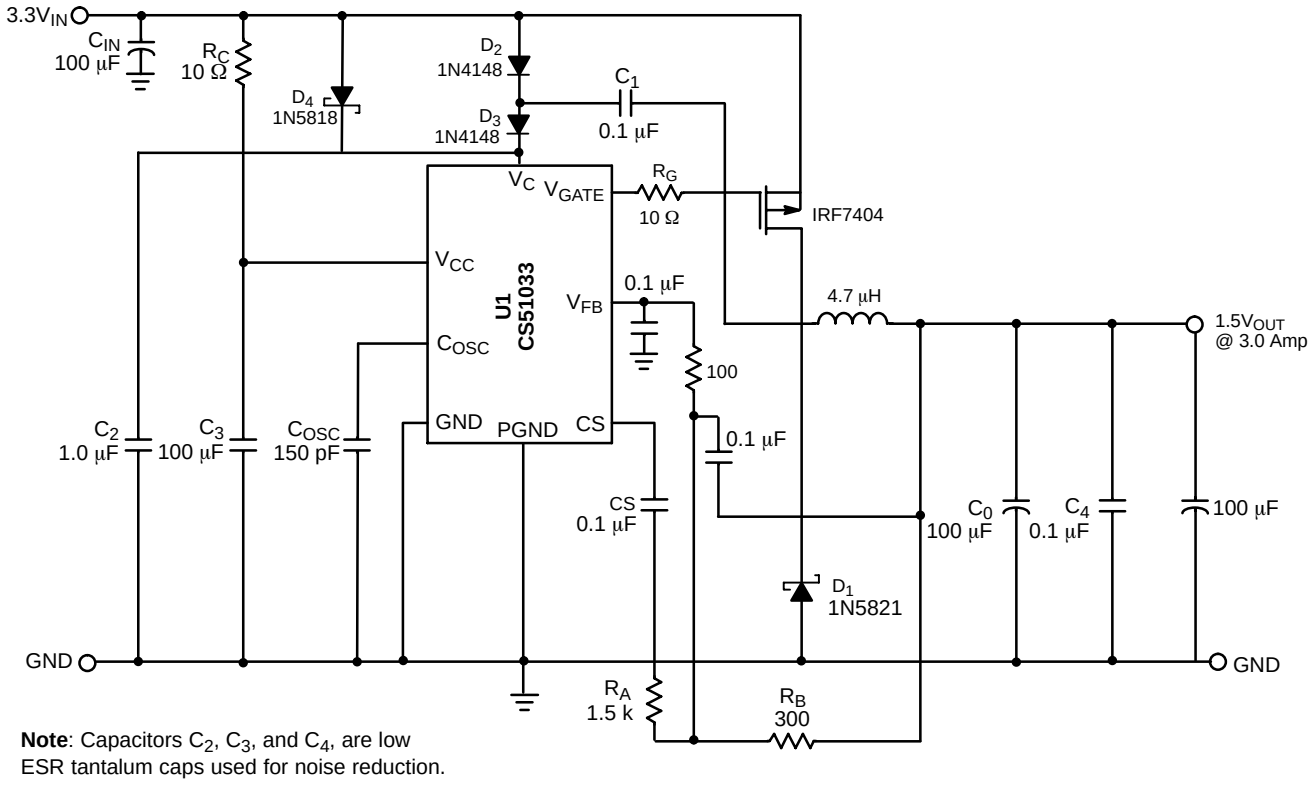
51033	= Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
x	= Continuation of Device Code x = Y or G
▪	= Pb−Free Package

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.



Note: Capacitors C_2, C_3, and C_4, are low ESR tantalum caps used for noise reduction.

Figure 1. Typical Application Diagram

MAXIMUM RATINGS

Rating		Value	Unit
Power Supply Voltage, V_{CC}		5.0	V
Driver Supply Voltage, V_C		20	V
Driver Output Voltage, V_{GATE}		20	V
C_{OSC}, CS, V_{FB} (Logic Pins)		5.0	V
Peak Output Current		1.0	A
Steady State Output Current		200	mA
Operating Junction Temperature, T_J		150	°C
Storage Temperature Range, T_S		−65 to 150	°C
ESD (Human Body Model)		2.0	kV
Package Thermal Resistance,	Junction−to−Case, $R_{\theta JC}$ Junction−to−Ambient, $R_{\theta JA}$	45 165	°C/W °C/W
Lead Temperature Soldering:	Reflow (SMD styles only) (Note 1)	230 peak	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. 60 sec. max above 183°C.

ELECTRICAL CHARACTERISTICS (Specifications apply for $3.135 \le V_{CC} \le 3.465$, $3.0\ V \le V_C \le 16\ V$; Industrial Grade: $-40°C < T_A < 85°C$; $-40°C < T_J < 125°C$: Commercial Grade: $0°C < T_A < 70°C$; $0°C < T_J < 125°C$, unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Oscillator	**V_{FB} = 1.2 V**				
Frequency	C_{OSC} = 470 pF	160	200	240	kHz
Charge Current	1.4 V < V_{COSC} < 2.0 V	−	110	−	μA
Discharge Current	2.7 V > V_{COSC} > 2.0 V	−	660	−	μA
Maximum Duty Cycle	1 − (t_{OFF}/t_{ON})	80.0	83.3	−	%
Short Circuit Timer	**V_{FB} = 1.0 V; CS = 0.1 μF; V_{COSC} = 2.0 V**				
Charge Current	1.0 V < V_{CS} < 2.0 V	175	264	325	μA
Fast Discharge Current	2.55 V > V_{CS} > 2.4 V	40	66	80	μA
Slow Discharge Current	2.4 V > V_{CS} > 1.5 V	4.0	6.0	10	μA
Start Fault Inhibit Time	−	0.70	0.85	1.40	ms
Valid Fault Time	2.6 V > V_{CS} > 2.4 V	0.2	0.3	0.45	ms
GATE Inhibit Time	2.4 V > V_{CS} > 1.5 V	9.0	15	23	ms
Duty Cycle	−	2.5	3.1	4.6	%
CS Comparator	**V_{FB} = 1.0 V**				
Fault Enable CS Voltage	−	−	2.5	−	V
Max CS Voltage	V_{FB} = 1.5 V	−	2.6	−	V
Fault Detect Voltage	V_{CS} when GATE goes high	−	2.4	−	V
Fault Inhibit Voltage	Minimum V_{CS}	−	1.5	−	V
Hold Off Release Voltage	V_{FB} = 0 V	0.4	0.7	1.0	V
Regulator Threshold Voltage Clamp	V_{CS} = 1.5 V	0.725	0.866	1.035	V
V_{FB} Comparators	**V_{COSC} = V_{CS} = 2.0 V**				
Regulator Threshold Voltage	T_J = 25°C (Note 2) T_J = −40 to 125°C	1.225 1.210	1.250 1.250	1.275 1.290	V V
Fault Threshold Voltage	T_J = 25°C (Note 2) T_J = −40 to 125°C	1.12 1.10	1.15 1.15	1.17 1.19	V V
Threshold Line Regulation	$3.135\ V \le V_{CC} \le 3.465$	−	6.0	15	mV
Input Bias Current	V_{FB} = 0 V	−	1.0	4.0	μA
Voltage Tracking	(Regulator Threshold − Fault Threshold Voltage)	70	100	120	mV
Input Hysteresis Voltage	−	−	4.0	20	mV
Power Stage	**V_C = 10 V; V_{FB} = 1.2 V**				
GATE DC Low Saturation Voltage	V_{COSC} = 1.0 V; 200 mA Sink	−	1.2	1.5	V
GATE DC High Saturation Voltage	V_{COSC} = 2.7 V; 200 mA Source; V_C = V_{GATE}	−	1.5	2.1	V
Rise Time	C_{GATE} = 1.0 nF; 1.5 V < V_{GATE} < 9.0 V	−	25	60	ns
Fall Time	C_{GATE} = 1.0 nF; 9.0 V > V_{GATE} > 1.5 V	−	25	60	ns
Current Drain					
I_{CC}	3.135 V < V_{CC} < 3.465 V, Gate switching	−	3.5	6.0	mA
I_C	3.0 V < V_C < 16 V, Gate non−switching	−	2.7	4.0	mA

2. Guaranteed by design, not 100% tested in production.

PACKAGE PIN DESCRIPTION

Pin Number	Pin Symbol	Function
1	V_{GATE}	Driver pin to gate of external P−Ch FET.
2	PGND	Output power stage ground connection.
3	C_{OSC}	Oscillator frequency programming capacitor.
4	GND	Logic ground.
5	V_{FB}	Feedback voltage input.
6	V_{CC}	Logic supply voltage.
7	CS	Soft−Start and fault timing capacitor.
8	V_C	Driver supply voltage.

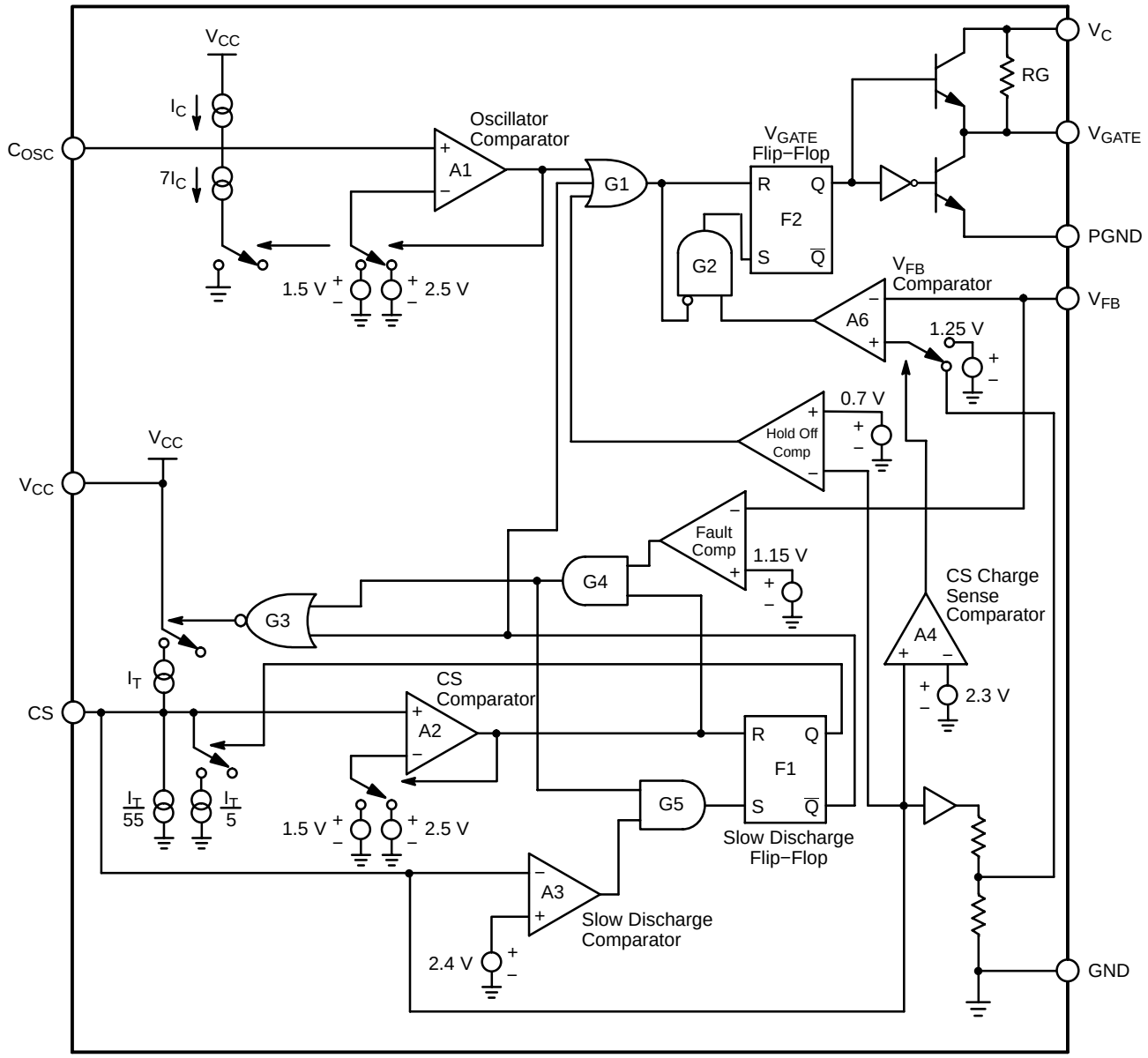


Figure 2. Block Diagram

CIRCUIT DESCRIPTION

THEORY OF OPERATION

Control Scheme

The CS51033 monitors the output voltage to determine when to turn on the P−Ch FET. If V_{FB} falls below the internal reference voltage of 1.25 V during the oscillator's charge cycle, the P−Ch FET is turned on and remains on for the duration of the charge time. The P−Ch FET gets turned off and remains off during the oscillator's discharge cycle time with the maximum duty cycle to 80%. It requires 7.0 mV typical, and 20 mV maximum ripple on the V_{FB} pin to operate. This method of control does not require any loop stability compensation.

Startup

The CS51033 has an externally programmable Soft−Start feature that allows the output voltage to come up slowly, preventing voltage overshoot on the output.

At startup, the voltage on all pins is zero. As V_{CC} rises, the V_C voltage along with the internal resistor R_G keeps the P−Ch FET off. As V_{CC} and V_C continue to rise, the oscillator capacitor (C_{OSC}) and the Soft−Start/Fault Timing capacitor (CS) charges via internal current sources. C_{OSC} gets charged by the current source I_C and CS gets charged by the I_T source combination described by:

$$I_{CS} = I_T - \left(\frac{I_T}{55} + \frac{I_T}{5}\right)$$

The internal Holdoff Comparator ensures that the external P−Ch FET is off until V_{CS} > 0.7 V, preventing the GATE flip−flop (F2) from being set. This allows the oscillator to reach its operating frequency before enabling the drive output. Soft−Start is obtained by clamping the V_{FB} comparator's (A6) reference input to approximately 1/2 of the voltage at the CS pin during startup, permitting the control loop and the output voltage to slowly increase. Once the CS pin charges above the Holdoff Comparator trip point of 0.7 V, the low feedback to the V_{FB} Comparator sets the GATE flip−flop during C_{OSC}'s charge cycle. Once the GATE flip−flop is set, V_{GATE} goes low and turns on the P−Ch FET. When V_{CS} exceeds 2.4 V, the CS charge sense comparator (A4) sets the V_{FB} comparator reference to 1.25 V completing the startup cycle.

Lossless Short Circuit Protection

The CS51033 has "lossless" short circuit protection since there is no current sense resistor required. When the voltage at the CS pin (the fault timing capacitor voltage) reaches 2.5 V, the fault timing circuitry is enabled. During normal operation the CS voltage is 2.6 V. During a short circuit or a transient condition, the output voltage moves lower and the voltage at V_{FB} drops. If V_{FB} drops below 1.15 V, the output of the fault comparator goes high and the CS51033 goes into a fast discharge mode. The fault timing capacitor, CS, discharges to 2.4 V. If the V_{FB} voltage is still below 1.15 V when the CS pin reaches 2.4 V, a valid fault condition has been detected. The slow discharge comparator output goes high and enables gate G5 which sets the slow discharge flip−flop. The V_{GATE} flip−flop resets and the output switch is turned off. The fault timing capacitor is slowly discharged to 1.5 V. The CS51033 then enters a normal startup routine. If the fault is still present when the fault timing capacitor voltage reaches 2.5 V, the fast and slow discharge cycles repeat as shown in Figure 3.

If the V_{FB} voltage is above 1.15 V when CS reaches 2.4 V a fault condition is not detected, normal operation resumes and CS charges back to 2.6 V. This reduces the chance of erroneously detecting a load transient as a fault condition.

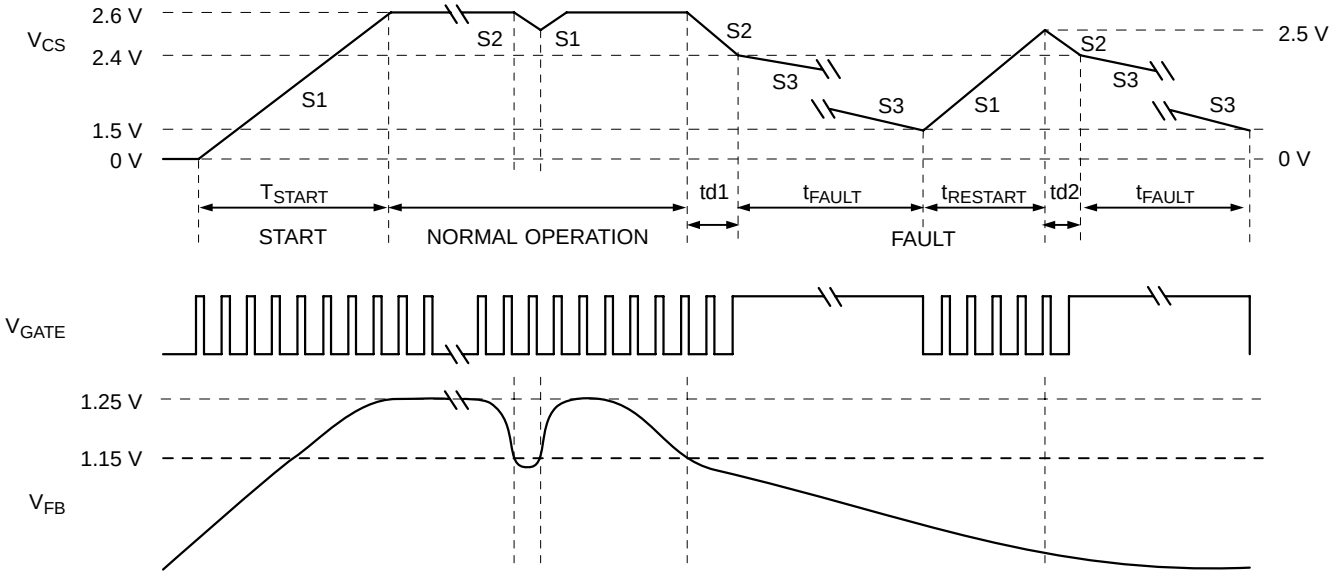


Figure 3. Voltage on Start Capacitor (V_{GS}), the Gate (V_{GATE}), and in the Feedback Loop (V_{FB}), During Startup, Normal and Fault Conditions

Buck Regulator Operation

A block diagram of a typical buck regulator is shown in Figure 4. If we assume that the output transistor is initially off, and the system is in discontinuous operation, the inductor current I_L is zero and the output voltage is at its nominal value. The current drawn by the load is supplied by the output capacitor C_O. When the voltage across C_O drops below the threshold established by the feedback resistors R1 and R2 and the reference voltage V_{REF}, the power transistor Q1 switches on and current flows through the inductor to the output. The inductor current rises at a rate determined by $(V_{IN} - V_{OUT})$/Load. The duty cycle (or "on" time) for the CS51033 is limited to 80%. If output voltage remains higher than nominal during the entire C_{OSC} change time, the Q1 does not turn on, skipping the pulse.

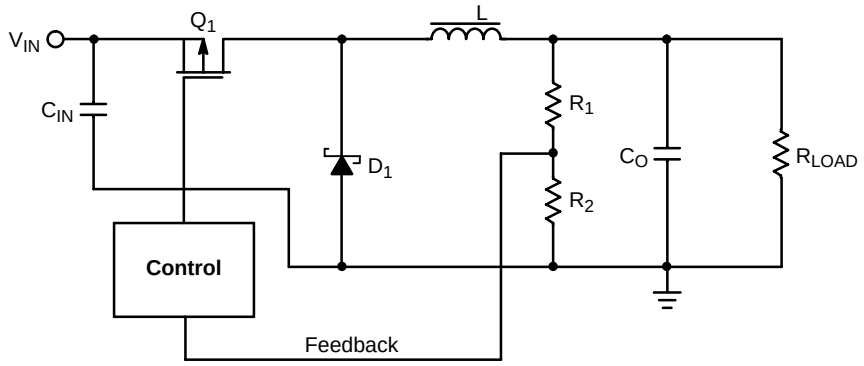


Figure 4. Buck Regulator Block Diagram

Charge Pump Circuit

(Refer to the CS51033 Application Diagram on page 2).

An external charge pump circuit is necessary when the V_C input voltage is below 5.0 V to ensure that there is suffifient gate drive voltage for the external FET. When V_{IN} is applied, capacitors C1 and C2 will be charged to a diodes drop below V_{IN} via diodes D2 and D4, respectively. When the P−Ch FET turns on, it's drain voltage will be approximately equal to V_{IN}. Since the voltage across C1 can not change instantaneously, D2 is reverse biased and the anode voltage rises to approximately 2.0×3.3 V − VD2. C1 transfers some of its stored charge C2 via D3. After several cycles there is sufficient gate drive voltage.

APPLICATIONS INFORMATION

DESIGNING A POWER SUPPLY WITH THE CS51033

Specifications

- V_{IN} = 3.3 V ±10% (i.e. 3.63 V max., 2.97 V min.)
- V_{OUT} = 1.5 V ±2.0%
- I_{OUT} = 0.3 A to 3.0 A
- Output ripple voltage < 33 mV.
- F_{SW} = 200 kHz

1) Duty Cycle Estimates

Since the maximum duty cycle D, of the CS51033 is limited to 80% min., it is best to estimate the duty cycle for the various input conditions to see that the design will work over the complete operating range.

The duty cycle for a buck regulator operating in a continuous conduction mode is given by:

$$D = \frac{V_{OUT} + V_D}{V_{IN} - V_{SAT}}$$

where:

$V_{SAT} = R_{DS(ON)} \times I_{OUT}$ Max.

In this case we can assume that V_D = 0.6 V and V_{SAT} = 0.6 V so the equation reduces to:

$$D = \frac{V_{OUT}}{V_{IN}}$$

From this, the maximum duty cycle D_{MAX} is 53%, this occurs when V_{IN} is at it's minimum while the minimum duty cycle D_{MIN} is 0.35%.

2) Switching Frequency and On and Off Time Calculations

F_{SW} = 200 kHz. The switching frequency is determined by C_{OSC}, whose value is determined by:

$$C_{OSC} = \frac{95}{F_{SW} \times \left(1 - \left(\frac{F_{SW}}{3 \times 10^6}\right) - \left(\frac{30 \times 10^3}{F_{SW}}\right)^2\right)} \cong 470\ pF$$

$$T = \frac{1.0}{F_{SW}} = 5.0\ \mu s$$

$$T_{ON(MAX)} = 5.0\ \mu s \times 0.53 = 2.65\ \mu s$$

$$T_{ON(MIN)} = 5.0\ \mu s \times 0.35 = 1.75\ \mu s$$

$$T_{OFF(MAX)} = 5.0\ \mu s - 0.7\ \mu s = 4.3\ \mu s$$

3) Inductor Selection

Pick the inductor value to maintain continuous mode operation down to 0.3 Amps.

The ripple current $\Delta I = 2 \times I_{OUT(MIN)} = 2 \times 0.3\ A = 0.6\ A$.

$$L_{MIN} = \frac{V_{OUT} + V_D \times T_{OFF(MAX)}}{\Delta I} = \frac{2.1\ V \times 4.3\ \mu s}{0.6\ A} \cong 15\ \mu H$$

The CS51033 will operate with almost any value of inductor. With larger inductors the ripple current is reduced and the regulator will remain in a continuous conduction mode for lower values of load current. A smaller inductor will result in larger ripple current. The core must not saturate with the maximum expected current, here given by:

$$I_{MAX} = \frac{I_{OUT} + \Delta I}{2.0} = 3.0\ A + 0.6\ A/2.0 = 3.3\ A$$

4) Output Capacitor

The output capacitor limits the output ripple voltage. The CS51033 needs a maximum of 15 mV of output ripple for the feedback comparator to change state. If we assume that all the inductor ripple current flows through the output capacitor and that it is an ideal capacitor (i.e. zero ESR), the minimum capacitance needed to limit the output ripple to 50 mV peak−to−peak is given by:

$$C_O = \frac{\Delta I}{8.0 \times F_{SW} \times \Delta V}$$

$$= \frac{0.6\ A}{8.0 \times (200 \times 10^3\ Hz) \times (33 \times 10^{-3}\ V)} \cong 11.4\ \mu F$$

The minimum ESR needed to limit the output voltage ripple to 50 mV peak−to−peak is:

$$ESR = \frac{\Delta V}{\Delta I} = \frac{50 \times 10^{-3}}{0.6\ A} = 55\ m\Omega$$

The output capacitor should be chosen so that its ESR is at least half of the calculated value and the capacitance is at least ten times the calculated value. It is often advisable to use several capacitors in parallel to reduce ESR.

Low impedance aluminum electrolytic, tantalum or organic semiconductor capacitors are a good choice for an output capacitor. Low impedance aluminum are the cheapest but are not available in surface mount at present. Solid tantalum chip capacitors are available from a number of suppliers and offer the best choice for surface mount applications. The capacitor working voltage should be greater than the output voltage in all cases.

5) V_{FB} Divider

$$V_{OUT} = 1.25\ V\left(\frac{R1 + R2}{R2}\right) = 1.25\ V\left(\frac{R1}{R2} + 1.0\right)$$

The input bias current to the comparator is 4.0 μA. The resistor divider current should be considerably higher than this to ensure that there is sufficient bias current. If we choose the divider current to be at least 250 times the bias current this gives a divider current of 1.0 mA and simplifies the calculations.

$$\frac{1.5\ V}{1.0\ mA} = R1 + R2 = 1.5\ k\Omega$$

Let R2 = 1.0 k

Rearranging the divider equation gives:

$$R1 = R2\left(\frac{V_{OUT}}{1.25} - 1.0\right) = 1.0\ k\Omega\left(\frac{1.5\ V}{1.25}\right) = 200\ \Omega$$

6) Divider Bypass Capacitor C_{RR}

Since the feedback resistors divide the output voltage by a factor of 4.0, i.e. 5.0 V/1.25 V= 4.0, it follows that the output ripple is also divided by four. This would require that the output ripple be at least 60 mV (4.0 × 15 mV) to trip the feedback comparator. We use a capacitor C_{RR} to act as an AC short so that the output ripple is not attenuated by the divider network. The ripple voltage frequency is equal to the switching frequency so we choose C_{RR} so that:

$$X_C = \frac{1.0}{2\pi fC}$$

is negligible at the switching frequency.

In this case F_{SW} is 200 kHz if we allow X_C = 3.0 Ω then:

$$C = \frac{1.0}{2\pi f3} \cong 0.265\ \mu F$$

7) Soft−Start and Fault Timing Capacitor CS

CS performs several important functions. First it provides a dead time for load transients so that the IC does not enter a fault mode every time the load changes abruptly. Secondly it disables the fault circuitry during startup, it also provides Soft−Start by clamping the reference voltage during startup to rise slowly and finally it controls the hiccup short circuit protection circuitry. This function reduces the P−Ch FET's duty cycle to 2.0% of the CS period.

The most important consideration in calculating CS is that it's voltage does not reach 2.5 V (the voltage at which the fault detect circuitry is enabled) before V_{FB} reaches 1.15 V otherwise the power supply will never start.

If the V_{FB} pin reaches 1.15 V, the fault timing comparator will discharge CS and the supply will not start. For the V_{FB} voltage to reach 1.15 V the output voltage must be at least 4 × 1.15 = 4.6 V.

If we choose an arbitrary startup time of 200 μs, we calculate the value of CS from:

$$T = \frac{CS \times 2.5\ V}{I_{CHARGE}}$$

$$CS_{(MIN)} = \frac{200\ \mu s \times 264\ \mu A}{2.5\ V} = 0.02\ \mu F$$

Use 0.1 μF.

The fault time out time is the sum of the slow discharge time the fast discharge time and the recharge time and is obviously dominated by the slow discharge time.

The first parameter is the slow discharge time, it is the time for the CS capacitor to discharge from 2.4 V to 1.5 V and is given by:

$$T_{SLOWDISCHARGE} = \frac{CS \times (2.4\ V - 1.5\ V)}{I_{DISCHARGE}}$$

where $I_{DISCHARGE}$ is 6.0 μA typical.

$$T_{SLOWDISCHARGE} = CS \times 1.5\ V \times 10^5$$

The fast discharge time occurs when a fault is first detected. The CS capacitor is discharged from 2.5 V to 2.4 V.

$$T_{FASTDISCHARGE} = \frac{CS \times (2.5\ V - 2.4\ V)}{I_{FASTDISCHARGE}}$$

where $I_{FASTDISCHARGE}$ is 66 μA typical.

$$T_{FASTDISCHARGE} = CS \times 1515$$

The recharge time is the time for CS to charge from 1.5 V to 2.5 V.

$$T_{CHARGE} = \frac{CS \times (2.5\ V - 1.5\ V)}{I_{CHARGE}}$$

where I_{CHARGE} is 264 μA typical.

$$T_{CHARGE} = CS \times 3787$$

The fault time out time is given by:

$$T_{FAULT} = CS \times (3787 + 1515 + 1.5 \times 10^5)$$

$$T_{FAULT} = CS \times (1.55 \times 10^5)$$

For this circuit

$$T_{FAULT} = 0.1 \times 10^{-6} \times 1.55 \times 10^5 = 0.0155$$

A larger value of CS will increase the fault time out time but will also increase the Soft−Start time.

8) Input Capacitor

The input capacitor reduces the peak currents drawn from the input supply and reduces the noise and ripple voltage on the V_{CC} and V_C pins. This capacitor must also ensure that the V_{CC} remains above the UVLO voltage in the event of an output short circuit. C_{IN} should be a low ESR capacitor of at least 100 μF. A ceramic surface mount capacitor should also be connected between V_{CC} and ground to prevent spikes.

9) MOSFET Selection

The CS51033 drives a P−Channel MOSFET. The V_{GATE} pin swings from GND to V_C. The type of P−Ch FET used depends on the operating conditions but for input voltages below 7.0 V a logic level FET should be used.

Choose a P−Ch FET with a continuous drain current (I_D) rating greater than the maximum output current. $R_{DS(ON)}$ should be less than

$$R_{DS} <= \frac{0.6\ V}{I_{OUT(MAX)}} 167\ m\Omega$$

The Gate−to−Source voltage V_{GS} and the Drain−to−Source Breakdown Voltage should be chosen based on the input supply voltage.

The power dissipation due to the conduction losses is given by:

$$P_D = I_{OUT}^2 \times R_{DS(ON)} \times D$$

The power dissipation due to the switching losses is given by:

$$P_D = 0.5 \times V_{IN} \times I_{OUT} \times (T_R{}^r + T_F) \times F_{SW}$$

where T_R = Rise Time and T_F = Fall Time.

10) Diode Selection

The flyback or catch diode should be a Schottky diode because of it's fast switching ability and low forward voltage drop. The current rating must be at least equal to the maximum output current. The breakdown voltage should be at least 20 V for this 12 V application.

The diode power dissipation is given by:

$$P_D = I_{OUT} \times V_D \times (1.0 - D_{MIN})$$

ORDERING INFORMATION

Device	Operating Temperature Range	Package	Shipping†
CS51033YD8	−40°C < T_A < 85°C	SOIC−8	98 Units / Rail
CS51033YD8G		SOIC−8 (Pb−Free)	98 Units / Rail
CS51033YDR8		SOIC−8	2500 Tape & Reel
CS51033YDR8G		SOIC−8 (Pb−Free)	2500 Tape & Reel
CS51033GD8	0°C < T_A < 70°C	SOIC−8	98 Units / Rail
CS51033GD8G		SOIC−8 (Pb−Free)	98 Units / Rail
CS51033GDR8		SOIC−8	2500 Tape & Reel
CS51033GDR8G		SOIC−8 (Pb−Free)	2500 Tape & Reel

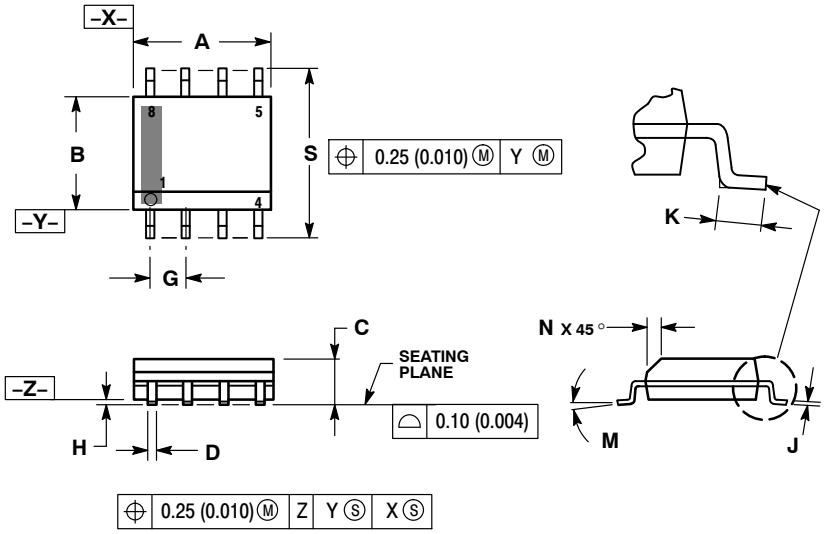
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

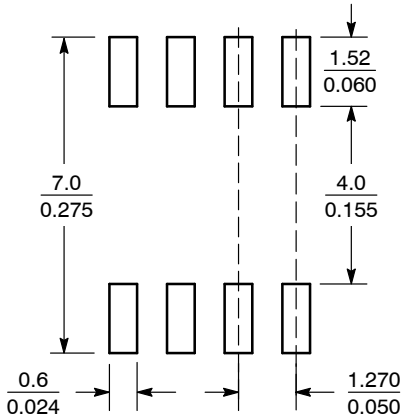
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

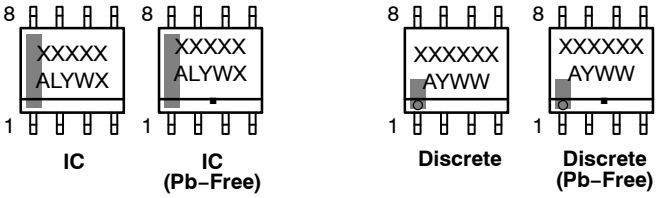
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC | **IC (Pb−Free)** | **Discrete** | **Discrete (Pb−Free)**

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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DESCRIPTION:	**SOIC−8 NB**		**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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