



-48V Hot-Swap Controllers with External RSENSE

MAX5948A/MAX5948B

General Description

The MAX5948A/MAX5948B are hot-swap controllers that allow a circuit card to be safely hot plugged into a live backplane. The MAX5948A/MAX5948B operate from -20V to -80V and are well-suited for -48V power systems. The MAX5948A is pin- and function-compatible with both the LT1640AL and LT1640L. The MAX5948B is pin- and function-compatible with both the LT1640AH and LT1640H.

The MAX5948A/MAX5948B provide a controlled turn-on to circuit cards preventing glitches on the power-supply rail and damage to board connectors and components. The MAX5948A/MAX5948B provide undervoltage, over-voltage, and overcurrent protection. These devices ensure the input voltage is stable and within tolerance before applying power to the load.

Both the MAX5948A and MAX5948B protect a system against overcurrent and short-circuit conditions by turning off the external MOSFET in the event of a fault condition.

Both devices feature an open-drain power-good status output, $\overline{\text{PWRGD}}$ for MAX5948A or PWRGD for MAX5948B, that can be used to enable downstream converters.

The MAX5948A/MAX5948B are available in an 8-pin SO package. Both devices are specified for the extended -40°C to +85°C temperature range.

Applications

Central-Office Switching
Network Switches/Routers
Server Line Cards
Base-Station Line Cards

Features

- ◆ Allow Safe Board Insertion and Removal from a Live -48V Backplane
- ◆ Pin- and Function-Compatible with LT1640AL/LT1640L (MAX5948A)
- ◆ Pin- and Function-Compatible with LT1640AH/LT1640H (MAX5948B)
- ◆ Withstand -100V Input Transients with No External Components
- ◆ Operate from -20V to -80V
- ◆ Programmable Inrush and Short-Circuit Current Limits
- ◆ Programmable Overvoltage Protection
- ◆ Programmable Undervoltage Lockout
- ◆ Power Up into a Shorted Load
- ◆ Power-Good Control Output

Ordering Information

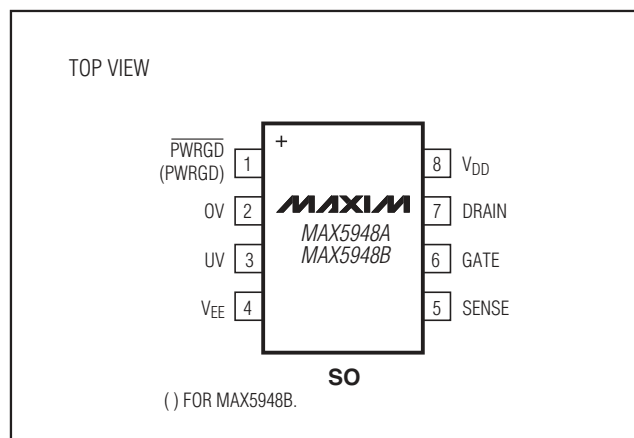
PART	TEMP RANGE	PIN-PACKAGE
MAX5948AESA+	-40°C to +85°C	8 SO
MAX5948BESA+	-40°C to +85°C	8 SO

+Denotes a lead(Pb)-free/RoHS-compliant package.

Selector Guide

PART	PWRGD POLARITY
MAX5948AESA	Active Low ($\overline{\text{PWRGD}}$)
MAX5948BESA	Active High (PWRGD)

Pin Configuration



Typical Operating Circuit appears at end of data sheet.



-48V Hot-Swap Controllers with External RSENSE

ABSOLUTE MAXIMUM RATINGS

(All voltages are referenced to V_{EE} , unless otherwise noted.)

Supply Voltage ($V_{DD} - V_{EE}$)	-0.3V to +100V
PWRGD, \overline{PWRGD}	-0.3V to +100V
DRAIN (Note 1)	-2V to +100V
SENSE	-0.3V to +20V
GATE (internally clamped)	-0.3V to +18V
UV and OV	-0.3V to +60V
Current through SENSE	$\pm 20\text{mA}$
Current into GATE	$\pm 300\text{mA}$

Current into Any Other Pin	$\pm 20\text{mA}$
Current into Drain	-100mA to +20mA
Continuous Power Dissipation ($T_A = +70^\circ\text{C}$)	
8-Pin SO (derate 5.9mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$)	471mW
Operating Temperature Range	-40°C to $+85^\circ\text{C}$
Junction Temperature	$+150^\circ\text{C}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (soldering, 10s)	$+300^\circ\text{C}$
Soldering Temperature (reflow)	$+260^\circ\text{C}$

Note 1: Test condition per Figure 1. DRAIN current must be limited to the specified 100mA maximum.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V_{EE} = 0\text{V}$, $V_{DD} = 48\text{V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$. Typical values are at $T_A = +25^\circ\text{C}$, unless otherwise noted.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
Operating Input Voltage Range	V_{DD}		20		80	V
Supply Current	I_{DD}	$V_{UV} = 3\text{V}$, $OV = V_{EE}$, $SENSE = V_{EE}$		0.7	2	mA
GATE DRIVER AND CLAMPING CIRCUITS						
Gate Pin Pullup Current	I_{PU}	GATE drive on, $V_{GATE} = V_{EE}$	-30	-45	-60	μA
Gate Pin Pulldown Current	I_{PD}	Any fault condition, $V_{GATE} = 2\text{V}$	24	50	70	mA
External Gate Drive	ΔV_{GATE}	$V_{GATE} - V_{EE}$, $20\text{V} \leq V_{DD} \leq 80\text{V}$	10	13.5	18	V
GATE to V_{EE} Clamp Voltage	V_{GSCLMP}	$V_{GATE} - V_{EE}$, current into GATE = 30mA	15	16.4	18	V
CIRCUIT BREAKER						
Current-Limit Trip Voltage	V_{CB}	$V_{CB} = V_{SENSE} - V_{EE}$	40	50	60	mV
SENSE Input Bias Current	I_{SENSE}	$V_{SENSE} = 50\text{mV}$	0	-0.03	-1	μA
UV PIN						
UV High Threshold	V_{UVH}	UV low to high transition	1.213	1.243	1.272	V
UV Low Threshold	V_{UVL}	UV high to low transition	1.198	1.223	1.247	V
UV Hysteresis	V_{UVHY}			20		mV
UV Input Bias Current	I_{INUV}	$V_{UV} = V_{EE}$	0		-0.5	μA
OV PIN						
OV High Threshold	V_{OVH}	OV low to high transition	1.198	1.223	1.247	V
OV Low Threshold	V_{OVL}	OV high to low transition	1.165	1.203	1.232	V
OV Hysteresis	V_{OVHY}			20		mV
OV Input Bias Current	I_{INOV}	$V_{OV} = V_{EE}$	0		-0.5	μA
PWRGD OUTPUT SIGNAL REFERENCED TO DRAIN						
DRAIN Input Bias Current	I_{DRAIN}	$V_{DRAIN} = 48\text{V}$	10	80	250	μA
Power-Good Threshold	V_{PG}	$V_{DRAIN} - V_{EE}$, high to low transition	1.1	1.4	2.0	V
Power-Good Threshold Hysteresis	V_{PGHY}			0.4		V

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MAX5948A/MAX5948B

ELECTRICAL CHARACTERISTICS (continued)

($V_{EE} = 0V$, $V_{DD} = 48V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$. Typical values are at $T_A = +25^{\circ}C$, unless otherwise noted.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PWRGD, \overline{PWRGD} Output Leakage	I_{OH}	$V_{\overline{PWRGD}}$ (MAX5948A) = 80V, $V_{DRAIN} = 48V$, $V_{\overline{PWRGD}}$ (MAX5948B) = 80V, $V_{DRAIN} = 0V$			10	μA
Power-Good Output Impedance (PWRGD to DRAIN)	R_{OUT}	$V_{\overline{PWRGD}}$ (MAX5948B) ($V_{DRAIN} - V_{EE}$) < V_{PG}		500 x 10 ³		$M\Omega$
\overline{PWRGD} Output Low Voltage	V_{OL}	$V_{\overline{PWRGD}} - V_{EE}$; $V_{DRAIN} - V_{EE} < V_{PG}$, $I_{OUT} = 1mA$ (MAX5948A)		0.11	0.4	V
PWRGD Output Low Voltage	V_{OL}	$V_{PWRGD} - V_{DRAIN}$; $V_{DRAIN} = 5V$, $I_{OUT} = 1mA$ (MAX5948B)		0.11	0.4	V
AC PARAMETERS						
OV High to GATE Low	t_{PHLOV}	Figures 2, 3		0.5		μs
UV Low to GATE Low	t_{PHLUV}	Figures 2, 4		0.4		μs
OV Low to GATE High	t_{PLHOV}	Figures 2, 3		3.3		μs
UV High to GATE High	t_{PLHVL}	Figures 2, 4		3.4		μs
SENSE High to GATE Low	$t_{PHLSENSE}$	Figures 2, 5	2	3	4	μs
DRAIN Low to \overline{PWRGD} Low DRAIN Low to (PWRGD - DRAIN) High	t_{PHLPG}	MAX5948A, Figures 2, 6		0.5		μs
		MAX5948B, Figures 2, 6		0.5		
DRAIN High to \overline{PWRGD} High DRAIN High to (PWRGD - DRAIN) Low	t_{PLHPG}	MAX5948A, Figures 2, 6		0.5		μs
		MAX5948B, Figures 2, 6		0.5		

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to V_{EE} , unless otherwise specified.

Note 3: Limits are 100% tested at $T_A = +25^{\circ}C$ and $+85^{\circ}C$. Limits at $-40^{\circ}C$ are guaranteed by design.

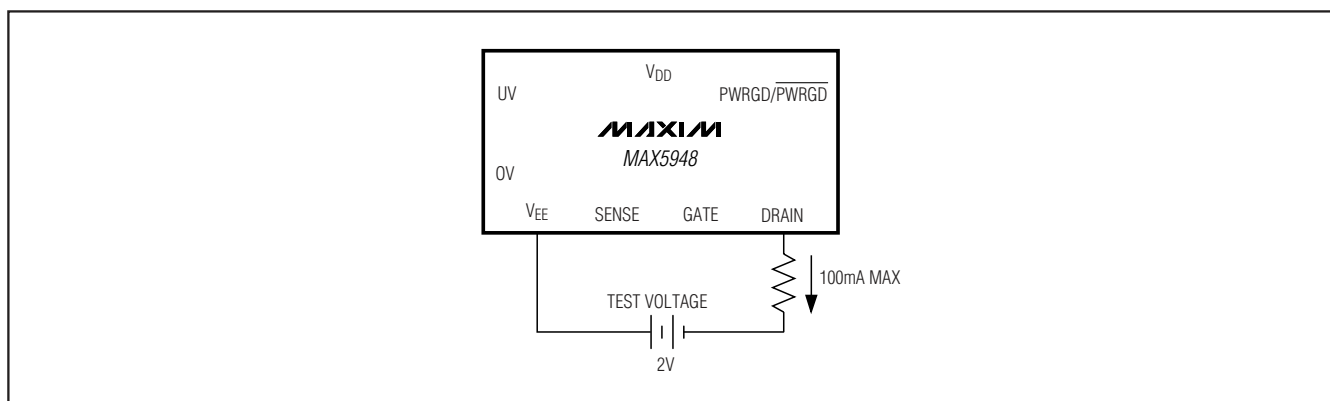
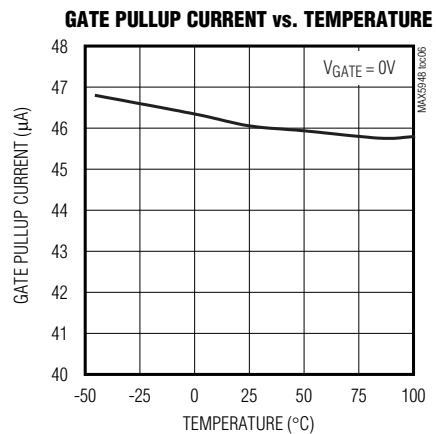
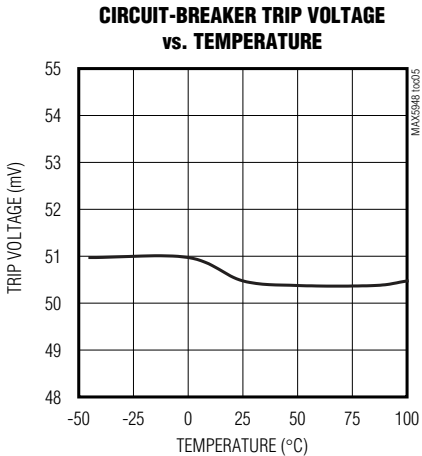
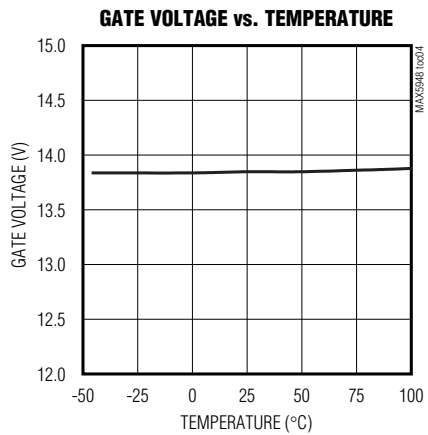
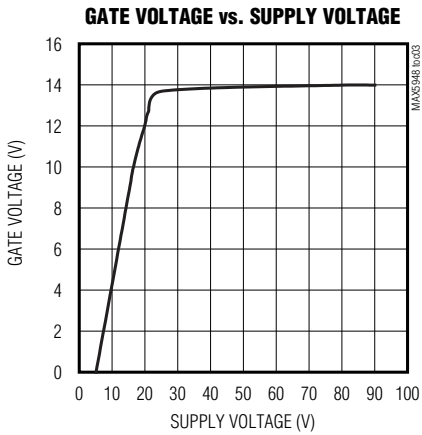
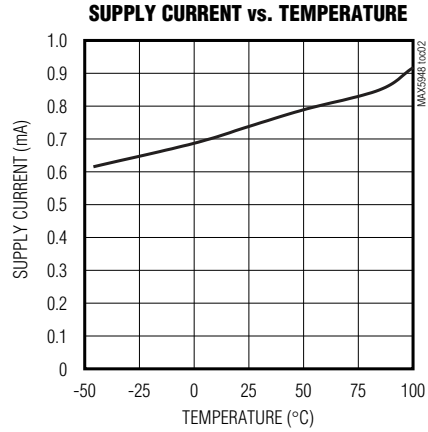
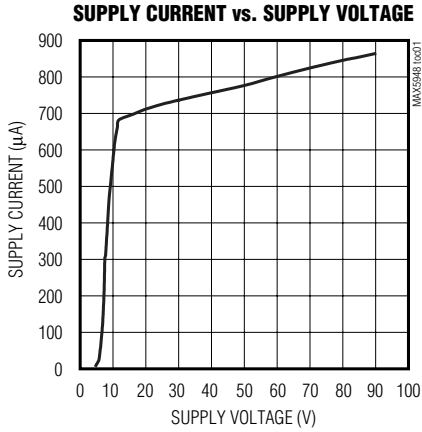


Figure 1. -2V DRAIN Voltage Test Circuit

-48V Hot-Swap Controllers with External RSENSE

Typical Operating Characteristics

(V_{DD} = 48V, V_{EE} = 0V, T_A = +25°C, unless otherwise noted.)



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MAX5948A/MAX5948B

Typical Operating Characteristics (continued)

($V_{DD} = 48V$, $V_{EE} = 0V$, $T_A = +25^\circ C$, unless otherwise noted.)

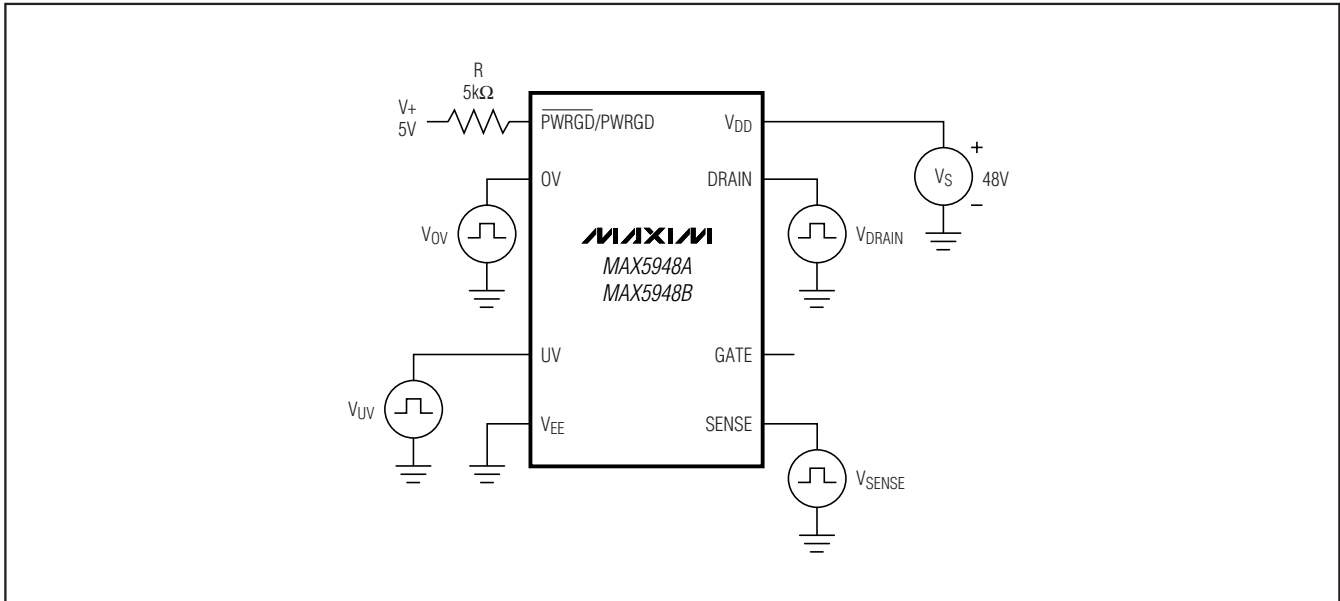
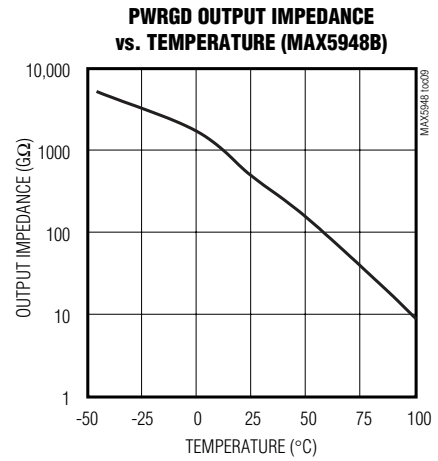
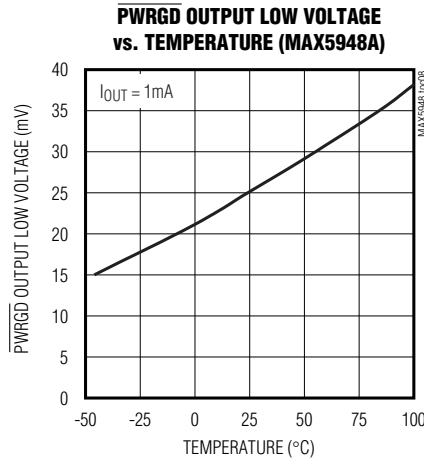
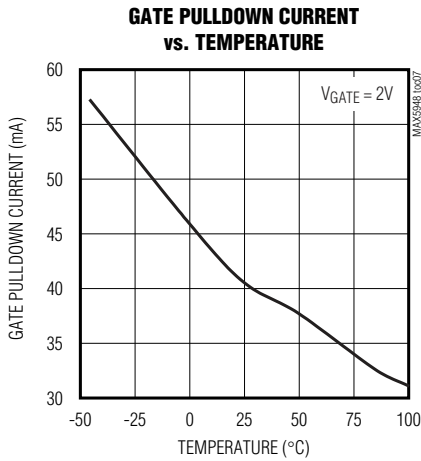


Figure 2. Test Circuit 1

-48V Hot-Swap Controllers with External RSENSE

Timing Diagrams

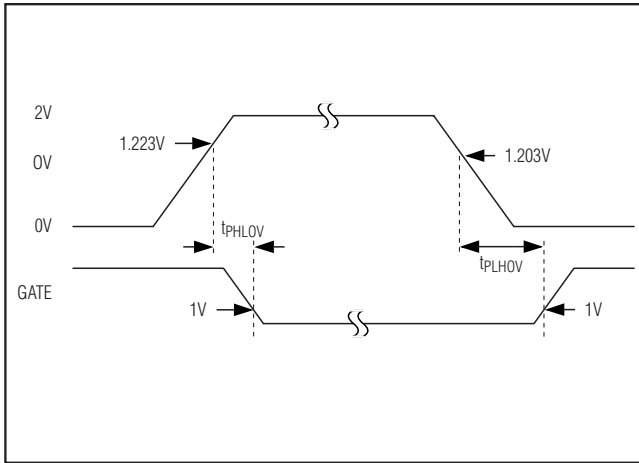


Figure 3. OV to GATE Timing

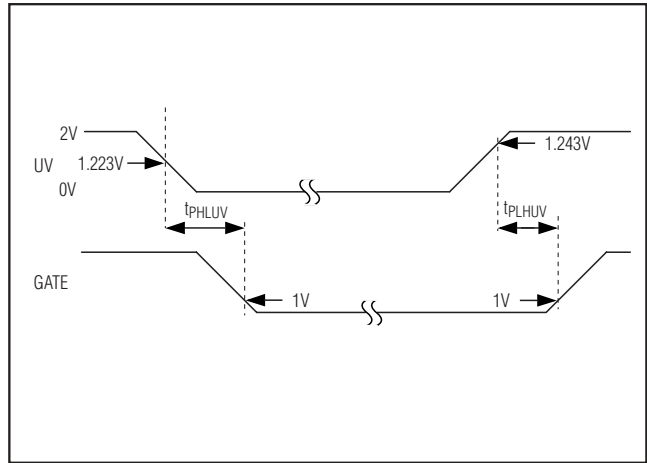


Figure 4. UV to GATE Timing

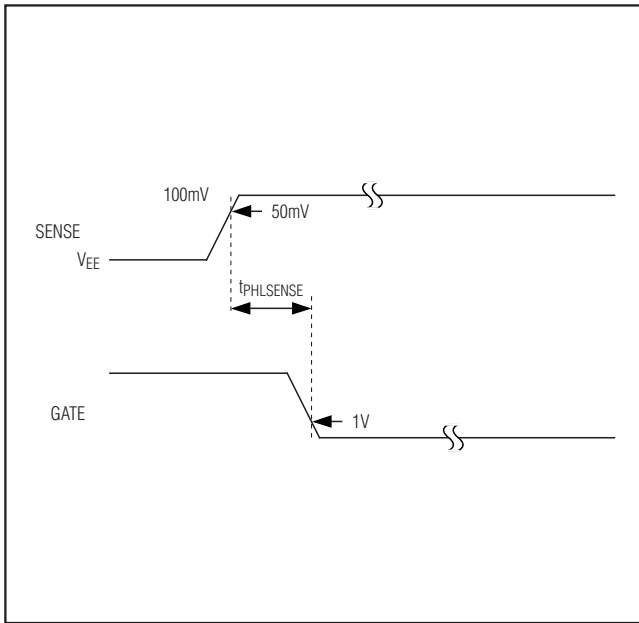


Figure 5. SENSE to GATE Timing

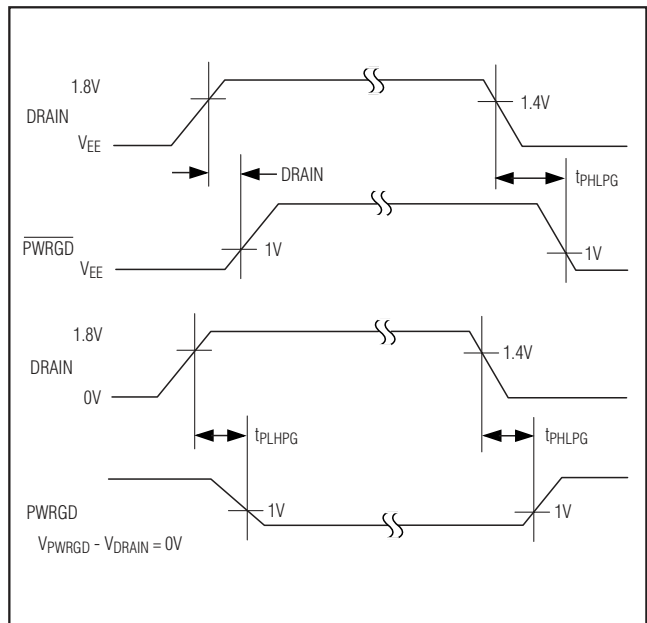


Figure 6. DRAIN to PWRGD/PWRGD Timing

-48V Hot-Swap Controllers with External RSENSE

MAX5948A/MAX5948B

Pin Description

PIN		NAME	FUNCTION
MAX5948A	MAX5948B		
1	—	$\overline{\text{PWRGD}}$	Power-Good Signal Output. $\overline{\text{PWRGD}}$ is an active-low open-drain status output referenced to V_{EE} . $\overline{\text{PWRGD}}$ is low when $V_{\text{DRAIN}} - V_{EE} \leq V_{\text{PG}}$, indicating a power-good condition. $\overline{\text{PWRGD}}$ is open drain otherwise.
—	1	PWRGD	Power-Good Signal Output. PWRGD is an active-high open-drain status output referenced to DRAIN. PWRGD is in a high-impedance state when $V_{\text{DRAIN}} - V_{EE} \leq V_{\text{PG}}$, indicating a power-good condition. PWRGD is pulled low to DRAIN otherwise.
2	2	OV	Input Pin for Overvoltage Detection. OV is referenced to V_{EE} . When OV is pulled above V_{OVH} voltage, the GATE pin is immediately pulled low. The GATE pin remains low until the OV pin voltage reduces to V_{OVL} .
3	3	UV	Input Pin for Undervoltage Detection. UV is referenced to V_{EE} . When UV is pulled above V_{UVH} voltage, the GATE is enabled. When UV is pulled below V_{UVL} , GATE is pulled low. UV is also used to reset the circuit breaker after a fault condition. To reset the circuit breaker, pull UV below V_{UVL} .
4	4	V_{EE}	Device Negative Power-Supply Input. Connect to the negative power-supply rail.
5	5	SENSE	Current-Sense Voltage Input. Connect to an external sense resistor and the external MOSFET source. The voltage drop across the external sense resistor is monitored to detect overcurrent or short-circuit fault conditions. Connect SENSE to V_{EE} to disable the circuit-breaker feature.
6	6	GATE	Gate-Drive Output. Connect to gate of the external n-channel MOSFET.
7	7	DRAIN	Output-Voltage Sense Input. Connect to the output-voltage node (drain of external n-channel MOSFET).
8	8	V_{DD}	Positive Power-Supply Rail Input. This is the power ground in the negative-supply voltage system. Connect to the most positive potential of the power-supply inputs.

Detailed Description

The MAX5948A/MAX5948B are integrated hot-swap controllers for -48V power systems. They allow circuit boards to be safely hot plugged into a live backplane without causing a glitch on the power-supply rail. When circuit boards are inserted into a live backplane, the bypass capacitors at the input of the board's power module or switching power supply can draw large inrush currents as they charge. The inrush currents can cause glitches on the system power-supply rail and damage components on the board.

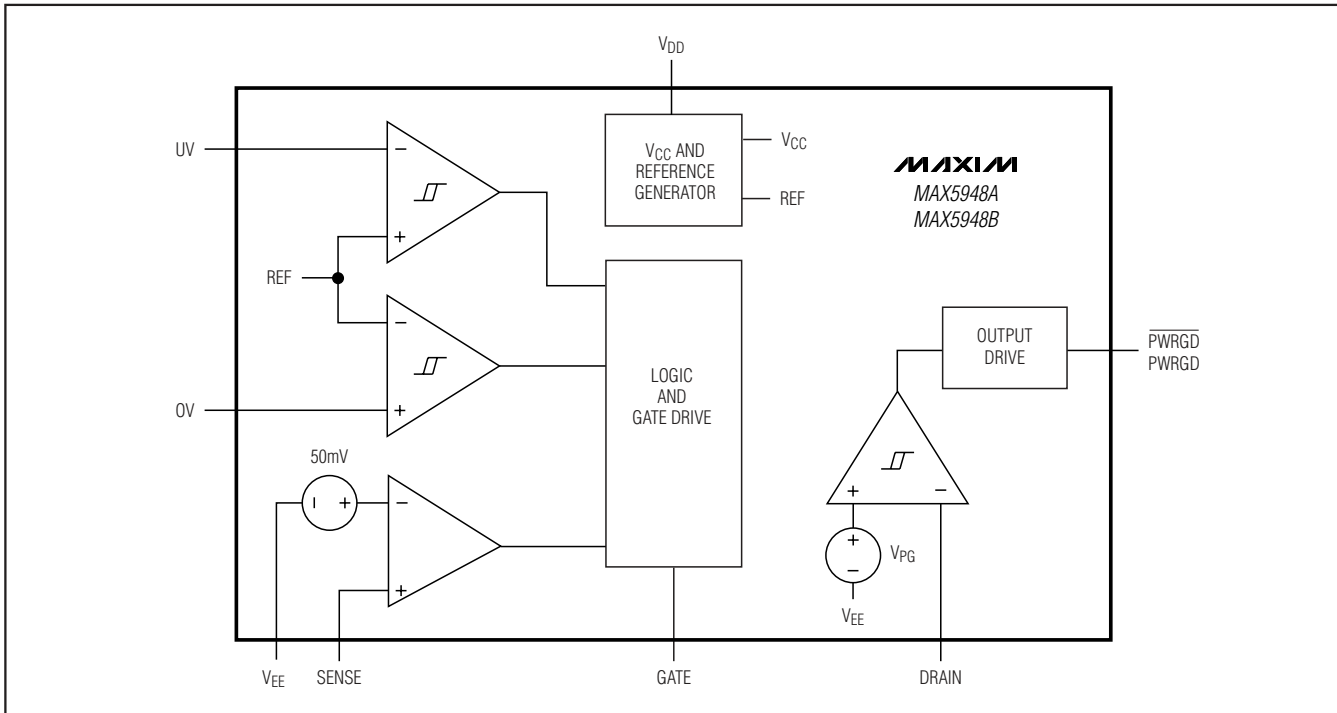
The MAX5948A/MAX5948B provide a controlled turn-on to circuit cards preventing glitches on the power-supply rail and damage to board connectors and components. Both the MAX5948A and MAX5948B provide undervoltage, overvoltage, and overcurrent protection. The MAX5948A/MAX5948B ensure the input voltage is stable and within tolerance before applying power to the load.

Board Insertion

Figure 6a shows a typical hot-swap circuit for -48V systems. When the circuit board first makes contact with the backplane, the DRAIN to GATE capacitance (C_{gd}) of Q1 pulls up the GATE voltage to roughly $I(V_{EE} \times C_{\text{gd}}) / (C_{\text{gd}} + C_{\text{gs}})I$. The MAX5948_ features an internal dynamic clamp between GATE and V_{EE} to keep the gate-to-source voltage of Q1 low during hot insertion, preventing Q1 from passing an uncontrolled current to the load. For most applications, the internal clamp between GATE and V_{EE} of the MAX5948A/MAX5948B eliminates the need for an external gate-to-source capacitor. Resistor R3 limits the current into the clamp circuitry during card insertion.

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Block Diagram



Power-Supply Ramping

The MAX5948A/MAX5948B can reside either on the backplane or the removable circuit board (Figure 6a). Power is delivered to the load by placing an external n-channel MOSFET pass transistor in the power-supply path.

After the circuit board is inserted into the backplane and the supply voltage at VEE is stable and within the under-voltage and overvoltage tolerance, the MAX5948A/MAX5948B turn on Q1. The MAX5948A/MAX5948B gradually turn on the external MOSFET by charging the gate of Q1 with a 45µA current source. Capacitor C2 provides a feedback signal to accurately limit the inrush current. The inrush current can be calculated:

$$I_{\text{INRUSH}} = (I_{\text{PU}} \times C_L) / C_2$$

where C_L is the total load capacitance, $C_3 + C_4$, and I_{PU} is the MAX5948_ gate pullup current.

Figure 6b shows the inrush current waveform. The current through C2 controls the GATE voltage. At the end of the DRAIN ramp, the GATE voltage is charged to its final value. The GATE-to-SENSE clamp limits the maximum V_{GS} to about 18V under any condition.

Board Removal

If the card is removed from a live backplane, the output capacitor on the card may not be immediately discharged. While the output capacitor is discharging, the MAX5948_ continues to operate as if the input supply were still connected because the output capacitor temporarily supplies operating current to the IC. If the circuit is connected as in Figure 7a, the voltage at the UV pin falls below the UVLO detect threshold, and the MAX5948_ turns off the external MOSFET. If R4 in the circuit is connected directly to the -48V return, the external MOSFET remains on until the capacitor is discharged sufficiently to drop the UV pin voltage to the UVLO detect threshold.

In either case, when the MOSFET is turned off, the output capacitor continues to discharge by the IC supply current I_{DD} . The I_{DD} flows into the IC at the VDD terminal, out at the VEE terminal, and back to the capacitor through the substrate diode of the external MOSFET. There is also a parallel current path between the VEE and DRAIN terminals through multiple internal ESD-protection diodes. The protection circuit built into the IC allows the DRAIN terminal voltage to drop below that of the VEE terminal so long as the absolute maximum allowed DRAIN terminal current (-100mA) is not exceeded. As I_{DD} is only 2mA maximum, this limiting current will not even be approached.

-48V Hot-Swap Controllers with External RSENSE

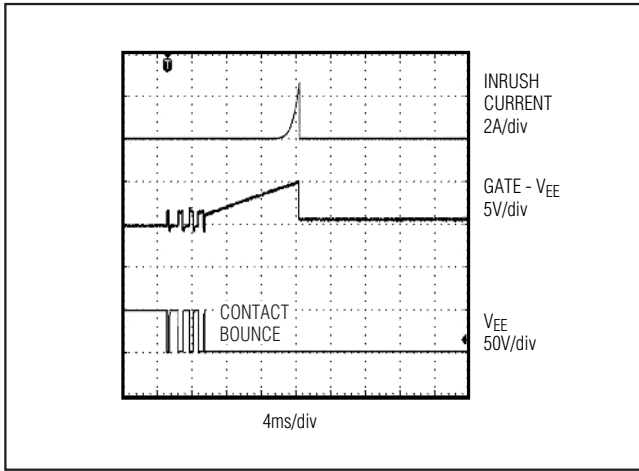


Figure 8. Startup Into a Short Circuit

If more than 3μs (typ) deglitch time (tPHLSENSE) is needed to prevent spurious shutdown due to load current spikes or noise, a simple lowpass filter can be used between the SENSE and VEE pins as shown in Figure 9. Resistor R7 and capacitor C3 slow down the response of the circuit breaker to filter momentary glitches in the SENSE voltage. The additional delay time can be estimated with the following equation:

$$t_{cb\,dly} = R7 \times C3 \times \ln\left(\frac{V_f - V_l}{V_f - V_{CB}}\right)$$

$$= R7 \times C3 \times \ln\left(\frac{I_f - I_l}{I_f - I_{CB}}\right)$$

where I_f is the current in fault condition, I_l is the initial current before the fault, and I_{CB} is the circuit-breaker trip current ($I_{CB} = V_{CB}/R1$). Alternatively, the corresponding voltages across the sense resistor (V_f , V_l , and V_{CB}) may be used in the equation as shown. The SENSE pin of the MAX5948A/MAX5948B sources very little current (0.02μA typ), so the addition of resistor R7 will introduce very little error in the circuit-breaker trip voltage. For example, a 10kΩ resistor for R7 will only cause a 200μV offset.

Example: A system has a 1A nominal load current and a 20mΩ sense resistor. The circuit-breaker delay needs to be increased to 50μs in response to a load current step to 5A. The circuit-breaker trip current is 50mV/20mΩ = 2.5A. Solving for R7 x C3 in the equation above yields a desired time constant of 100μs. This can be achieved with R7 = 100Ω and C3 = 1μF.

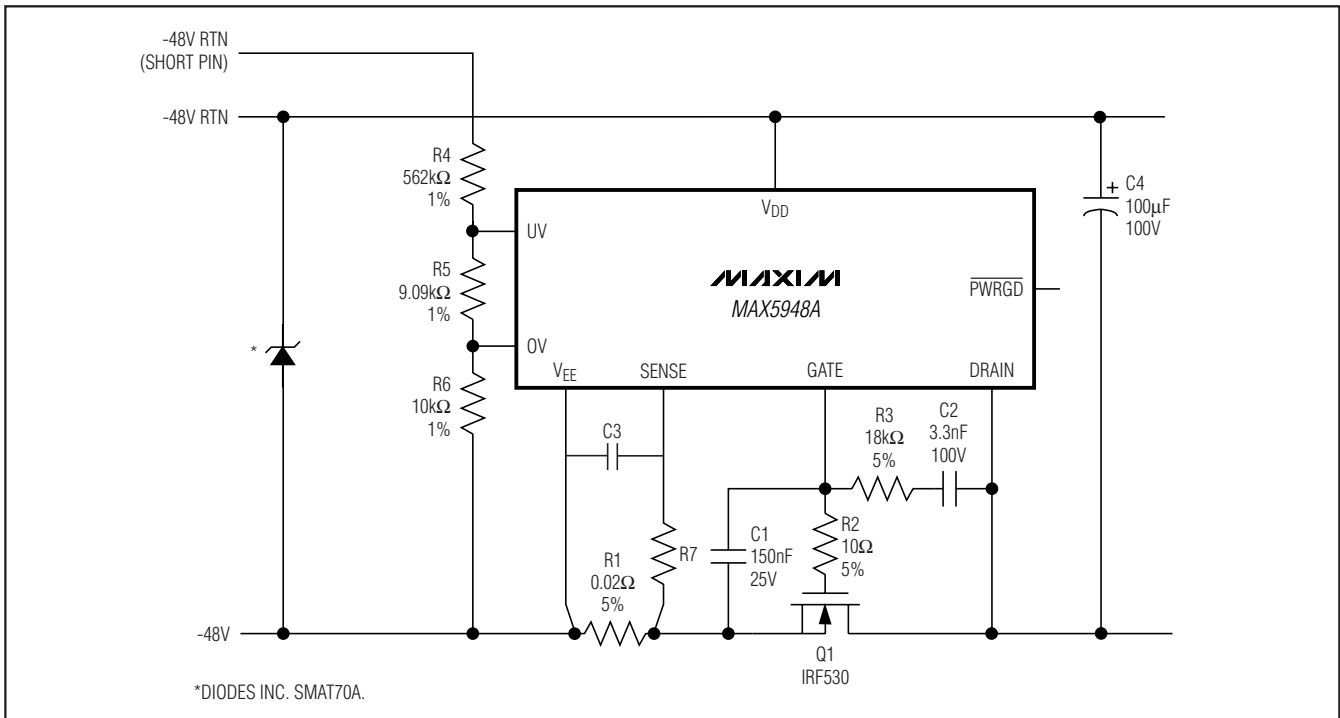


Figure 9. Extending the Short-Circuit Protection Delay

-48V Hot-Swap Controllers with External RSENSE

Figure 11a shows how to program the undervoltage and overvoltage trip thresholds using three resistors. With $R4 = 562k\Omega$, $R5 = 9.09k\Omega$, and $R6 = 10k\Omega$, the undervoltage threshold is set to 37.2V (with a 37.8V release from undervoltage) and the overvoltage is set to 71.1V (with a 69.9V release from overvoltage).

More hysteresis can be added to the undervoltage lockout with the circuit shown in Figure 11b. Resistor R3 connected between GATE and UV lowers the supply undervoltage lockout threshold (supply voltage decreasing) to:

$$V_{UV,HL} = V_{UVL} \left(\frac{R2 \times R3 + R1 \times R3 + R1 \times R2}{R2 \times R3} \right) - \left(\Delta V_{GATE} \times \frac{R1}{R3} \right)$$

where V_{UVL} is typically 1.223V. The supply voltage to release from undervoltage lockout (supply voltage increasing) is:

$$V_{UV,LH} = V_{UVH} \left(\frac{R2 \times R3 + R1 \times R3 + R1 \times R2}{R2 \times R3} \right)$$

where V_{UVH} is typically 1.243V. The supply undervoltage lockout hysteresis is the difference, or:

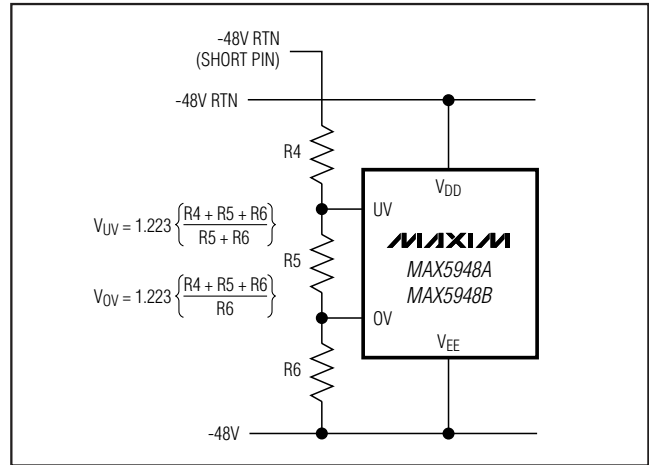


Figure 11a. Undervoltage and Overvoltage Sensing

$$V_{UV,HYS} = V_{UVHY} \left(\frac{R2 \times R3 + R1 \times R3 + R1 \times R2}{R2 \times R3} \right) + \left(\Delta V_{GATE} \times \frac{R1}{R3} \right)$$

where V_{UVHY} is typically 20mV.

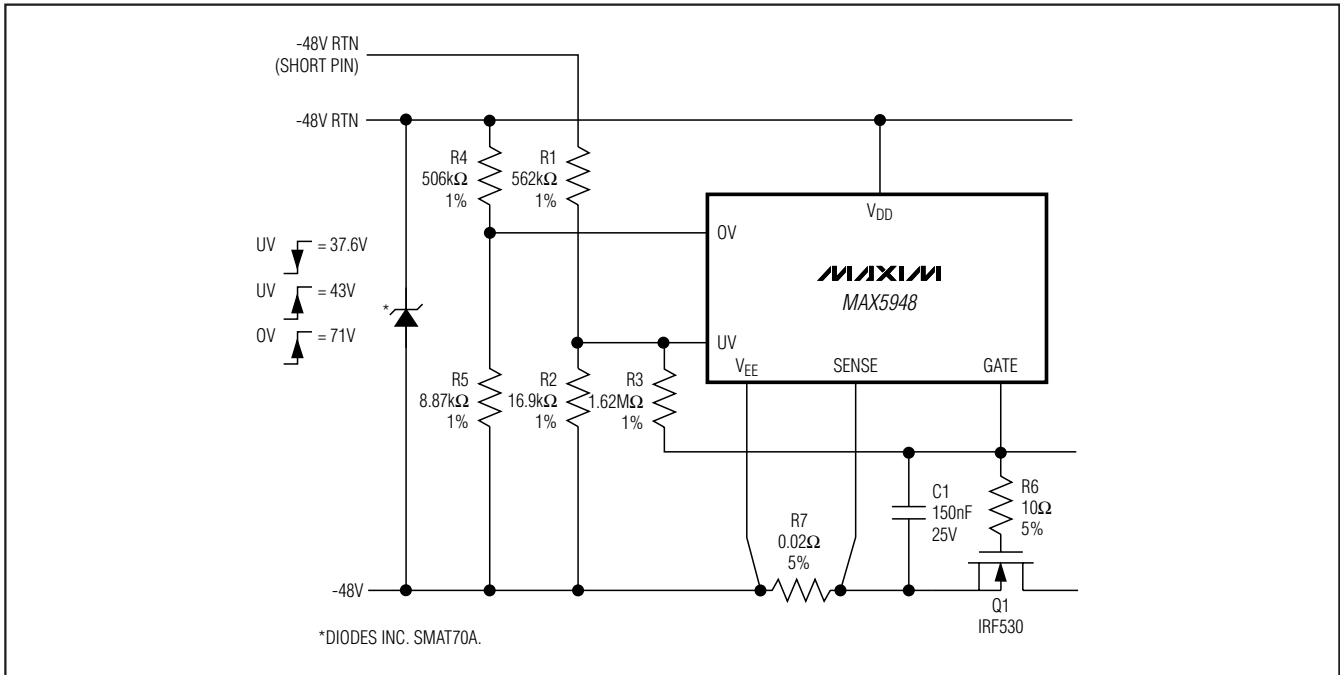


Figure 11b. Programmable Hysteresis For Undervoltage

-48V Hot-Swap Controllers with External RSENSE

MAX5948A/MAX5948B

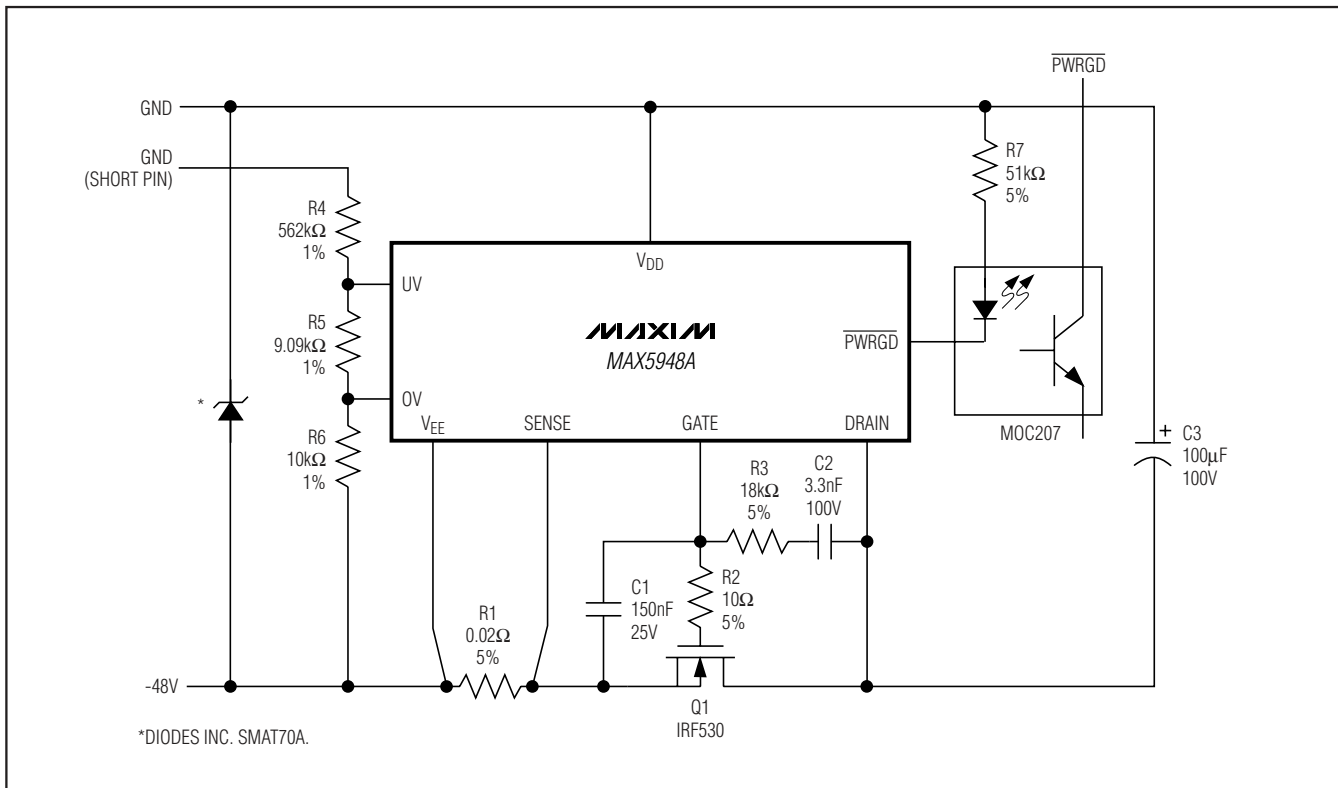


Figure 14. Using \overline{PWRGD} to Drive an Optoisolator

Applications Information

(Refer to the *Typical Operating Circuit*.)

Sense Resistor

The circuit-breaker threshold is set to 50mV (typically). Select a sense resistor that causes a drop equal to or above the current-limit threshold at a current level above the maximum normal operating current. Typically, set the overload current to 1.5 to 2.0 times the nominal load current plus the load-capacitance charging current during startup. Choose the sense resistor power rating to be greater than $(V_{CB})^2 / R_{SENSE}$.

Component Selection Procedure

- Determine load capacitance:
 $C_L = C_3 + C_4 + \text{module input capacitance}$
- Determine load current, I_{LOAD} .
- Select circuit-breaker current, for example:
 $I_{CB} = 2 \times I_{LOAD}$
- Calculate R_{SENSE} :

$$R_{SENSE} = \frac{50\text{mV}}{I_{CB}}$$

Realize that I_{CB} varies $\pm 20\%$ due to trip-voltage tolerance.

- Set allowable inrush current:

$$I_{INRUSH} \leq 0.8 \times \frac{40\text{mV}}{R_{SENSE}} - I_{LOAD} \text{ or}$$

$$I_{INRUSH} + I_{LOAD} \leq 0.8 \times I_{CB(MIN)}$$

- Determine value of C2:

$$C_2 = \frac{45\mu\text{A} \times C_L}{I_{INRUSH}}$$

- Calculate value of C1:

$$C_1 = (C_2 + C_{gd}) \times \left(\frac{V_{IN(MAX)} - V_{GS(TH)}}{V_{GS(TH)}} \right)$$

-48V Hot-Swap Controllers with External RSENSE

Using the IRL520NS, $V_{DS} \leq 0.625V$ even at $+80^{\circ}C$ so efficiency $\geq 98.6\%$ at $80^{\circ}C$. $P_D \leq 1.56W$ and junction temperature rise above case temperature would be $5^{\circ}C$ due to the package $\theta_{JC} = 3.1^{\circ}C/W$ thermal resistance. Of course, using the SUD40N10-25 would yield an efficiency greater than 99.8% to compensate for the increased cost.

If I_{CB} is set to twice I_{LOAD} , or 5A, V_{DS} momentarily doubles to $\leq 1.25V$. If $C_{OUT} = 4000\mu F$, transient-line input voltage is $\Delta 36V$, the 5A charging-current pulse is:

$$t = \frac{4000\mu F \times 1.25V}{5A} = 1ms$$

Entering the data sheet transient-thermal-resistance curves at 1ms provides a $\theta_{JC} = 0.9^{\circ}C/W$. $P_D = 6.25W$, so $\Delta t_{JC} = 5.6^{\circ}C$. Clearly, this is not a problem.

Example 2:

$I_{LOAD} = 10A$, efficiency = 98%, allowing $V_{DS} = 0.96V$ but $R_{DS(ON)} \leq 96m\Omega$. An IRF530 in a D²PAK exhibits $R_{DS(ON)} \leq 90m\Omega$ at $+25^{\circ}C$ and $\leq 135m\Omega$ at $+80^{\circ}C$. Power dissipation is 9.6W at $+25^{\circ}C$ or 14.4W at $+80^{\circ}C$. Junction-to-case thermal resistance is $1.9W/^{\circ}C$, so the junction temperature rise would be approximately $5^{\circ}C$ above the $+25^{\circ}C$ case temperature. For higher efficiency, consider IRL540NS with $R_{DS(ON)} \leq 44m\Omega$. This allows $\eta = 99\%$, $P_D \leq 4.4W$, and $T_{JC} = +4^{\circ}C$ ($\theta_{JC} = 1.1^{\circ}C/W$) at $+25^{\circ}C$.

Thermal calculations for the transient condition yield $I_{CB} = 20A$, $V_{DS} = 1.8V$, $t = 0.5ms$, transient $\theta_{JC} = 0.12^{\circ}C/W$, $P_D = 36W$ and $\Delta t_{JC} = 4.3^{\circ}C$.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to www.maxim-ic.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 SO	S8+5	21-0041	90-0096

-48V Hot-Swap Controllers with External RSENSE

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/04	Initial release	—
1	8/11	Updated <i>Ordering Information, Absolute Maximum Ratings, Electrical Characteristics, and Package Information.</i>	1, 2, 3, 17

MAX5948A/MAX5948B

MAX5948A/MAX5948B

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