NCP2817

NOCAP™ LongPlay Headphone Amplifier

NCP2817 is a dual LongPlay true ground headphone amplifier designed for portable communication device applications such as mobile phones. This part is capable of delivering typical 27 mW of continuous average power into a 32 Ω load from a 1.8 V power supply with a THD+N of 1%.

Based on the power supply delivered to the device, an internal power management block generates a symmetrical positive and negative voltage. Thus, the internal amplifiers provide outputs referenced to Ground and the losses are reduced which helps to increase the battery life. In this NOCAP configuration, the two external heavy coupling capacitors can be removed. It offers significant space and cost savings compared to a typical stereo application.

NCP2817 is available with internal gain of −1.5 V/V. It reaches a superior −100 dB PSRR and noise floor. Thus, it offers high fidelity audio sound, as well as a direct connection to the battery. It contains circuitry to prevent from “Pop & Click” noise that would otherwise occur during turn−on and turn−off transitions. The device is available in 12 bump CSP package (1.62 x 1.22, 0.4P) which helps to save space on the board.

Features

- NOCAP Output Eliminates DC−Blocking Capacitors:
  - Saves Board Area
  - Saves Component Cost
  - No Low−Frequency Response Attenuation
- LongPlay Architecture: Increase the Battery Life
- High PSRR (−100 dB): Direct Connection to the Battery
- High SNR Performance (100 dB)
- “Pop and Click” Noise Protection Circuitry
- Internal Gain (−1.5 V/V) or External Adjustable Gain
- Ultra Low Current Shutdown Mode
- High Impedance Mode
- 1.6 V − 5.5 V Operation
- Thermal Overload Protection Circuitry
- CSP 1.62 x 1.22, 0.4P
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

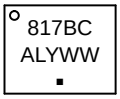
- Headset Audio Amplifier for
  - Cellular Phones
  - MP3 player
  - Personal Digital Assistant and Portable Media Player
  - Portable devices

ON Semiconductor®

www.onsemi.com

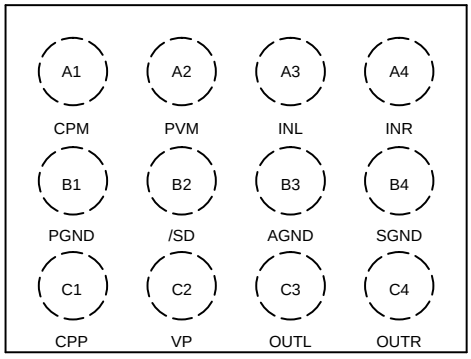
MARKING DIAGRAM

12 PIN CSP
FC SUFFIX
CASE 499BJ



A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
▪ = Pb−Free Package

PIN ASSIGNMENT



(Top View)
12−Pin 1.2 x 1.6 mm CSP

ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

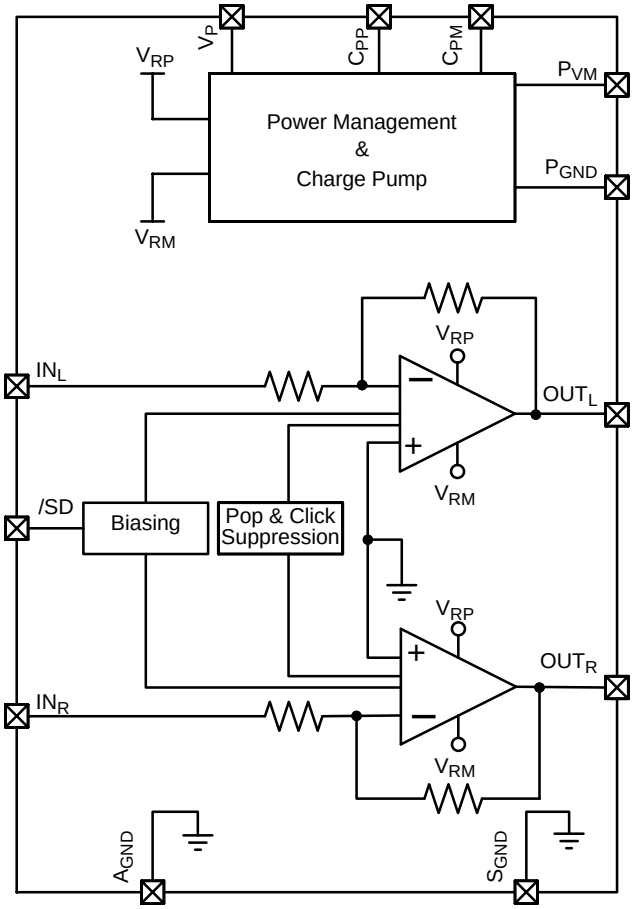


Figure 1. Block Diagram

PIN FUNCTION DESCRIPTION

Pin	Pin Name	Type	Description
A1	C_{PM}	Input / Output	Charge pump flying capacitor negative terminal. A 1 μF ceramic capacitor to C_{PP} is required
A2	P_{VM}	Output	Charge pump output. A 1 μF ceramic capacitor to ground is needed
A3	IN_L	Input	Left input of the audio source
A4	IN_R	Input	Right input of the audio source
B1	P_{GND}	Ground	Power ground. This pin should be connected directly to the ground plane.
B2	/SD	Input	Enable activation.
B4	S_{GND}	Ground	Sense Ground. Connect to shield terminal of headphone jack or ground plane.
C1	C_{PP}	Input / Output	Charge pump flying capacitor positive terminal. A 1 μF ceramic capacitor to C_{PM} is required
C2	V_P	Power	Positive supply voltage. Connected to single secondary cell Lithium−Ion battery or any other kind of power supply
C3	OUT_L	Output	Left audio channel output signal
C4	OUT_R	Output	Right audio channel output signal
B3	A_{GND}	Ground	Analog ground. This pin should be connected directly to the GND plane. Careful layout and no direct connection to other ground pins are required to ensure good noise immunity

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
V_P Pin: Power Supply Voltage (Note 1)	V_P	−0.3 to + 6.0	V
/SD Pin: Input	V_{mr1}	−0.3 to V_P + 0.3	V
Human Body Model (HBM) ESD Rating are (Notes 2 and 3)	ESD HBM	2000	V
Machine Model (MM) ESD Rating are (Note 2 and 3)	ESD MM	200	V
CSP 1.62 x 1.22, 0.4P package (Note 6 and 7) Thermal Resistance Junction to Case	$R_{\theta JC}$	(Note 7)	°C/W
Operating Ambient Temperature Range	T_A	−40 to + 85	°C
Operating Junction Temperature Range	T_J	−40 to + 125	°C
Maximum Junction Temperature (Note 6)	T_{JMAX}	+ 150	°C
Storage Temperature Range	T_{STG}	−65 to + 150	°C
Moisture Sensitivity (Note 5)	MSL	Level 1	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Maximum electrical ratings are defined as those values beyond which damage to the device may occur at T_A = 25°C.
2. According to JEDEC standard JESD22−A108B.
3. This device series contains ESD protection and passes the following tests:
   Human Body Model (HBM) ±2.0 kV per JEDEC standard: JESD22−A114 for all pins.
   Machine Model (MM) ±200 V per JEDEC standard: JESD22−A115 for all pins.
4. Latch up Current Maximum Rating: ±100 mA per JEDEC standard: JESD78 class II.
5. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020A.
6. The thermal shutdown set to 150 °C (typical) avoids irreversible damage on the device due to power dissipation.
7. The $R_{\theta CA}$ is dependent on the PCB heat dissipation. The maximum power dissipation (P_D) is dependent on the min input voltage, the max output current and external components selected.

$$R_{\theta CA} = \frac{125 - T_A}{P_D} - R_{\theta JC}$$

ELECTRICAL CHARACTERISTICS Min & Max Limits apply for T_A between −40°C to +85°C and T_J up to + 125°C for V_P = 3.6 V (Unless otherwise noted). Typical values are referenced to T_A = + 25°C and V_P = 3.6 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{BATTERY}$	Supply voltage range		1.6		5.5	V
I_{SD}	Shutdown current				1	μA
I_Q	Quiescent current	V_P = 1.8 V		2.3	3.0	mA
R_{IN}	Input resistance		7.5	10	12.5	kΩ
R_{SD}	/SD pull−down resistor			300		kΩ
	Maximum input signal swing			2.8		V_{PP}
V_{IH}	High−level input voltage SD pin		1.2			V
V_{IL}	Low−level input voltage SD pin				0.4	V
UVLO	UVLO threshold	Falling edge		1.4		V
$UVLO_{HYS}$	UVLO hysteresis			100		mV
T_{SD}	Thermal shutdown temperature			160		°C
V_{OS}	Output offset voltage	Input AC grounded		± 0.5		mV
T_{WU}	Turning On time			1		ms
V_{LP}	Max Output Swing (peak value)	V_P = 1.8 V, Headset = 32 Ω	1.13			V_{peak}
P_O	Max Output Power (Note 8)	V_P = 1.8 V, THD+N = 1% Headset = 16 Ω Headset = 32 Ω	 20	 41 27		mW

8. Guaranteed by design and characterized.
9. Typical application circuit as depicted

ELECTRICAL CHARACTERISTICS Min & Max Limits apply for T_A between −40°C to +85°C and T_J up to + 125°C for V_P = 3.6 V (Unless otherwise noted). Typical values are referenced to T_A = + 25°C and V_P = 3.6 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
P_O	Max Output Power	V_P = 3.6 V, THD+N = 1% Headset = 16 Ω Headset = 32 Ω		 42 27		mW
	Crosstalk (Note 8)	Headset ≥ 16 Ω		−95	−80	dB
PSRR	Power Supply Rejection Ratio	Inputs Shorted to Ground F = 217 Hz to 1 kHz		−100		dB
THD+N	Total Harmonic Distortion + Noise	Headset = 16 Ω P_{OUT} = 10 mW, F = 1 kHz		0.02		%
THD+N	Total Harmonic Distortion + Noise	Headset = 32 Ω P_{OUT} = 10 mW, F = 1 kHz		0.02		%
THD+N	Total Harmonic Distortion + Noise	Headset = 32 Ω $V_{OUTR} - V_{OUTL}$ = 400 mV, F = 1 kHz		−80		dB
SNR	Signal to noise ratio			100		dB
Z_{SD}	Output Impedance in Shutdown Mode			12		kΩ
	Max Channel to channel gain tolerance	B Version only T_A = +25°C	−2	±0.3	+2	%
F_{SW1}	Headset charge pump switching frequency	P_{OUT} > 500 μW		1		MHz
F_{SW2}	Headset charge pump switching frequency	P_{OUT} < 500 μW		125		kHz
A_V	Voltage Gain		−1.54	−1.5	−1.46	V/V

8. Guaranteed by design and characterized.
9. Typical application circuit as depicted

TYPICAL OPERATING CHARACTERISTICS

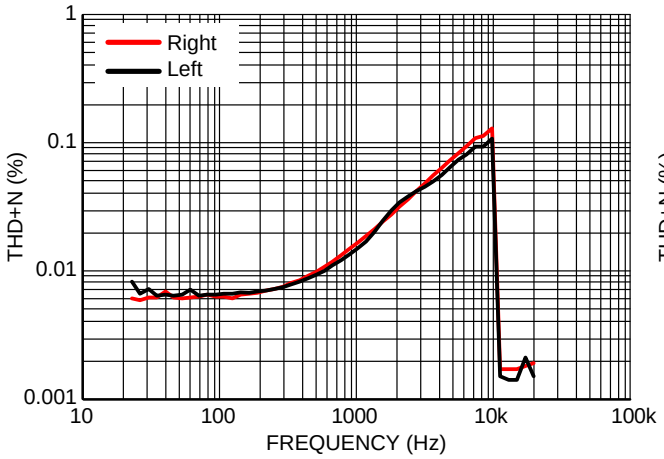


Figure 2. THD+N vs Frequency @ P_{out} = 10 mW, R_L = 32 Ω, V_P = 1.8 V

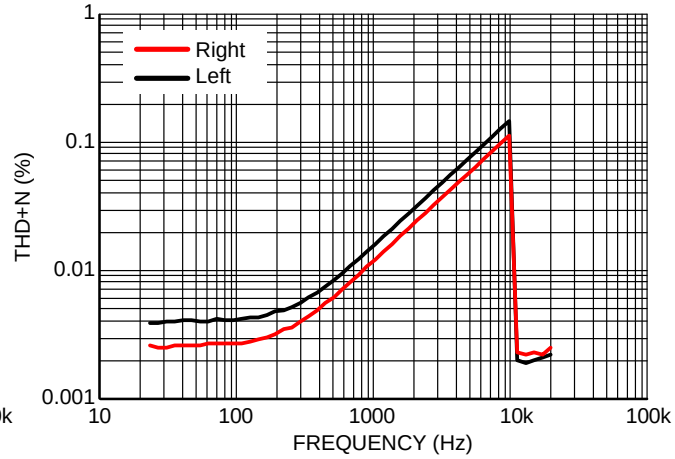


Figure 3. THD+N vs Frequency @ P_{out} = 10 mW, R_L = 16 Ω, V_P = 1.8 V

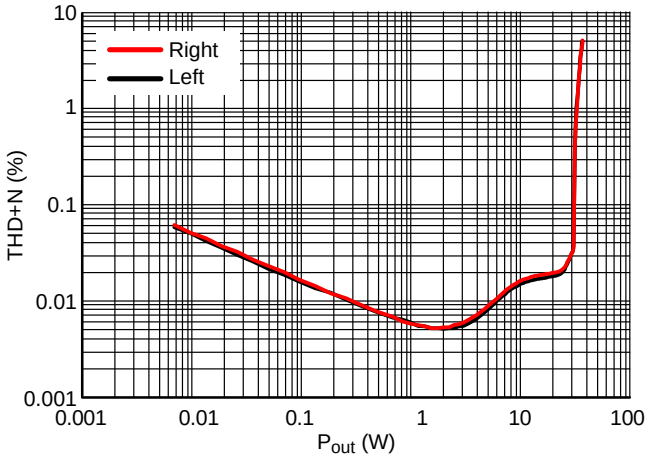


Figure 4. THD+N vs P_{out} @ 25°C Load = 32 Ω, V_P = 1.8 V

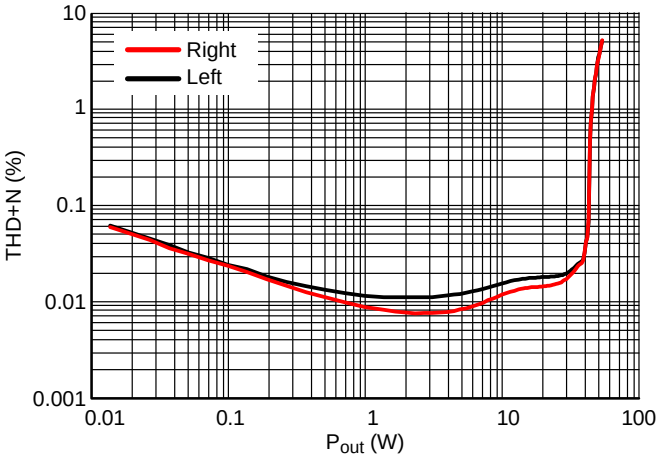


Figure 5. THD+N vs P_{out} @ 25°C Load = 16 Ω, V_P = 1.8 V

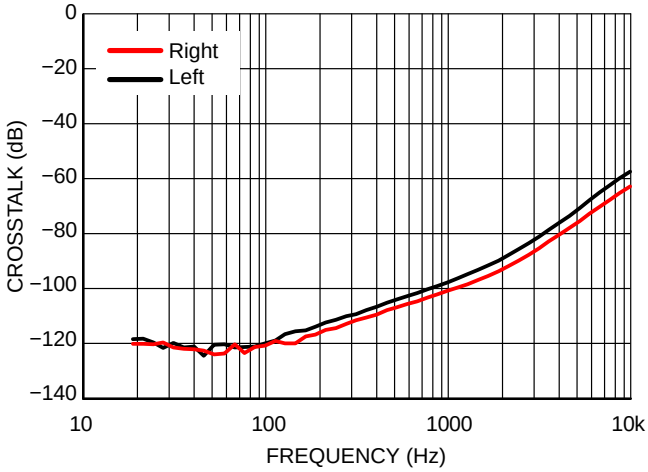


Figure 6. PSRR vs Frequency @ V_P = 3.6 V

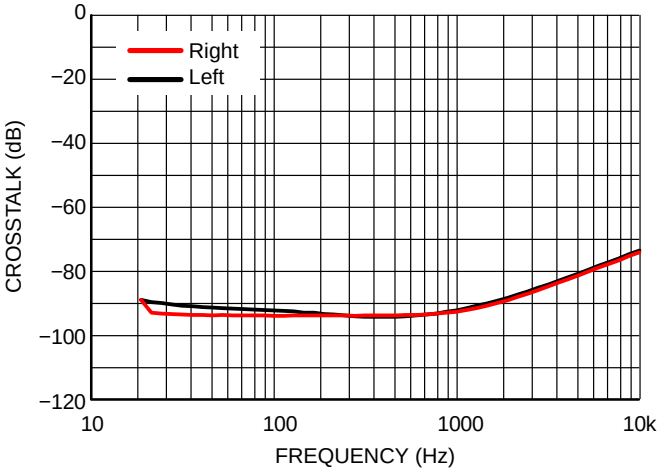


Figure 7. Crosstalk vs. Frequency @ V_P = 3.6 V P_{out} = 10 mW

TYPICAL OPERATING CHARACTERISTICS

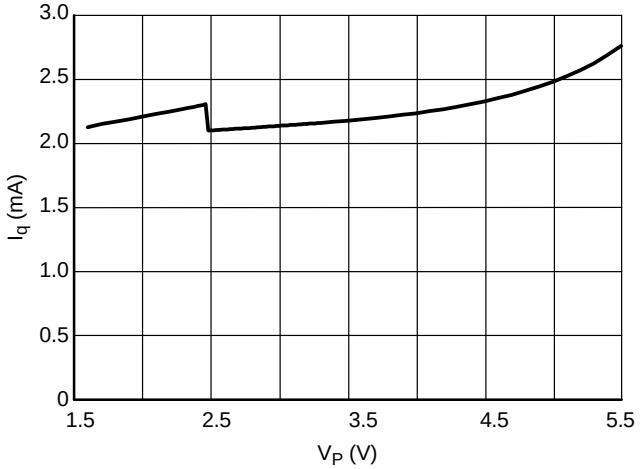


Figure 8. Quiescent Current vs V_P (V_P Rising)

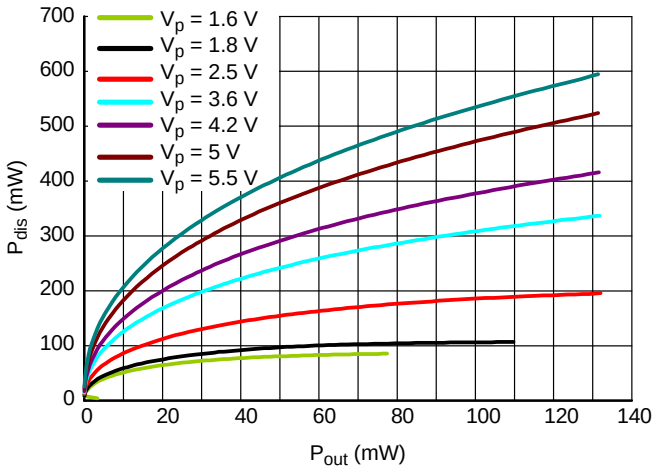


Figure 9. Power Dissipation vs P_{out} @ 25°C (P_{out} Left + Right)

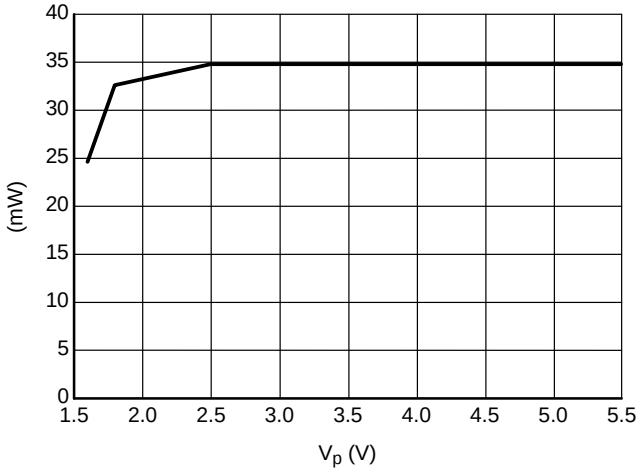


Figure 10. Maximum Output Power vs V_p (THD+N < 1%, R_L = 32 Ω)

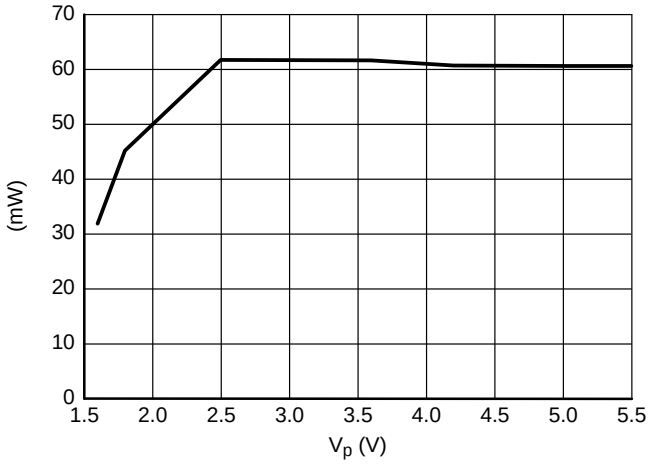


Figure 11. Maximum Output Power vs V_p(THD+N < 1%, R_L = 16 Ω)

DETAIL OPERATING DESCRIPTION

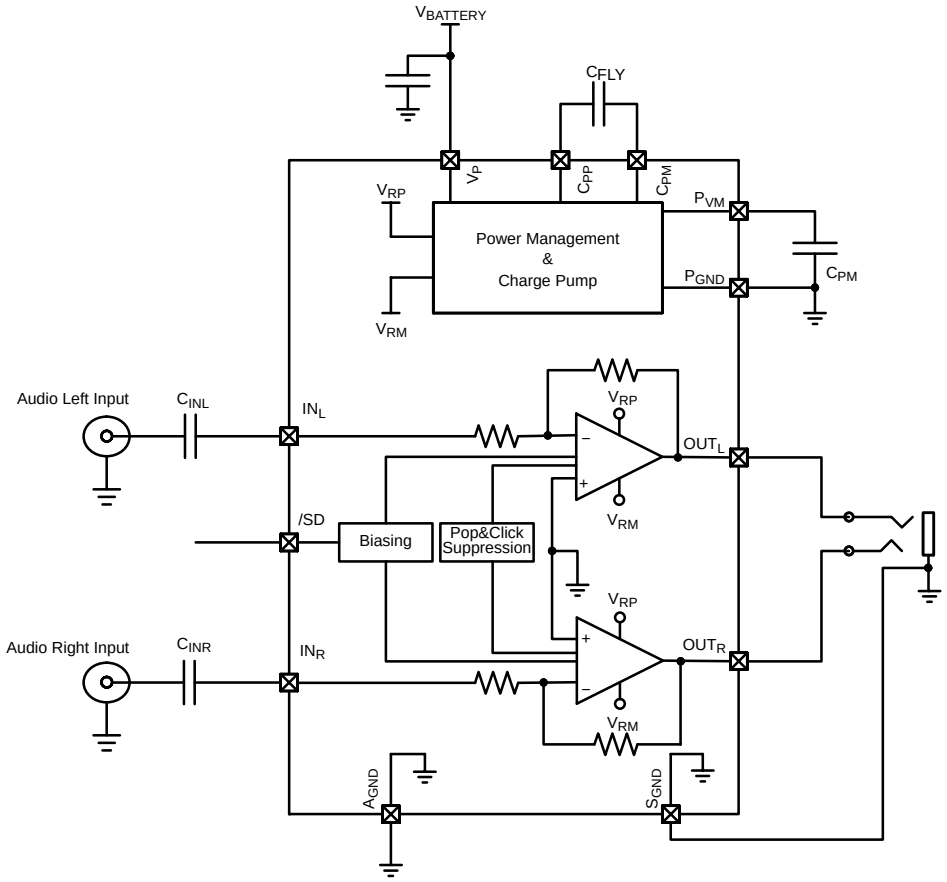


Figure 12. Typical Application Circuit

Detailed Descriptions

The NCP2817 stereo headphone amplifier features the ON Semiconductor NOCAP architecture that eliminates the large output DC−blocking capacitors required by conventional headphone amplifier.

An integrated power supply block generates low noise positive (V_{RP}) and negative (V_{RM}) voltages from the positive supply voltage (V_P). The stereo headphone amplifiers operate from these symmetrical supplies. Amplifiers output are referenced to ground (GND), instead of DC voltage (typically $V_P/2$) for conventional headphone amplifiers.

The NCP2817 integrates two true ground amplifiers, an Under Voltage Lock Out (UVLO), a short circuit protection and a thermal shutdown circuitry. In addition, a special circuit is embedded to eliminate pop and click noise that occurs during turn on and turn off time.

NCP2817 has an embedded gain setting network set to 1.5 V/V.

NOCAP™

NOCAP is a patented architecture which requires only two small ceramic capacitors. From single positive only rail, it generates the symmetrical positive and negative rails that supplies amplifiers output stage. This feature allows the output of the amplifiers to be biased around the ground level and eliminates need of huge DC voltage blocking capacitors.

LongPlay Architecture

The “LongPlay” feature, based on unique ultra low current consumption architecture saves more battery life by reducing the quiescent current depending on the load.

Current Limit Protection Circuit

The NCP2817 output power stage features a protection circuitry against short to ground. The current is limited to 300 mA typical when an output is shorted to GND and a signal is applied to the input.

Thermal Overload Protection

Internal amplifiers are switched off when the temperature exceed 160°C, and will be switched back on when the temperature decreases below 140°C.

Under Voltage Lockout

When the battery voltage decreases below 1.4 V, the amplifiers are turned off. The hysteresis to turn back on the device is 100 mV.

Pop and Click Suppression Circuitry

The NCP2817 includes a special circuitry to eliminate any pop and click noise during turn on and turn off time.

During uncontrolled turn on and turn off sequences, normal amplifiers would create an output offset. This offset drives the loudspeaker and generates a parasitic noise called “pop and click noise”.

The NCP2817 carefully controls the amplifier output stages during turn on and off sequences to eliminate this problem.

Input capacitor selection

The input coupling capacitor blocks the DC voltage at the amplifier input terminal. This capacitor creates a high−pass filter with the R_{IN} input resistor (10 kΩ for NCP2817).

The size of the capacitor must be large enough to cut off low frequencies without severe attenuation in the audio bandwidth (20 Hz − 20 kHz).

The cut off frequency for the input high−pass filter is:

$$F_c = \frac{1}{2\pi R_{in} C_{in}}$$

With R_{IN} = 10 kΩ
A F_c < 20 Hz is recommended.

Charge Pump Capacitor Selection

Use ceramic capacitor with low ESR for better performances. X5R / X7R capacitor is recommended.

The C_{FLY} flying capacitor serves to transfer charge during the generation of the negative voltage and directly affects load regulation and charge pump output impedance. A too low value results in poor current performance while higher value increases charge pump regulation and lowers output impedance (until internal switches $R_{DS(on)}$ becomes predominant). We recommend 1 μF, but lower values can be uses in systems with lower audio power requirements.

The C_{PVM} capacitor must be equal at least to the C_{FLY} capacitor to allow maximum transfer charge. In addition, the ESR of C_{PVM} capacitor directly affects ripple on P_{VM} as well as charge pump output impedance. We recommend 1 μF, but lower values can be uses in systems with lower audio power requirements.

Table 1. SUGGEST TYPICAL VALUE AND MANUFACTURER

Value	Reference	Package	Manufac-turer
1 μF	C1005X5R0J105K	0402	TDK
1 μF	GRM155R60J105K19	0402	Murata

Power Supply Decoupling Capacitor (C1)

The NCP2817 is a NOCAP amplifier and proper power supply bypassing is critical to reduce noise, high THD+N and PSRR performances. It is recommended to use a 1uF X5R / X7R ceramic capacitor and place it as close as possible to the V_P pin.

Shutdown Function

The device enters in shutdown mode when shutdown signal is low. During the shutdown mode, the DC quiescent current of the circuit does not exceed 1 μA. In this configuration, the output impedance is 20 kΩ on each output.

Layout Recommendation

Minimize trace impedance of the power, the ground and all output traces. The voltage drop between NCP2817 and the headset load results in decrease of output power and efficiency. We strongly recommend using wide traces for power supply inputs to optimize the power supplies efficiency and regulation performances. Good ground connection improves the amplifier immunity to external switching noise, improves crosstalk between channels as well as general audio performances. We also recommend wide PCB traces for the power outputs routing. If possible, we recommend to use local Ground and power planes.

The power supply decoupling capacitor C_{BYP} will help to minimize the input voltage ripple during fast load transients. It is important to minimize traces impedances from C_{BYP} to GND plane and from C_{BYP} to V_P pin as close as possible of the V_P pin. C_{BYP} should be placed as close as possible to the V_P pin.

The charge pump creates the VPM negative voltage that supplies the amplifiers. C_{FLY} and C_{PVM} capacitors location and access impedances are also critical. Connect C_{FLY} and C_{PVM} as close as possible of the NCP2817 and route their terminal to the associated pin with wide traces to minimize impedance and optimize the charge pump ripple and efficiency performances. In addition, the C_{FLY} and C_{PVM} capacitors as well as the traces connecting capacitors to the device should be kept away from the audio input and output traces to avoid any switching noise coupling with the audio signal.

A_{GND} is the ground reference for all internal analog features so, particular attention should govern the A_{GND} pin connection to the Ground reference plane. A_{GND} pin should be directly connected to the board Ground reference plane and keep it separated from other ground connections. The A_{GND} to GND ground reference plane trace should not be shared with the trace between S_{GND} or P_{GND} and the Ground plane.

ORDERING INFORMATION

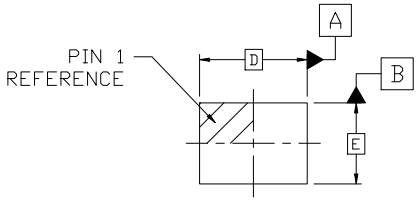
Device	Package	Shipping†
NCP2817BFCCT2G	WLCSP12 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

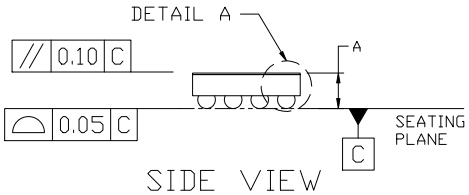
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

WLCSP12 1.62x1.22x0.539
CASE 499BJ
ISSUE D

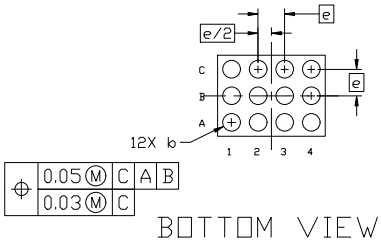
DATE 02 JUN 2022



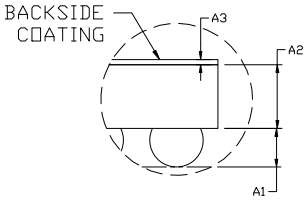
TOP VIEW



SIDE VIEW



BOTTOM VIEW

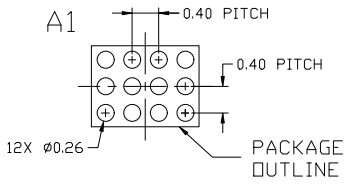


DETAIL A
SCALE 1:3

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO DATUM C.
4. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

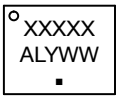
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.484	0.539	0.594
A1	0.164	0.194	0.224
A2	0.295	0.320	0.345
A3	0.025 BSC		
b	0.239	0.269	0.299
D	1.62 BSC		
E	1.22 BSC		
e	0.40 BSC		



RECOMMENDED
MOUNTING FOOTPRINT*

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98AON48124E	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	WLCSP12 1.62x1.22x0.539	PAGE 1 OF 1

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
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