

# Features

- ESD protect for one line with bi-directional
- Provide transient protection for the protected line to

IEC 61000-4-2 (ESD) ±30kV (air), ±30kV (contact) IEC 61000-4-5 (Lightning) 5A (8/20μs)

- Ultra-low capacitance: 0.4pF typical
- 0402 small DFN package saves board space
- Protect one I/O line or one power line
- Fast turn-on and low clamping voltage
- Suitable for, **8V and below,** operating voltage applications
- Solid-state silicon-avalanche and active circuit triggering technology
- Green part
- AEC-Q101 qualified

### **Applications**

- Automotive applications
- Antenna applications
- USB3.0 / USB2.0
- High Definition Multi-media Interface (HDMI)
- Hand held portable applications
- High speed data interfaces

## Description

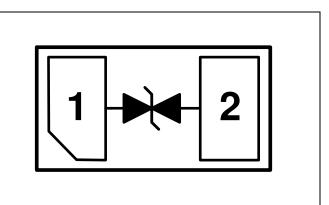
AZ9568-01F is a design which includes a bi-directional ESD rated clamping cell to protect high speed data interfaces in an electronic systems. The AZ9568-01F has been specifically designed to protect sensitive components which are connected to data and transmission lines from over-voltage caused by Electrostatic Discharging (ESD) and Lightning.

AZ9568-01F is a unique design which includes proprietary clamping cells with ultra-low capacitance in a small package. During transient conditions, the proprietary clamping cells prevent over-voltage on the control/data lines, protecting any downstream components.

AZ9568-01F is bi-directional and may be used on lines where the signal swings above and below ground.

AZ9568-01F may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 ( $\pm$ 15kV air,  $\pm$ 8kV contact discharge).

# Circuit Diagram / Pin Configuration



#### DFN1006P2E (Bottom View)

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# SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS					
PARAMETER	SYMBOL	RATING	UNIT		
Peak Pulse Current (tp = 8/20µs)	I <sub>PP</sub>	5	A		
Operating Voltage	V <sub>DC</sub>	±8.8	V		
ESD per IEC 61000-4-2 (Air)	V <sub>ESD-1</sub>	±30	kV		
ESD per IEC 61000-4-2 (Contact)	V <sub>ESD-2</sub>	±30			
Lead Soldering Temperature	T <sub>SOL</sub>	260 (10 sec.)	°C		
Operating Temperature	T <sub>OP</sub>	-55 to +125	°C		
Storage Temperature	T <sub>STO</sub>	-55 to +150	°C		

ELECTRICAL CHARACTERISTICS						
PARAMETER	SYMBOL	MIN	ТҮР	МАХ	UNIT	
Reverse Stand-Off Voltage	V <sub>RWM</sub>	T=25 °C.	-8.0		8.0	V
Reverse Leakage Current	I <sub>Leak</sub>	$V_{RWM} = \pm 8V$ , T=25 °C.			1.0	μΑ
Reverse Breakdown Voltage	$V_{BV}$	I <sub>BV</sub> = 1mA, T=25 ℃.	10			V
Surge Clamping Voltage	$V_{CL ext{-surge}}$	I <sub>PP</sub> = 5A, tp = 8/20μs, T=25°C.		16		V
ESD Clamping Voltage (Note 1)	$V_{CL-ESD}$	IEC 61000-4-2 +8kV (I <sub>TLP</sub> = 16A), Contact mode, T=25 °C.		20		V
ESD Dynamic Turn-on Resistance	R <sub>dynamic</sub>	IEC 61000-4-2, 0~+8kV, Contact mode, T=25 °C.		0.5		Ω
Channel Input Capacitance	C <sub>IN</sub>	V <sub>R</sub> = 0V, f = 1MHz, T=25 °C.		0.4	0.7	pF

Note 1: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.

TLP conditions:  $Z_0$ = 50 $\Omega$ ,  $t_p$ = 100ns,  $t_r$ = 1ns.



# **Typical Characteristics**

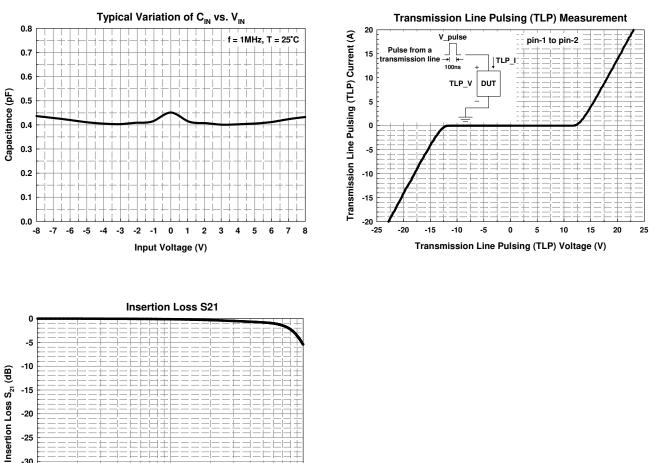
-20 -25 -30 -35

-40

1e+8

-3dB Freq.: ~ 8.7GHz

1e+9 Frequency (Hz)



1e+10



# **Application Information**

The AZ9568-01F is designed to protect one line against system ESD pulses by clamping it to an acceptable reference. It provides bi-directional protection.

The usage of the AZ9568-01F is shown in Fig. 1. Protected line, such as data line, control line, or power line, is connected at pin 1. The pin 2 is connected to a ground plane on the board. In order to minimize parasitic inductance in the board traces, all path lengths connected to the pins of AZ9568-01F should be kept as short as possible. In order to obtain enough suppression of ESD induced transient, good circuit board is critical. Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ9568-01F.
- Place the AZ9568-01F near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.
- NEVER route critical signals near board edges and near the lines which the ESD transient easily injects to.

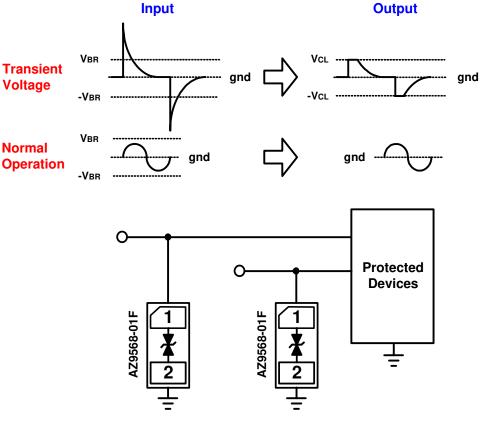
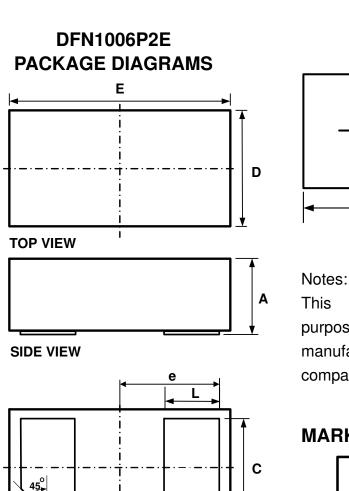


Fig. 1



## **Mechanical Details**

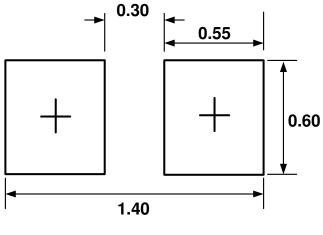
0.05



**MILLIMETERS** SYMBOL MIN. MAX. Е 0.95 1.05 D 0.55 0.65 Α 0.45 0.55 0.45 BSC е L 0.20 0.30 С 0.45 0.55

0.125 BOTTOM VIEW

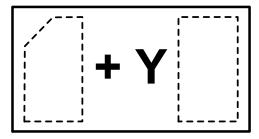
#### LAND LAYOUT



#### (Unit: mm)

This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

# **MARKING CODE**



**Top View** 

Y=Device Code

Part Number	Marking Code
AZ9568-01F.R7GR (Green part)	Y

Note. Green means Pb-free, RoHS, and Halogen free compliant.



### **Ordering Information**

PN#	Material	Туре	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZ9568-01F.R7GR	Green	T/R	7 inch	12,000/reel	4 reels = 48,000/box	6 boxes = 288,000/carton

### **Revision History**

Revision	Modification Description		
Revision 2019/01/14	Preliminary release.		
Revision 2020/08/14	ormal release.		