

PSMN2R5-60PL

N-channel 60 V, 2.6 mΩ logic level MOSFET in SOT78
27 February 2013 Product data sheet

1. General description

Logic level N-channel MOSFET in SOT78 using TrenchMOS technology. Product design and manufacture has been optimized for use in battery operated power tools.

2. Features and benefits

- High efficiency due to low switching & conduction losses
- Robust construction for demanding applications
- Logic level gate

3. Applications

- Battery-powered tools
- Load switching
- Motor control
- Uninterruptible power supplies

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V_{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C		-	-	60	V
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; <u>Fig. 1</u>	[1]	-	-	150	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; <u>Fig. 2</u>		-	-	349	W
Static charac	teristics		1		'		-
R _{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; Fig. 11		-	2	2.6	mΩ
Dynamic cha	racteristics				'		
Q _{G(tot)}	total gate charge	V _{GS} = 10 V; I _D = 25 A; V _{DS} = 48 V;		-	223	-	nC
Q_{GD}	gate-drain charge	Fig. 13; Fig. 14		-	41.2	-	nC
Avalanche ru	ggedness						
E _{DS(AL)S}	non-repetitive drain- source avalanche energy	I_D = 150 A; $V_{sup} \le$ 60 V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped; Fig. 3		-	-	521.7	mJ

[1] Continuous current is limited by package.



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5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	mb	D
2	D	drain	├	
3	S	source		mbb076 S
			TO-220AB (SOT78)	

6. Ordering information

Table 3. Ordering information

Type number	Package					
	Name	Description	Version			
PSMN2R5-60PL	TO-220AB	plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB	SOT78			

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN2R5-60PL	PSMN2R5-60PL

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C		-	60	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20 \text{ k}\Omega$		-	60	V
V_{GS}	gate-source voltage			-20	20	V
I _D	drain current	T _{mb} = 25 °C; V _{GS} = 10 V; <u>Fig. 1</u>	[1]	-	150	Α
		T _{mb} = 100 °C; V _{GS} = 10 V; <u>Fig. 1</u>	[1]	-	150	Α
I _{DM}	peak drain current	T_{mb} = 25 °C; pulsed; $t_p \le 10 \mu s$; Fig. 4		-	1002	Α

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Symbol	Parameter	Conditions		Min	Max	Unit
P _{tot}	total power dissipation	T _{mb} = 25 °C; <u>Fig. 2</u>		-	349	W
T _{stg}	storage temperature			-55	175	°C
Tj	junction temperature			-55	175	°C
T _{sld(M)}	peak soldering temperature			-	260	°C
Source-dra	in diode		1	1		
I _S	source current	T _{mb} = 25 °C	[1]	-	150	Α
I _{SM}	peak source current	pulsed; $t_p \le 10 \ \mu s$; $T_{mb} = 25 \ ^{\circ}C$		-	1002	Α
Avalanche	ruggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I_D = 150 A; $V_{sup} \le$ 60 V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped; Fig. 3		-	521.7	mJ

[1] Continuous current is limited by package.

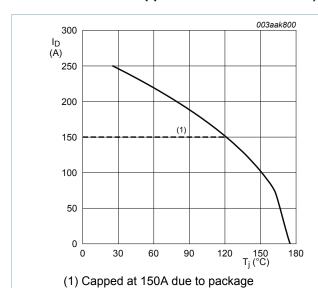


Fig. 1. Continuous drain current as a function of mounting base temperature

$$V_{GS} \geq 10\,V$$

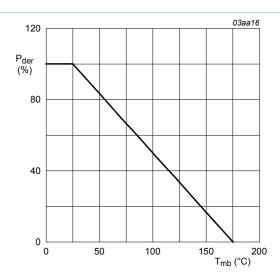


Fig. 2. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100 \,\%$$

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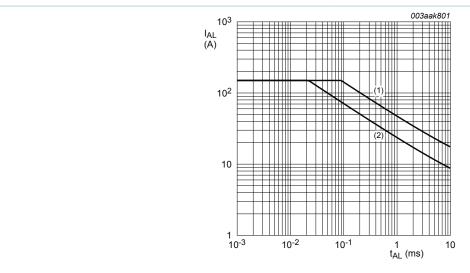
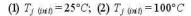


Fig. 3. Avalanche rating; avalanche current as a function of avalanche time



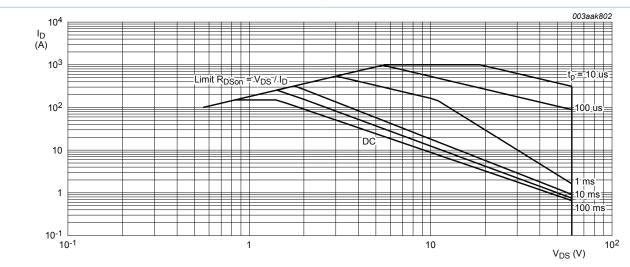


Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

 $T_{mb} = 25^{\circ}C$; I_{DM} is a single pulse

9. Thermal characteristics

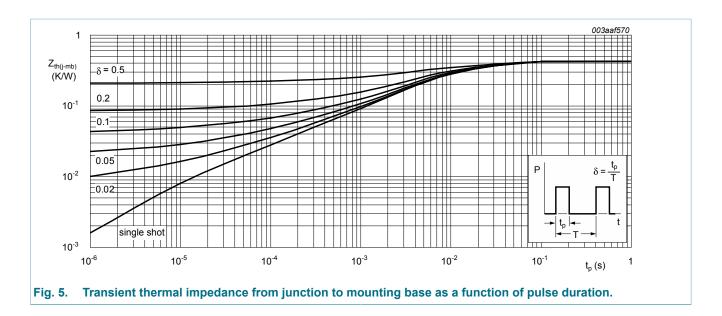
Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R _{th(j-mb)}	thermal resistance from junction to mounting base	Fig. 5	-	0.35	0.43	K/W
R _{th(j-a)}	thermal resistance from junction to ambient	vertical in still air	-	60	-	K/W

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10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics					
V _{(BR)DSS}	drain-source	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 °C$	60	-	-	V
	breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 °C$	54	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 25 °C; Fig. 9; Fig. 10	1.4	1.7	2.1	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ °C};$ Fig. 9	-	-	2.45	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ °C};$ Fig. 9	0.5	-	-	V
I _{DSS} drain leakage current	drain leakage current	$V_{DS} = 60 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 ^{\circ}\text{C}$	-	0.08	1	μΑ
		V _{DS} = 60 V; V _{GS} = 0 V; T _j = 175 °C	-	-	500	μA
I _{GSS}	gate leakage current	V _{GS} = 16 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
		V _{GS} = -16 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
R _{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; Fig. 11	-	2	2.6	mΩ
		V_{GS} = 4.5 V; I_D = 25 A; T_j = 25 °C; Fig. 11	-	2.3	3.15	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 175 °C; Fig. 12; Fig. 11	-	-	5.6	mΩ
R_G	gate resistance	f = 1 MHz	0.5	1	2	Ω

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Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Dynamic cl	haracteristics		<u> </u>			
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 48 V; V _{GS} = 10 V; Fig. 13; Fig. 14	-	223	-	nC
		I _D = 25 A; V _{DS} = 48 V; V _{GS} = 5 V; Fig. 13; Fig. 14	-	120	-	nC
Q _{GS}	gate-source charge	I _D = 25 A; V _{DS} = 48 V; V _{GS} = 10 V;	-	25.6	-	nC
Q_{GD}	gate-drain charge	Fig. 13; Fig. 14	-	41.2	-	nC
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz;	-	11700	-	pF
C _{oss}	output capacitance	T _j = 25 °C; <u>Fig. 15</u>	-	1025	-	pF
C _{rss}	reverse transfer capacitance		-	490	-	pF
t _{d(on)}	turn-on delay time	V_{DS} = 25 V; R_L = 1.8 Ω ; V_{GS} = 5 V;	-	71	-	ns
t _r	rise time	$R_{G(ext)} = 5 \Omega$	-	119	-	ns
t _{d(off)}	turn-off delay time		-	224	-	ns
t _f	fall time		-	128	-	ns
Source-dra	in diode					
V _{SD}	source-drain voltage	I _S = 25 A; V _{GS} = 0 V; T _j = 25 °C; <u>Fig. 16</u>	-	0.77	1.2	V
t _{rr}	reverse recovery time	$I_S = 20 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s}; V_{GS} = 0 \text{ V};$	-	53	-	ns
Q _r	recovered charge	V _{DS} = 25 V	-	98	-	nC

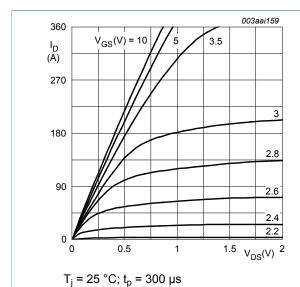


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

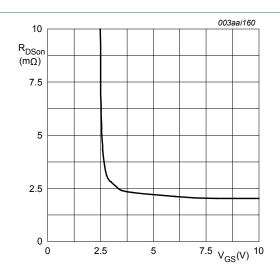


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$$T_j = 25^{\circ}C; I_D = 25A$$

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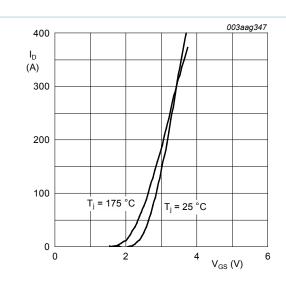


Fig. 8. Transfer characteristics: drain current as a function of gate-source voltage; typical values



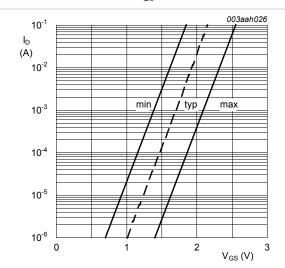


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

$$T_j = 25$$
°C; $V_{DS} = 5V$

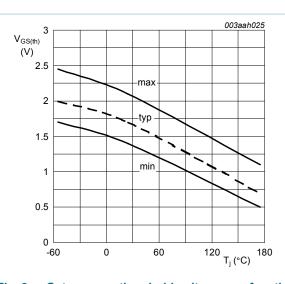
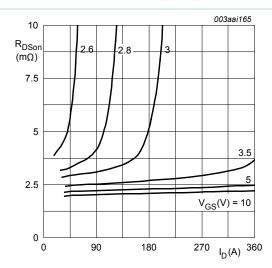


Fig. 9. Gate-source threshold voltage as a function of junction temperature

$$I_D = 1 \text{ mA}; \ V_{DS} = V_{GS}$$



 $T_i = 25 \,^{\circ}\text{C}; t_p = 300 \,\mu\text{s}$

Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

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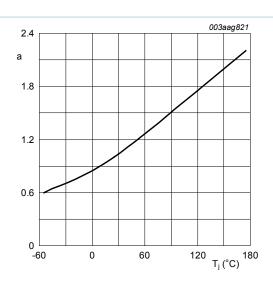


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$\mathbf{a} = \frac{R_{DSon}}{R_{DSon(25~\mathrm{C})}}$$

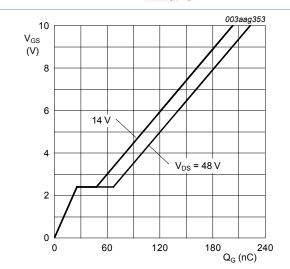


Fig. 14. Gate-source voltage as a function of gate charge; typical values

 $T_i = 25 \,^{\circ}C; I_D = 25 \,^{\circ}A$

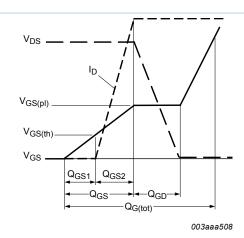


Fig. 13. Gate charge waveform definitions

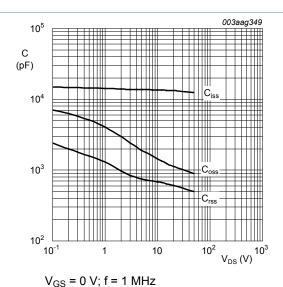
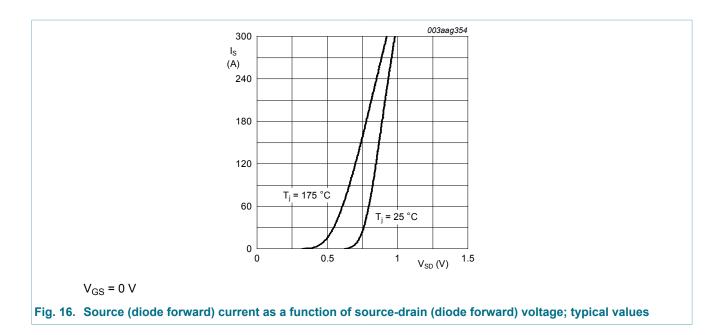


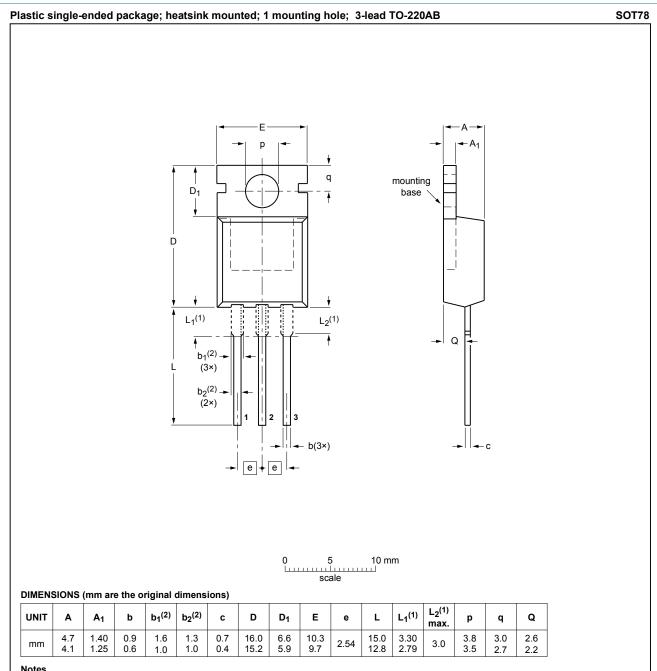
Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

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11. Package outline



- 1. Lead shoulder designs may vary.
- 2. Dimension includes excess dambar.

OUTLINE		REFERENCES		REFERENCES			EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE		
SOT78		3-lead TO-220AB	SC-46			08-04-23 08-06-13		

Fig. 17. Package outline TO-220AB (SOT78)

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