

N-Channel Enhancement Mode Power MOSFET

Description

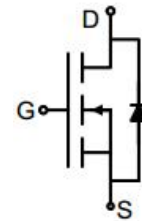
The GT10N10 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge. It can be used in a wide variety of applications.

General Features

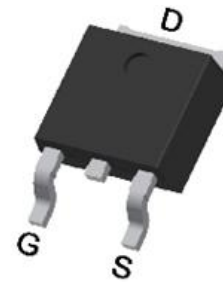
- V_{DS} 100V
- I_D (at $V_{GS} = 10V$) 7A
- $R_{DS(ON)}$ (at $V_{GS} = 10V$) < 140mΩ
- $R_{DS(ON)}$ (at $V_{GS} = 4.5V$) < 175mΩ
- 100% Avalanche Tested
- RoHS Compliant

Application

- Power switch
- DC/DC converters



Schematic diagram



TO-252

Ordering Information

Device	Package	Marking	Packaging
GT10N10	TO-252	GT10N10	2500pcs/Reel

Absolute Maximum Ratings $T_C = 25^\circ C$, unless otherwise noted

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	100	V
Continuous Drain Current	I_D	7	A
Pulsed Drain Current (note1)	I_{DM}	21	A
Gate-Source Voltage	V_{GS}	± 20	V
Power Dissipation	P_D	17	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 To 150	$^\circ C$

Thermal Resistance

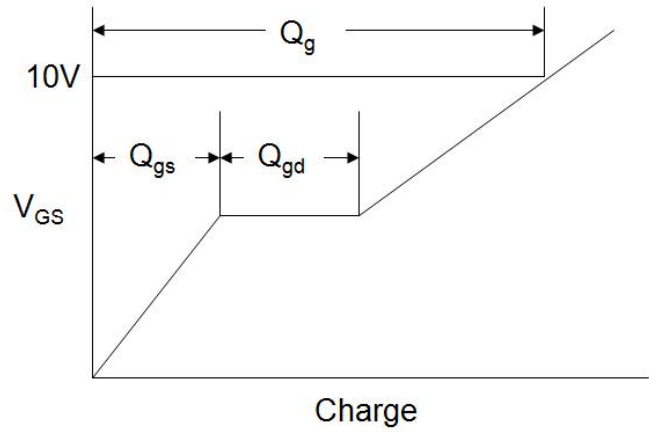
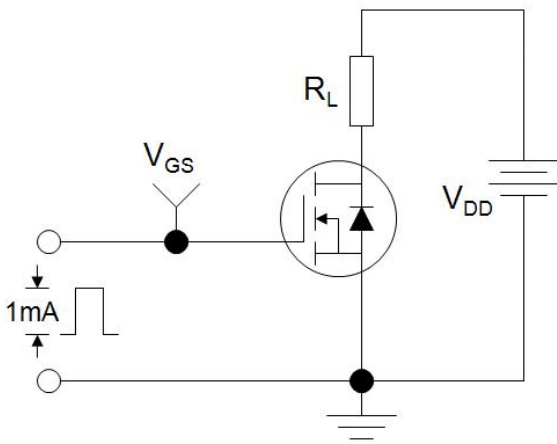
Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Ambient	R_{thJA}	50	$^\circ C/W$
Maximum Junction-to-Case	R_{thJC}	7.4	$^\circ C/W$

Specifications $T_J = 25^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Static Parameters						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	100	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 100V, V_{GS} = 0V$	--	--	1	μA
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20V$	--	--	± 100	nA
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	1.5	2	2.5	V
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 3.5A$	--	115	140	m Ω
		$V_{GS} = 4.5V, I_D = 3.5A$	--	150	175	
Forward Transconductance	g_{FS}	$V_{GS} = 15V, I_D = 2A$	3	--	--	S
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{GS} = 0V,$ $V_{DS} = 50V,$ $f = 1.0\text{MHz}$	--	206	--	pF
Output Capacitance	C_{oss}		--	28.9	--	
Reverse Transfer Capacitance	C_{rss}		--	1.4	--	
Total Gate Charge	Q_g	$V_{DD} = 50V,$ $I_D = 3.5A,$ $V_{GS} = 10V$	--	4.3	--	nC
Gate-Source Charge	Q_{gs}		--	1.5	--	
Gate-Drain Charge	Q_{gd}		--	1.1	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = 50V,$ $I_D = 3.5A,$ $R_G = 2\Omega$	--	14.7	--	ns
Turn-on Rise Time	t_r		--	3.5	--	
Turn-off Delay Time	$t_{d(off)}$		--	20.9	--	
Turn-off Fall Time	t_f		--	2.7	--	
Drain-Source Body Diode Characteristics						
Continuous Body Diode Current	I_S	$T_C = 25^\circ\text{C}$	--	--	7	A
Body Diode Voltage	V_{SD}	$T_J = 25^\circ\text{C}, I_{SD} = 3.5A, V_{GS} = 0V$	--	--	1.2	V
Reverse Recovery Charge	Q_{rr}	$I_F = 3.5A, V_{GS} = 0V$ $di/dt = 500A/\mu s$	--	52	--	nC
Reverse Recovery Time	T_{rr}		--	16	--	ns

Notes

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. Identical low side and high side switch with identical R_G

Gate Charge Test Circuit



Switch Time Test Circuit



EAS Test Circuit



Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 1. Output Characteristics

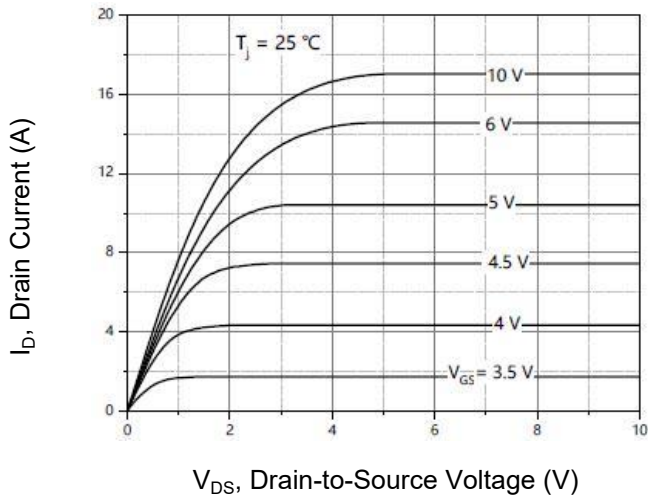


Figure 2. Transfer Characteristics

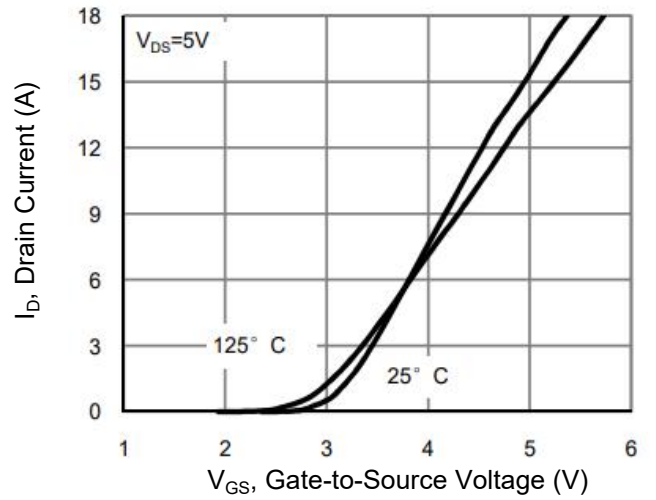


Figure 3. Drain Source On Resistance

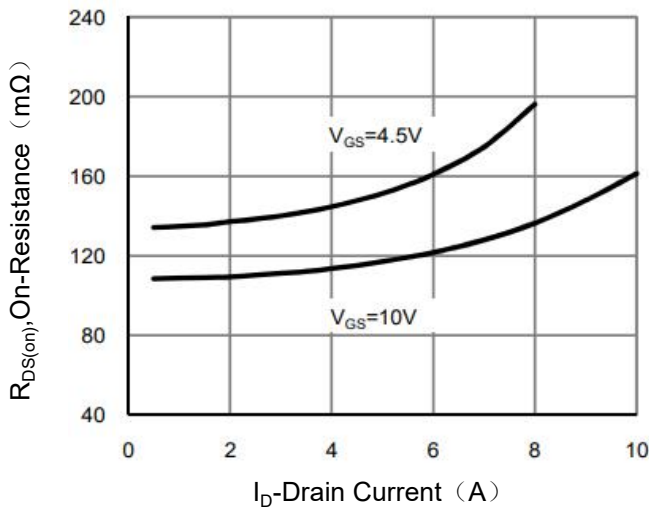


Figure 4. Gate Charge

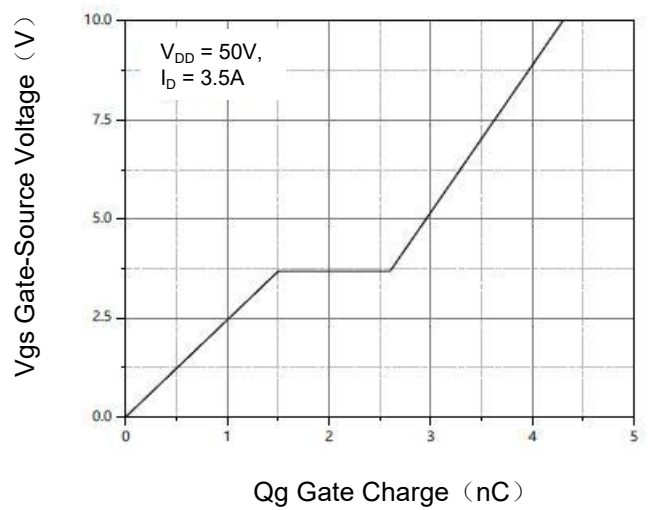


Figure 5. Capacitance

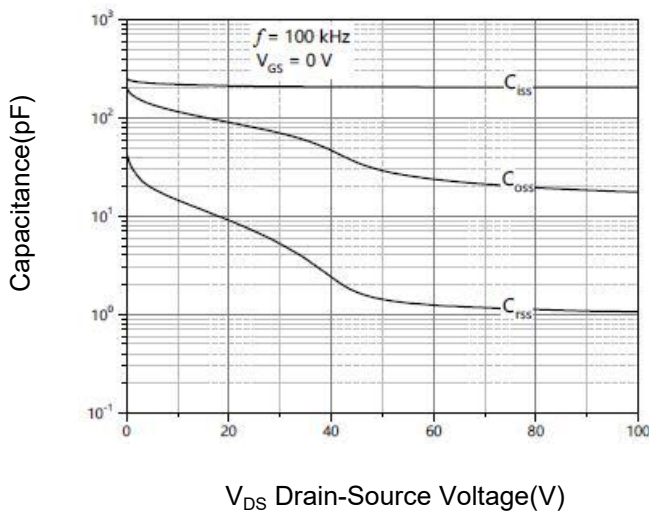
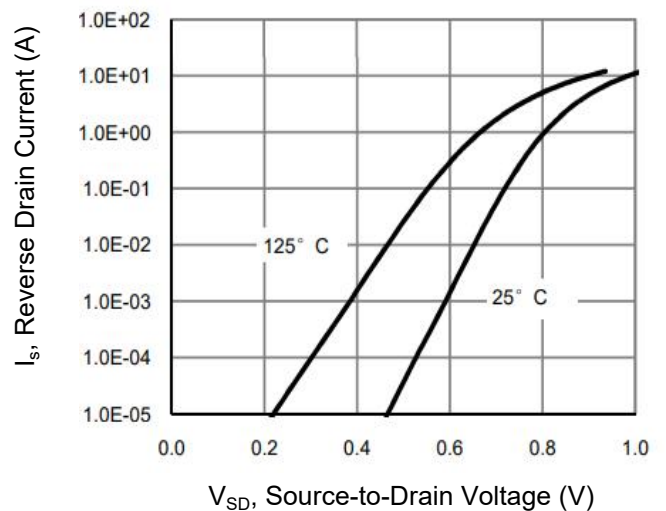


Figure 6. Source-Drain Diode Forward



Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 7. Drain-Source On-Resistance

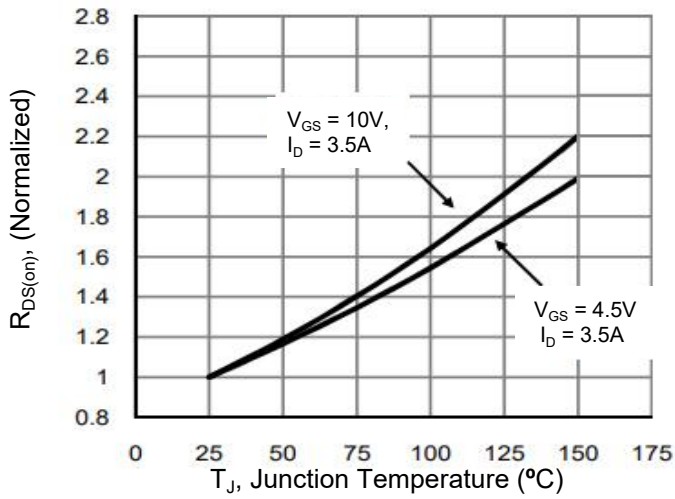


Figure 8. Safe Operation Area

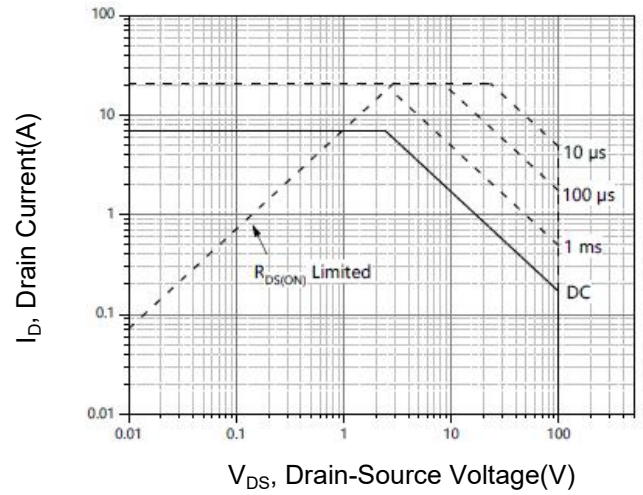
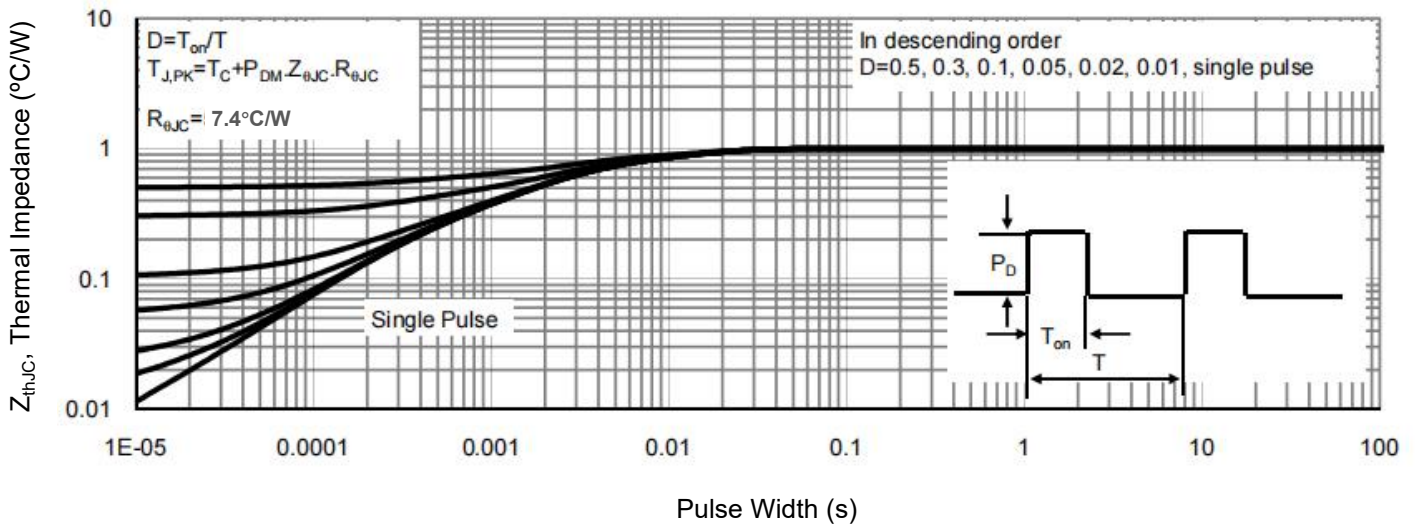
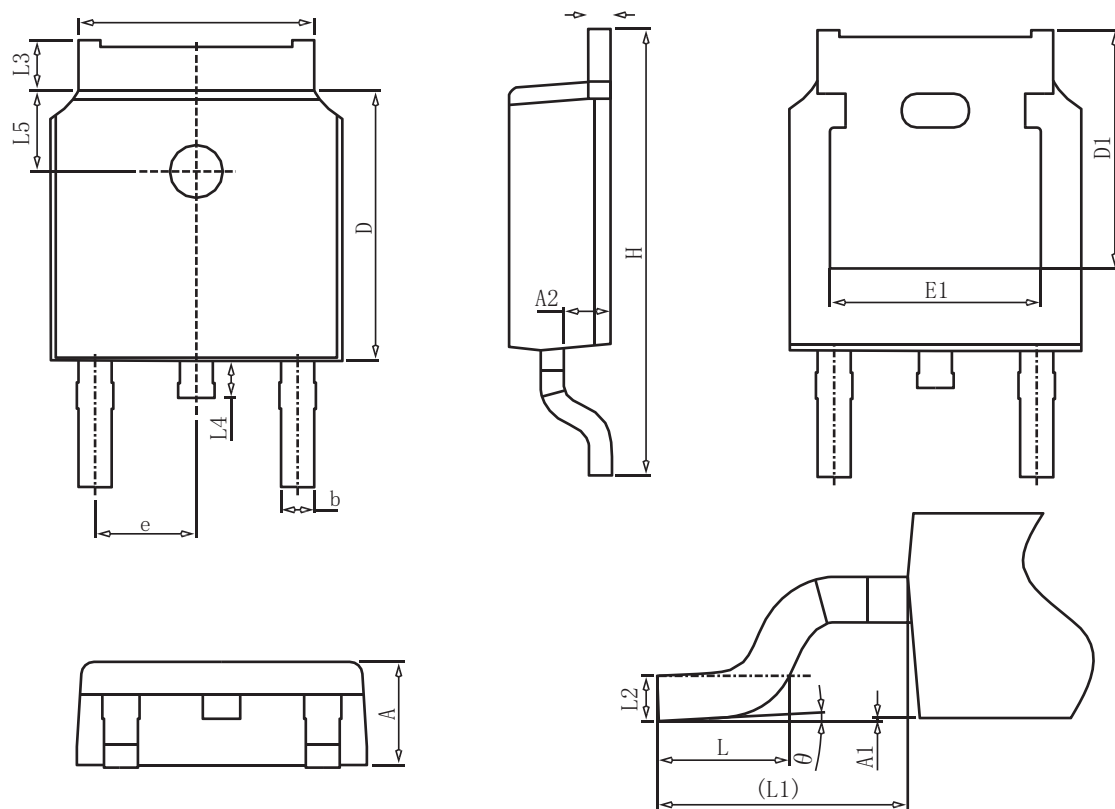


Figure 9. Normalized Maximum Transient Thermal Impedance



TO-252 Package Information



COMMON DIMENSIONS

SYMBOL	mm		
	MIN	NOM	MAX
A	2.20	2.30	2.40
A1	0.00	-	0.20
A2	0.97	1.07	1.17
b	0.68	0.78	0.90
b3	5.20	5.33	5.50
c	0.43	0.53	0.63
D	5.98	6.10	6.22
D1	5.30REF		
E	6.40	6.60	6.80
E1	4.63	-	-
e	2.286BSC		
H	9.40	10.10	10.50
L	1.38	1.50	1.75
L1	2.90REF		
L2	0.51BSC		
L3	0.88	-	1.28
L4	0.50	-	1.00
L5	1.65	1.80	1.95
θ	0°	-	8°