

USB3.0 and USB2.0 Combo Switch

Features

- → 1:2 mux/demux for USB 3.0SS, 2.0HS, and 2.0FS signals
- → Switches Tx, Rx, Dx, and USB_ID from USB3.0 connector
- → Insertion Loss for superspeed channels @ 2.5 GHz: -1.7dB
- → -3dB Bandwidth for superspeed channels: 4.7GHz
- → Return loss for superspeed channels @ 2.5GHz: -16dB
- → Low Bit-to-Bit Skew, 7ps max (between '+' and '-' bits)
- → Low Crosstalk for superspeed channels: -25dB@5.0 Gbps
- → Low Off Isolation for superspeed channels: -25dB@5.0 Gbps
- → V_{DD} Operating Range: 3.3V +/-10%
- → ESD Tolerance: 2kV HBM
- → Low channel-to-channel skew, 35ps max
- → Packaging (Pb-free & Green):
 - 32 TQFN (ZL)

Description

Pericom Semiconductor's PI3USB3102 USB3.0 and USB2.0 Combo Switch is a complete 1:2 switching solution for SuperSpeed USB 3.0 signals. PI3USB3102 provides differential high-speed lanes for the USB3.0 4.8 Gbps TX and RX lanes as well as a differential lane for 480 Mbps USB 2.0 signals and the USB_ID signal.

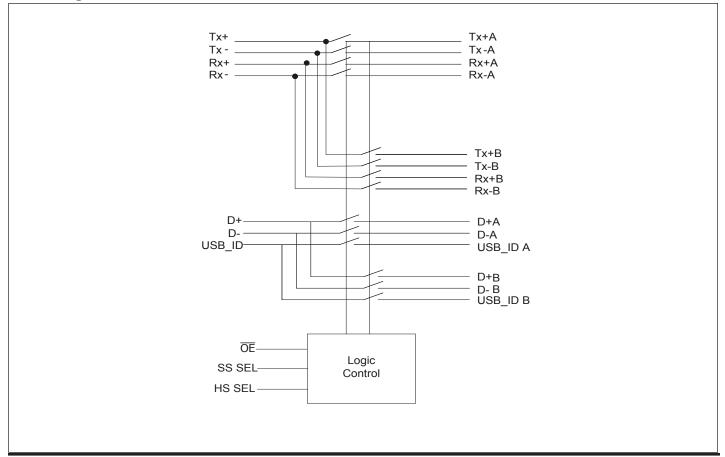
PI3USB3102 can be used to connect two hosts to a single device or a single host to two devices.

PI3USB3102 offers excellent signal integrity for high-speed signals and low power dissipation. Insertion loss is 1.7 dB and return loss is -16 dB at 2.5 GHz. Power dissipation is 6.6 mW maximum.

Application

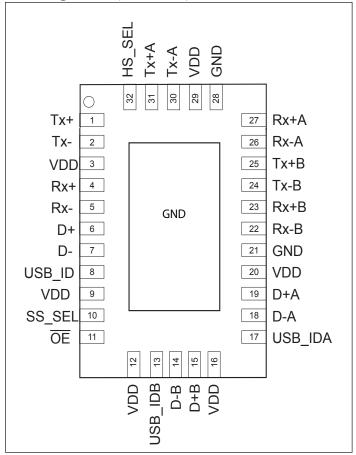
Routing of USB3.0 signals with low signal attenuation between source and sink.

Block Diagram





Pin Assignment (TQFN-32)



Truth Table

ŌĒ	SS_SEL	HS_SEL	Function
Low	Low	Low	Port A active for all channels
Low	Low	High	Port A for SS, port B for HS and ID
Low	High	Low	Port B for SS, port A for HS and ID
Low	High	High	Port B active for all channels
High	X	X	I/O's are hi-z and IC is power down



Pin Description

1 Tx+ I/O positive differential USB3.0 Tx signal for COM port 2 Tx- I/O negative differential USB3.0 Tx signal for COM port 3 VDD Power 3.3V +/-10% power supply 4 Rx+ I/O positive differential USB3.0 Rx signal for COM port 5 Rx I/O negative differential USB3.0 Rx signal for COM port 6 D+ I/O positive differential USB3.0 Rx signal for COM port 7 D- I/O negative differential USB2.0 signal for COM port 8 USB_IID I/O USB_ID for COM port 9 VDD Power 3.3V +/-10% power supply switch logic control for SuperSpeed Path 10 SS_SEL I IIf HIGH, then path B is selected for SuperSpeed channels only If LOW, then path A is selected for SuperSpeed channels only If LOW and all I/Os are hi-z 12 VDD Power 3.3V +/-10% power supply 13 USB_IDB I/O USB_ID for port B 14 D-B I/O negative differential USB2.0 signal for port B 15 D+B I/O positive differential USB2.0 signal for port B 16 VDD Power 3.3V +/-10% power supply 17 USB_IDA I/O USB_ID for port A 18 D-A I/O negative differential USB2.0 signal for port A 19 D+A I/O positive differential USB2.0 signal for port A 19 D+A I/O positive differential USB2.0 signal for port B 20 VDD Power 3.3V +/-10% power supply 21 GND Ground Ground 22 Rx-B I/O negative differential USB3.0 Rx signal for port B 23 Rx+B I/O negative differential USB3.0 Rx signal for port B 24 Tx-B I/O negative differential USB3.0 Rx signal for port B 25 Tx+B I/O negative differential USB3.0 Rx signal for port B 26 Rx-A I/O negative differential USB3.0 Rx signal for port B 27 Rx+A I/O positive differential USB3.0 Rx signal for port A 28 GND Ground Ground		cription	1		
Tx. I/O negative differential USB3.0 Tx signal for COM port 3 VDD Power 3.3V +/-10% power supply 4 Rx+ I/O positive differential USB3.0 Rx signal for COM port 5 Rx. I/O negative differential USB3.0 Rx signal for COM port 6 D+ I/O positive differential USB3.0 Rx signal for COM port 7 D- I/O negative differential USB3.0 signal for COM port 8 USB_ID I/O USB_ID for COM port 9 VDD Power 3.3V +/-10% power supply 8 switch logic control for SuperSpeed Path 10 If HIGH, then path B is selected for SuperSpeed channels only if LOW, then path A is selected for SuperSpeed channels only if LOW, then path A is selected for SuperSpeed channels only if LOW, then path A is selected for SuperSpeed channels only if LOW power supply 11 OE I Output enable. if OE is low, IC is enabled. If OE is high, then IC is power down and all I/Os are hi-z 12 VDD Power 3.3V +/-10% power supply 13 USB_IDB I/O USB_ID for port B 14 D-B I/O positive differential USB2.0 signal for port B 15 D+B I/O positive differential USB2.0 signal for port B 16 VDD Power 3.3V +/-10% power supply 17 USB_IDA I/O USB_ID for port A 18 D-A I/O positive differential USB2.0 signal for port A 19 D+A I/O positive differential USB2.0 signal for port A 20 VDD Power 3.3V +/-10% power supply 21 GND Ground Ground 22 Rx-B I/O negative differential USB2.0 signal for port A 23 Rx+B I/O negative differential USB3.0 Rx signal for port B 24 Tx-B I/O negative differential USB3.0 Rx signal for port B 25 Tx+B I/O positive differential USB3.0 Tx signal for port B 26 Rx-A I/O negative differential USB3.0 Tx signal for port A 27 Rx+A I/O positive differential USB3.0 Tx signal for port A 28 GND Ground Ground 29 VDD Power 3.3V +/-10% power supply 30 Tx-A I/O negative differential USB3.0 Tx signal for port A 31 Tx+A I/O positive differential USB3.0 Tx signal for port A 32 WHD Power 3.3V +/-10% power supply 33 WHD Power 3.3V +/-10% power supply 34 WHD Power 3.3V +/-10% power supply 35 WHD Power 3.3V +/-10% power supply 36 WHD Power 3.3V +/-10% power supply 37	pin#	pin Name	Signal Type	Description	
VDD	1	Tx+	I/O	positive differential USB3.0 Tx signal for COM port	
Rx+	2	Tx-	I/O	negative differential USB3.0 Tx signal for COM port	
Second Part	3	VDD	Power	3.3V +/-10% power supply	
D+	4	Rx+	I/O	positive differential USB3.0 Rx signal for COM port	
D-	5	Rx-	I/O	negative differential USB3.0 Rx signal for COM port	
8 USB_ID I/O USB_ID for COM port 9 VDD Power 3.3V +/-10% power supply 10 SS_SEL I I IfHIGH, then path B is selected for SuperSpeed channels only IfLOW, then path B is selected for SuperSpeed channels only IfLOW, then path B is selected for SuperSpeed channels only IfLOW, then path B is selected for SuperSpeed channels only IfLOW, then path B is selected for SuperSpeed channels only IfLOW, then path A is selected for SuperSpeed channels only IfLOW, then path A is selected for SuperSpeed channels only IfLOW, then path A is selected for SuperSpeed channels only IfLOW, then path A is selected for SuperSpeed channels only IfLOW, then path A is selected for SuperSpeed channels only IfLOW, then path A is selected for SuperSpeed channels only IfLOW, then path A is selected for SuperSpeed channels only IfLOW, then path A is selected for SuperSpeed channels only IfLOW is selected for SuperSpeed channels only IfLOW, then path A is selected for SuperSpeed channels only IfLOW is selected for SuperSpeed channels only IfLOW, IfLOW, then path A is selected for SuperSpeed channels only IfLOW is selected for SuperSpeed channels only IfLOW, IfLOW, then path B is selected for SuperSpeed channels only IfLOW, IfLOW, then path B is selected for SuperSpeed channels only IfLOW, Intelligence on It. IfLOW, then path B is selected for SuperSpeed channels only It. IfLOW, then path B is selected for SuperSpeed channels only It. IfLOW, Intelligence on It. IfLOW, then path B is selected for SuperSpeed channels only It. IfLOW, It. Intelligence on It. IfLOW, It. It. IfLOW, It. It. IfLOW, It.	6	D+	I/O	positive differential USB2.0 signal for COM port	
9 VDD Power 3.3V +/-10% power supply 8 switch logic control for SuperSpeed Path 10 SS_SEL I I If HIGH, then path B is selected for SuperSpeed channels only If LOW, then path A is selected for SuperSpeed channels only 11 OE I Output enable. if OE is low, IC is enabled. If OE is high, then IC is power down and all I/Os are hi-z 12 VDD Power 3.3V +/-10% power supply 13 USB_IDB I/O USB_ID for port B 14 D-B I/O negative differential USB2.0 signal for port B 15 D+B I/O positive differential USB2.0 signal for port B 16 VDD Power 3.3V +/-10% power supply 17 USB_IDA I/O USB_ID for port A 18 D-A I/O negative differential USB2.0 signal for port A 19 D+A I/O positive differential USB2.0 signal for port A 19 D+A I/O positive differential USB2.0 signal for port A 20 VDD Power 3.3V +/-10% power supply 21 GND Ground Ground 22 Rx-B I/O negative differential USB3.0 Rx signal for port B 23 Rx+B I/O positive differential USB3.0 Rx signal for port B 24 Tx-B I/O positive differential USB3.0 Tx signal for port B 25 Tx+B I/O positive differential USB3.0 Rx signal for port A 27 Rx+A I/O positive differential USB3.0 Rx signal for port A 28 GND Ground Ground 29 VDD Power 3.3V +/-10% power supply 30 Tx-A I/O negative differential USB3.0 Tx signal for port A 31 Tx+A I/O positive differential USB3.0 Tx signal for port A 32 WISB_IDA IV negative differential USB3.0 Tx signal for port A 33 Signal for port A 34 Signal for port A 35 Signal for port A 36 GND Ground Ground 37 Fx-A I/O negative differential USB3.0 Tx signal for port A 38 Signal for port A 39 VDD Power 3.3V +/-10% power supply 30 Tx-A I/O negative differential USB3.0 Tx signal for port A 31 Signal for port A 32 WISB_IDA IV NO Signal for port A 33 Signal for port A 34 Signal for port A 35 Signal for port A 36 GND Ground Ground 37 Fx-A I/O negative differential USB3.0 Tx signal for port A 39 Signal for port A	7	D-	I/O	negative differential USB2.0 signal for COM port	
switch logic control for SuperSpeed Path If HIGH, then path B is selected for SuperSpeed channels only If LOW, then path A is selected for SuperSpeed channels only Upper and being a speech of the path B is selected for SuperSpeed channels only Upper and being a speech of the path B is selected for SuperSpeed channels only Upper and being a speech of SuperSpeed channels only Upper and being a speech of SuperSpeed channels only Upper and being a speech of SuperSpeed channels only Upper and being a speech of SuperSpeed channels only Upper and being a speech of SuperSpeed channels only Upper and being a speech of SuperSpeed channels only Upper and being a speech of SuperSpeed channels only Upper and being a speech of SuperSpeed channels only Upper and being a speech of SuperSpeed channels only Upper and being a speech of SuperSpeed channels only Upper and being a speech of SuperSpeed channels only Upper and being a speech of SuperSpeed channels only Upper and being a speech of SuperSpeed channels only Upper and being a speech of SuperSpeed channels only Upper and being a speech of SuperSpeech channels only Upper and being a speech of SuperSpeech channels only Upper and being a speech of SuperSpeech channels only Upper and being a speech of SuperSpeech channels only Upper and being a speech of SuperSpeech channels only Upper and being a speech of SuperSpeech channels only Upper and being a speech of SuperSpeech channels only Upper and being a speech of SuperSpeech channels only Upper and being a speech of SuperSpeech channels only Upper and being a speech of SuperSpeech channels only Upper and being and being a speech of Superspeech of Superspeech and Upper and Up	8	USB_ID	I/O	USB_ID for COM port	
If HIGH, then path B is selected for SuperSpeed channels only If LOW, then path A is selected for SuperSpeed channels only If LOW, then path A is selected for SuperSpeed channels only If LOW, then path A is selected for SuperSpeed channels only down and all I/Os are hi-z VDD	9	VDD	Power	3.3V +/-10% power supply	
If LOW, then path A is selected for SuperSpeed channels only Output enable. if OE is low, IC is enabled. If OE is high, then IC is power down and all I/Os are hi-z VDD Power 3.3V +/-10% power supply USB_IDB I/O USB_ID for port B I/O negative differential USB2.0 signal for port B I/O positive differential USB2.0 signal for port B I/O positive differential USB2.0 signal for port B I/O USB_IDA I/O USB_ID for port A USB_IDA I/O USB_ID for port A D-A I/O negative differential USB2.0 signal for port A D-A I/O negative differential USB2.0 signal for port A D-A I/O positive differential USB2.0 signal for port A D-A I/O positive differential USB2.0 signal for port A D-A I/O positive differential USB2.0 signal for port A D-A I/O positive differential USB3.0 Rx signal for port B Rx-B I/O negative differential USB3.0 Rx signal for port B Rx+B I/O positive differential USB3.0 Tx signal for port B IX-B I/O negative differential USB3.0 Tx signal for port B Rx-A I/O negative differential USB3.0 Rx signal for port B Rx-A I/O negative differential USB3.0 Rx signal for port A Rx+A I/O positive differential USB3.0 Rx signal for port A Rx+A I/O negative differential USB3.0 Rx signal for port A Rx+A I/O positive differential USB3.0 Rx signal for port A Rx+A I/O positive differential USB3.0 Rx signal for port A Rx+A I/O positive differential USB3.0 Rx signal for port A Rx+A I/O positive differential USB3.0 Tx signal for port A Rx+A I/O negative differential USB3.0 Tx signal for port A Rx+A I/O negative differential USB3.0 Tx signal for port A I Tx+A I/O negative differential USB3.0 Tx signal for port A Switch logic control for USB2.0 (D+/-) and USB_ID path If High, path B is selected				switch logic control for SuperSpeed Path	
I Output enable. if OE is low, IC is enabled. If OE is high, then IC is power down and all I/Os are hi-z 12 VDD Power 3.3V +/-10% power supply 13 USB_IDB I/O USB_ID for port B 14 D-B I/O negative differential USB2.0 signal for port B 15 D+B I/O positive differential USB2.0 signal for port B 16 VDD Power 3.3V +/-10% power supply 17 USB_IDA I/O USB_ID for port A 18 D-A I/O negative differential USB2.0 signal for port A 19 D+A I/O positive differential USB2.0 signal for port A 19 D+A I/O positive differential USB2.0 signal for port A 20 VDD Power 3.3V +/-10% power supply 21 GND Ground Ground 22 Rx-B I/O negative differential USB3.0 Rx signal for port B 23 Rx+B I/O positive differential USB3.0 Rx signal for port B 24 Tx-B I/O negative differential USB3.0 Tx signal for port B 25 Tx+B I/O positive differential USB3.0 Tx signal for port B 26 Rx-A I/O negative differential USB3.0 Rx signal for port A 27 Rx+A I/O positive differential USB3.0 Rx signal for port A 28 GND Ground Ground 29 VDD Power 3.3V +/-10% power supply 30 Tx-A I/O negative differential USB3.0 Tx signal for port A 31 Tx+A I/O positive differential USB3.0 Tx signal for port A 32 witch logic control for USB2.0 (D+/-) and USB_ID path	10	SS_SEL	I		
USB_IDB I/O USB_ID for port B 14 D-B I/O negative differential USB2.0 signal for port B 15 D+B I/O positive differential USB2.0 signal for port B 16 VDD Power 3.3V +/-10% power supply 17 USB_IDA I/O USB_ID for port A 18 D-A I/O negative differential USB2.0 signal for port A 19 D+A I/O positive differential USB2.0 signal for port A 20 VDD Power 3.3V +/-10% power supply 21 GND Ground Ground 22 Rx-B I/O negative differential USB3.0 Rx signal for port B 23 Rx+B I/O positive differential USB3.0 Rx signal for port B 24 Tx-B I/O negative differential USB3.0 Tx signal for port B 25 Tx+B I/O positive differential USB3.0 Tx signal for port B 26 Rx-A I/O negative differential USB3.0 Rx signal for port A 27 Rx+A I/O positive differential USB3.0 Rx signal for port A 28 GND Ground Ground 29 VDD Power 3.3V +/-10% power supply 30 Tx-A I/O negative differential USB3.0 Tx signal for port A 31 Tx+A I/O positive differential USB3.0 Tx signal for port A 32 WHS_SEL I I If High, path B is selected	11	ŌĒ	I		
14 D-B I/O negative differential USB2.0 signal for port B 15 D+B I/O positive differential USB2.0 signal for port B 16 VDD Power 3.3V +/-10% power supply 17 USB_IDA I/O USB_ID for port A 18 D-A I/O negative differential USB2.0 signal for port A 19 D+A I/O positive differential USB2.0 signal for port A 20 VDD Power 3.3V +/-10% power supply 21 GND Ground Ground 22 Rx-B I/O negative differential USB3.0 Rx signal for port B 23 Rx+B I/O positive differential USB3.0 Rx signal for port B 24 Tx-B I/O negative differential USB3.0 Tx signal for port B 25 Tx+B I/O positive differential USB3.0 Tx signal for port B 26 Rx-A I/O negative differential USB3.0 Rx signal for port A 27 Rx+A I/O positive differential USB3.0 Rx signal for port A 28 GND Ground Ground 29 VDD Power 3.3V +/-10% power supply 30 Tx-A I/O negative differential USB3.0 Tx signal for port A 31 Tx+A I/O positive differential USB3.0 Tx signal for port A 32 switch logic control for USB2.0 (D+/-) and USB_ID path 33 HS_SEL I If High, path B is selected	12	VDD	Power	3.3V +/-10% power supply	
14 D-B I/O negative differential USB2.0 signal for port B 15 D+B I/O positive differential USB2.0 signal for port B 16 VDD Power 3.3V +/-10% power supply 17 USB_IDA I/O USB_ID for port A 18 D-A I/O negative differential USB2.0 signal for port A 19 D+A I/O positive differential USB2.0 signal for port A 20 VDD Power 3.3V +/-10% power supply 21 GND Ground Ground 22 Rx-B I/O negative differential USB3.0 Rx signal for port B 23 Rx+B I/O positive differential USB3.0 Rx signal for port B 24 Tx-B I/O negative differential USB3.0 Tx signal for port B 25 Tx+B I/O positive differential USB3.0 Tx signal for port B 26 Rx-A I/O negative differential USB3.0 Rx signal for port A 27 Rx+A I/O positive differential USB3.0 Rx signal for port A 28 GND Ground Ground 29 VDD Power 3.3V +/-10% power supply 30 Tx-A I/O negative differential USB3.0 Tx signal for port A 31 Tx+A I/O positive differential USB3.0 Tx signal for port A 32 switch logic control for USB2.0 (D+/-) and USB_ID path 33 HS_SEL I If High, path B is selected	13	USB_IDB	I/O	USB_ID for port B	
16 VDD Power 3.3V +/-10% power supply 17 USB_IDA I/O USB_ID for port A 18 D-A I/O negative differential USB2.0 signal for port A 19 D+A I/O positive differential USB2.0 signal for port A 20 VDD Power 3.3V +/-10% power supply 21 GND Ground Ground 22 Rx-B I/O negative differential USB3.0 Rx signal for port B 23 Rx+B I/O positive differential USB3.0 Rx signal for port B 24 Tx-B I/O negative differential USB3.0 Tx signal for port B 25 Tx+B I/O positive differential USB3.0 Tx signal for port B 26 Rx-A I/O negative differential USB3.0 Rx signal for port A 27 Rx+A I/O positive differential USB3.0 Rx signal for port A 28 GND Ground Ground 29 VDD Power 3.3V +/-10% power supply 30 Tx-A I/O negative differential USB3.0 Tx signal for port A 31 Tx+A I/O positive differential USB3.0 Tx signal for port A 32 HS_SEL I I If High, path B is selected	14	D-B	I/O	negative differential USB2.0 signal for port B	
17 USB_IDA I/O USB_ID for port A 18 D-A I/O negative differential USB2.0 signal for port A 19 D+A I/O positive differential USB2.0 signal for port A 20 VDD Power 3.3V +/-10% power supply 21 GND Ground Ground 22 Rx-B I/O negative differential USB3.0 Rx signal for port B 23 Rx+B I/O positive differential USB3.0 Rx signal for port B 24 Tx-B I/O negative differential USB3.0 Tx signal for port B 25 Tx+B I/O positive differential USB3.0 Tx signal for port B 26 Rx-A I/O negative differential USB3.0 Rx signal for port A 27 Rx+A I/O positive differential USB3.0 Rx signal for port A 28 GND Ground Ground 29 VDD Power 3.3V +/-10% power supply 30 Tx-A I/O negative differential USB3.0 Tx signal for port A 31 Tx+A I/O positive differential USB3.0 Tx signal for port A 32 HS_SEL I I If High, path B is selected	15	D+B	I/O	· ·	
D-A I/O negative differential USB2.0 signal for port A 19 D+A I/O positive differential USB2.0 signal for port A 20 VDD Power 3.3V +/-10% power supply 21 GND Ground Ground 22 Rx-B I/O negative differential USB3.0 Rx signal for port B 23 Rx+B I/O positive differential USB3.0 Rx signal for port B 24 Tx-B I/O negative differential USB3.0 Tx signal for port B 25 Tx+B I/O positive differential USB3.0 Tx signal for port B 26 Rx-A I/O negative differential USB3.0 Rx signal for port A 27 Rx+A I/O positive differential USB3.0 Rx signal for port A 28 GND Ground Ground 29 VDD Power 3.3V +/-10% power supply 30 Tx-A I/O negative differential USB3.0 Tx signal for port A 31 Tx+A I/O positive differential USB3.0 Tx signal for port A 32 WSB2L I If High, path B is selected	16	VDD	Power	· · · · · · · · · · · · · · · · · · ·	
19 D+A I/O positive differential USB2.0 signal for port A 20 VDD Power 3.3V +/-10% power supply 21 GND Ground Ground 22 Rx-B I/O negative differential USB3.0 Rx signal for port B 23 Rx+B I/O positive differential USB3.0 Rx signal for port B 24 Tx-B I/O negative differential USB3.0 Tx signal for port B 25 Tx+B I/O positive differential USB3.0 Tx signal for port B 26 Rx-A I/O negative differential USB3.0 Rx signal for port A 27 Rx+A I/O positive differential USB3.0 Rx signal for port A 28 GND Ground Ground 29 VDD Power 3.3V +/-10% power supply 30 Tx-A I/O negative differential USB3.0 Tx signal for port A 31 Tx+A I/O positive differential USB3.0 Tx signal for port A 32 HS_SEL I I If High, path B is selected	17	USB_IDA	I/O	2 22 1	
VDD Power 3.3V +/-10% power supply GND Ground Ground Rx-B I/O negative differential USB3.0 Rx signal for port B Tx-B I/O negative differential USB3.0 Tx signal for port B Tx-B I/O positive differential USB3.0 Tx signal for port B Tx+B I/O positive differential USB3.0 Tx signal for port B Rx-A I/O positive differential USB3.0 Rx signal for port A Rx+A I/O negative differential USB3.0 Rx signal for port A Rx+A I/O positive differential USB3.0 Rx signal for port A GND Ground Ground Ground Tx-A I/O negative differential USB3.0 Tx signal for port A I Tx+A I/O positive differential USB3.0 Tx signal for port A Switch logic control for USB2.0 (D+/-) and USB_ID path If High, path B is selected	18	D-A	I/O	-	
GND Ground Ground Rx-B I/O negative differential USB3.0 Rx signal for port B Rx+B I/O positive differential USB3.0 Rx signal for port B I/O negative differential USB3.0 Tx signal for port B I/O negative differential USB3.0 Tx signal for port B I/O positive differential USB3.0 Tx signal for port B Rx-B I/O positive differential USB3.0 Rx signal for port B Rx-A I/O negative differential USB3.0 Rx signal for port A Rx+A I/O positive differential USB3.0 Rx signal for port A GND Ground Ground Ground YDD Power 3.3V +/-10% power supply Tx-A I/O negative differential USB3.0 Tx signal for port A I/O positive differential USB3.0 Tx signal for port A When the power of the power of the power supply and the power of the po	19	D+A	I/O	positive differential USB2.0 signal for port A	
22 Rx-B I/O negative differential USB3.0 Rx signal for port B 23 Rx+B I/O positive differential USB3.0 Rx signal for port B 24 Tx-B I/O negative differential USB3.0 Tx signal for port B 25 Tx+B I/O positive differential USB3.0 Tx signal for port B 26 Rx-A I/O negative differential USB3.0 Rx signal for port A 27 Rx+A I/O positive differential USB3.0 Rx signal for port A 28 GND Ground Ground 29 VDD Power 3.3V +/-10% power supply 30 Tx-A I/O negative differential USB3.0 Tx signal for port A 31 Tx+A I/O positive differential USB3.0 Tx signal for port A 32 switch logic control for USB2.0 (D+/-) and USB_ID path 33 If HS_SEL I If High, path B is selected	20	VDD	Power	3.3V +/-10% power supply	
23 Rx+B I/O positive differential USB3.0 Rx signal for port B 24 Tx-B I/O negative differential USB3.0 Tx signal for port B 25 Tx+B I/O positive differential USB3.0 Tx signal for port B 26 Rx-A I/O negative differential USB3.0 Rx signal for port A 27 Rx+A I/O positive differential USB3.0 Rx signal for port A 28 GND Ground Ground 29 VDD Power 3.3V +/-10% power supply 30 Tx-A I/O negative differential USB3.0 Tx signal for port A 31 Tx+A I/O positive differential USB3.0 Tx signal for port A 32 switch logic control for USB2.0 (D+/-) and USB_ID path 33 If HS_SEL I If High, path B is selected	21	GND	Ground	Ground	
Tx-B I/O negative differential USB3.0 Tx signal for port B Tx+B I/O positive differential USB3.0 Tx signal for port B Rx-A I/O negative differential USB3.0 Rx signal for port A Rx+A I/O positive differential USB3.0 Rx signal for port A Ground Ground Ground VDD Power 3.3V +/-10% power supply Tx-A I/O negative differential USB3.0 Tx signal for port A Tx+A I/O positive differential USB3.0 Tx signal for port A Witch logic control for USB3.0 Tx signal for port A switch logic control for USB2.0 (D+/-) and USB_ID path If High, path B is selected	22	Rx-B	I/O	negative differential USB3.0 Rx signal for port B	
Tx+B I/O positive differential USB3.0 Tx signal for port B Rx-A I/O negative differential USB3.0 Rx signal for port A Rx+A I/O positive differential USB3.0 Rx signal for port A Rx+A I/O positive differential USB3.0 Rx signal for port A Rx+A I/O positive differential USB3.0 Tx signal for port A Tx-A I/O negative differential USB3.0 Tx signal for port A Tx+A I/O positive differential USB3.0 Tx signal for port A switch logic control for USB2.0 (D+/-) and USB_ID path If High, path B is selected	23	Rx+B	I/O	positive differential USB3.0 Rx signal for port B	
Rx-A I/O negative differential USB3.0 Rx signal for port A Rx+A I/O positive differential USB3.0 Rx signal for port A Rx+A I/O positive differential USB3.0 Rx signal for port A Rx+A I/O Ground Ground Power 3.3V +/-10% power supply Tx-A I/O negative differential USB3.0 Tx signal for port A Tx+A I/O positive differential USB3.0 Tx signal for port A switch logic control for USB2.0 (D+/-) and USB_ID path If High, path B is selected	24	Tx-B	I/O	negative differential USB3.0 Tx signal for port B	
27 Rx+A I/O positive differential USB3.0 Rx signal for port A 28 GND Ground Ground 29 VDD Power 3.3V +/-10% power supply 30 Tx-A I/O negative differential USB3.0 Tx signal for port A 31 Tx+A I/O positive differential USB3.0 Tx signal for port A 32 switch logic control for USB2.0 (D+/-) and USB_ID path 33 If High, path B is selected	25	Tx+B	I/O	positive differential USB3.0 Tx signal for port B	
28 GND Ground Ground 29 VDD Power 3.3V +/-10% power supply 30 Tx-A I/O negative differential USB3.0 Tx signal for port A 31 Tx+A I/O positive differential USB3.0 Tx signal for port A 32 SEL I If High, path B is selected	26	Rx-A	I/O	negative differential USB3.0 Rx signal for port A	
29 VDD Power 3.3V +/-10% power supply 30 Tx-A I/O negative differential USB3.0 Tx signal for port A 31 Tx+A I/O positive differential USB3.0 Tx signal for port A switch logic control for USB2.0 (D+/-) and USB_ID path If High, path B is selected	27	Rx+A	I/O	positive differential USB3.0 Rx signal for port A	
30 Tx-A I/O negative differential USB3.0 Tx signal for port A 31 Tx+A I/O positive differential USB3.0 Tx signal for port A switch logic control for USB2.0 (D+/-) and USB_ID path If High, path B is selected	28	GND	Ground	Ground	
31 Tx+A I/O positive differential USB3.0 Tx signal for port A switch logic control for USB2.0 (D+/-) and USB_ID path If High, path B is selected	29	VDD	Power	3.3V +/-10% power supply	
switch logic control for USB2.0 (D+/-) and USB_ID path If High, path B is selected	30	Tx-A	I/O	negative differential USB3.0 Tx signal for port A	
32 HS_SEL I If High, path B is selected	31	Tx+A	I/O	positive differential USB3.0 Tx signal for port A	
				switch logic control for USB2.0 (D+/-) and USB_ID path	
If LOW, path A is selected	32	HS_SEL	I	If High, path B is selected	
				If LOW, path A is selected	



Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-0.5V to +4.2V -0.5V to V _{DD}
DC Output Current	
Power Dissipation	0.5W

Note: Stresses greater than those listed under MAXI-MUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics for Switching over Operating Range

 $(TA = -40^{\circ}C \text{ to } +85^{\circ}C, VDD = 3.3V \pm 10\%)$

Parameter	Description	Test Conditions(1)	Min	Typ(1)	Max	Units
V _{IH}	Input HIGH Voltage	Guaranteed HIGH level	1.5			
v_{IL}	Input LOW Voltage	Guaranteed LOW level			0.75	V
V _{IK}	Clamp Diode Voltage, Dx	$V_{\mathrm{DD}} = \mathrm{Max.}$, $I_{\mathrm{IN}} = -18\mathrm{mA}$		-0.8	-1.1	
IIH	Input HIGH Current	$V_{DD} = Max., V_{IN} = V_{DD}$			±5	
I_{IL}	Input LOW Current	$V_{DD} = Max., V_{IN} = GND$			±5	μΑ
I _{OFF_HS/ID}	I/O leakage when part is off for D+, D- and USB_ID signals only	$V_{DD} = 0V$, $V_{INPUT} = 0V$ to 3.6V			20	
R _{ON_SS}	On resistance between input to output for SuperSpeed signals	$V_{\rm DD}$ = 3.3V, Vinput = 0V to 1V, $I_{\rm INPUT}$ = 20mA		10	13	Ohm
R _{ON_FS}	On resistance between input to output for USB2.0 FS signals (D+/D-)	V_{DD} = 3.3V, Vinput = 0 to 3.3V, I_{INPUT} = 20mA		7	9	Ohm
R _{ON_HS}	On resistance between input to output for USB2.0 HS signals (D+/D-)	V _{DD} = 3.3V, Vinput = -0.4V to +0.4V, I _{INPUT} = 20mA		4	6	Ohm
USB_ID_I	Input voltage tolerance on USB_ID path				5.5	V
USB_ID_O	Output voltage on USB_ID path	USB_ID input from 0V to 5.25V			3.6	V

Power Supply Characteristics (TA = -40°C to +85°C)

Parameter	Description	Test Conditions ⁽¹⁾	Min	Typ ⁽¹⁾	Max	Units
I_{CC}	Quiescent Power Supply Current	V_{DD} = Max., V_{IN} = GND or V_{DD}			2	mA



Dynamic Electrical Characteristics over Operating Range (TA = -40° to $+85^{\circ}$ C, VDD = 3.3V $\pm 10\%$)

Parameter	Description	Test Conditions		Тур.	Max	Units
X _{TALK}	Crosstalk on SuperSpeed Channels	See Fig. 1 for Measurement Setup f= 2.5 GHz		-25dB		1D
O _{IRR}	OFF Isolation on SuperSpeed Channels	See Fig. 2 for Measurement Setup, f= 2.5 GHz		-22dB		dB
I_{LOSS}	Differential Insertion Loss on SuperSpeed Channels	@5.0Gbps (see figure 3)		-1.7		dB
R _{loss}	Differential Return Loss on SuperSpeed channels	@ 2.5GHz		-16		dB
BW_SS	Bandwidth -3dB for SuperSpeed path (Tx±/ Rx±)	See figure 3		4.7		GHz
BW_HS	-3dB BW for USB high speed path (D+/-)	See figure 3		1.5		GHz
Tsw a-b	time it takes to switch from port A to port B				1	us
Tsw b-a	time it takes to switch from port B to port A				1	us
Tstartup	Vdd valid to channel enable				10	us
Twakeup	Enabling output by changing \overline{OE} from low to High				10	us

^{1.} For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.

Switching Characteristics (T_A= -40° to +85°C, $V_{DD}=3.3V\pm10\%$)

Parameter	Description		Тур.	Max.	Units
T _{pd}	Propagation delay (input pin to output pin)		80		ps
t _{b-b}	Bit-to-bit skew within the same differential pair		5		ps
t _{ch-ch}	Channel-to-channel skew			35	ps

^{2.} Typical values are at $V_{\rm DD}$ = 3.3V, $T_{\rm A}$ = 25°C ambient and maximum loading.



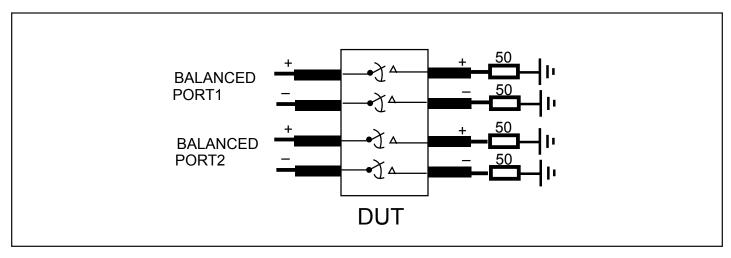


Fig 1. Crosstalk Setup

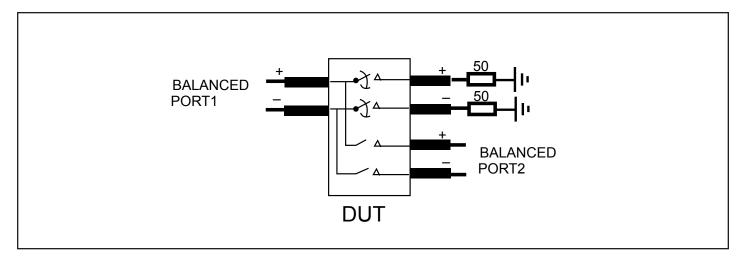


Fig 2. Off-isolation setup

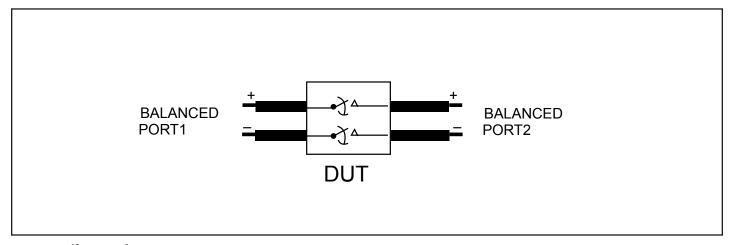


Fig 3. Differential Insertion Loss set up



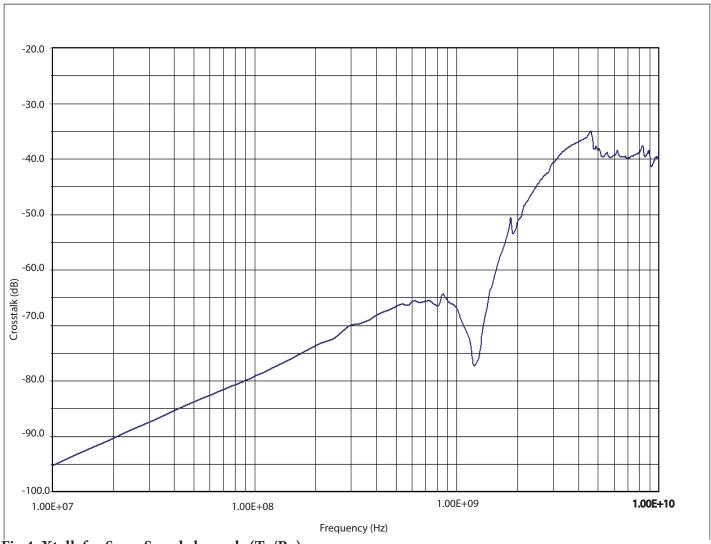


Fig 4. Xtalk for SuperSpeed channels (Tx/Rx)



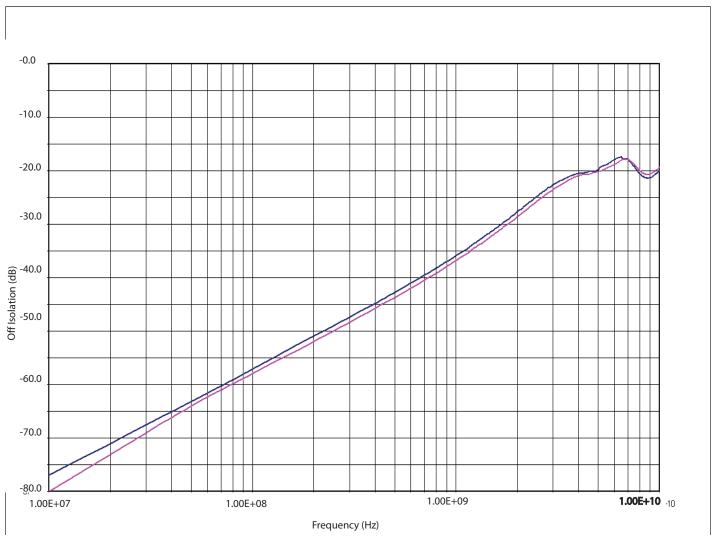


Fig 5. Off Isolation for SuperSpeed channels (Tx/Rx). Red is for path B and Blue is for path A



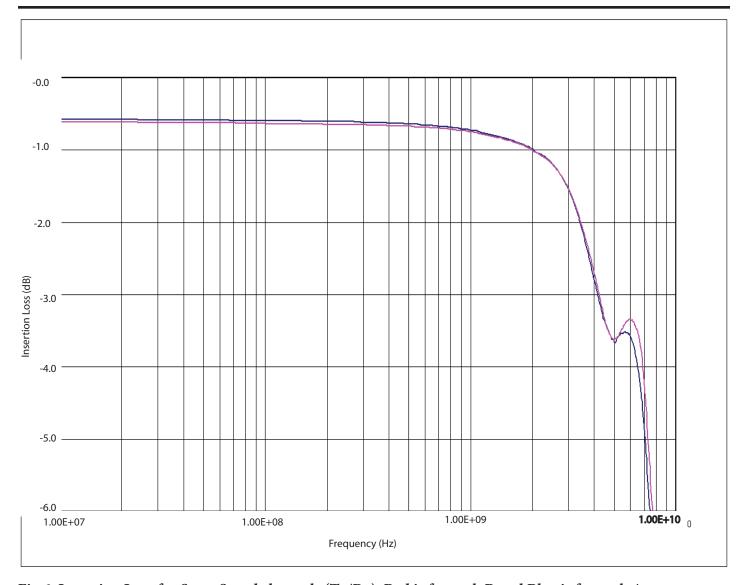
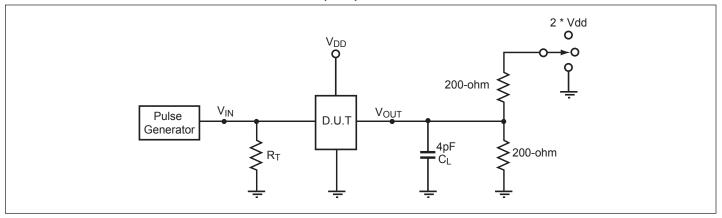


Fig 6. Insertion Loss for SuperSpeed channels (Tx/Rx). Red is for path B and Blue is for path A



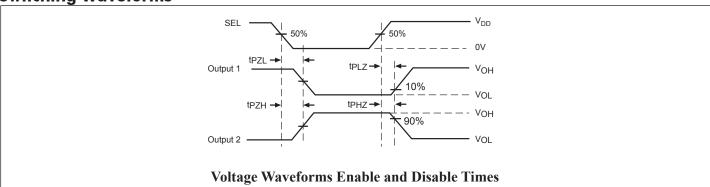
Test Circuit for Electrical Characteristics(1-5)



Notes:

- 1. C_L = Load capacitance: includes jig and probe capacitance.
- 2. R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator
- 3. Output 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
- 4. Output 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- 5. All input impulses are supplied by generators having the following characteristics: $PRR \leq MHz, Z_O = 50\Omega, t_R \leq 2.5 ns, t_F \leq 2.5 ns.$
- 6. The outputs are measured one at a time with one transition per measurement.

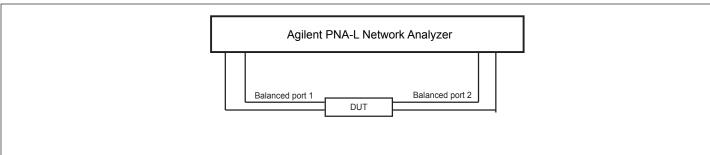
Switching Waveforms



Switch Positions

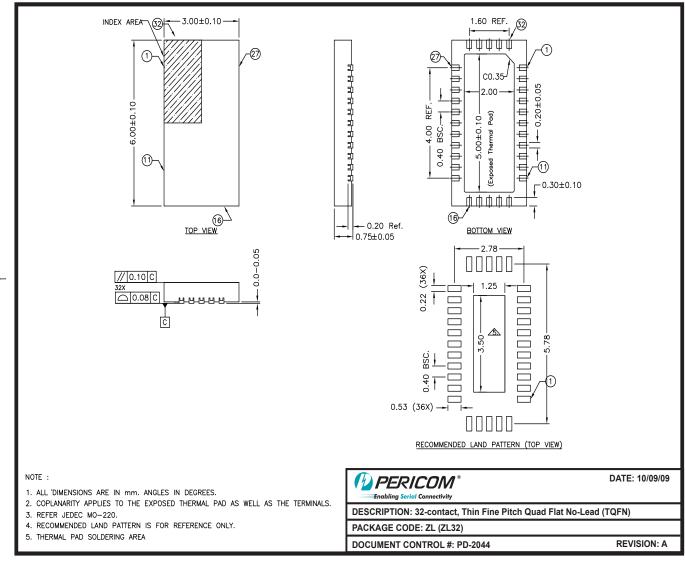
Test	Switch
t _{PLZ} , t _{PZL} (output on B-side)	2 * Vdd
t _{PHZ} , t _{PZH} (output on B-side)	GND
Prop Delay	Open

Test Circuit for Dynamic Electrical Characteristics





Packaging Mechanical: 32-Contact TQFN (ZL)



09-0125

Note:

For latest package info, please check: http://www.pericom.com/products/packaging/mechanicals.php

Ordering Information

Ordering Code	Package Code	Package Description		
PI3USB3102ZLE	ZL	Pb-free & Green, 32-contact TQFN, Copper Wire		
PI3USB3102ZLE+DA	ZL	Pb-free & Green, 32-contact TQFN, Gold Wire		

Notes

- $\bullet \ \ Thermal\ characteristics\ can\ be\ found\ on\ the\ company\ web\ site\ at\ www.pericom.com/packaging/$
- "E" denotes Pb-free and Green
- Adding an "X" at the end of the ordering code denotes tape and reel packaging