2:1 LVDS Multiplexer With 1:2 Fanout and Internal Termination

889474

DATA SHEET

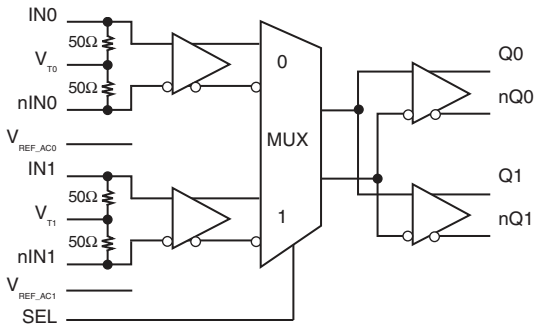
General Description

The 889474 is a high speed 2-to-1 differential multiplexer with integrated 2 output LVDS fanout buffer and internal termination and is a member of the family of high performance clock solutions from IDT. The 889474 is optimized for high speed and very low output skew, making it suitable for use in demanding applications such as SONET, 1 Gigabit and 10 Gigabit Ethernet, and Fibre Channel. The internally terminated differential input and V_{REF_AC} pins allow other differential signal families such as LVPECL, LVDS, LVHSTL and CML to be easily interfaced to the input with minimal use of external components. The 889474 is packaged in a small 4mm x 4mm 24-pin VFQFN package which makes it ideal for use in space-constrained applications.

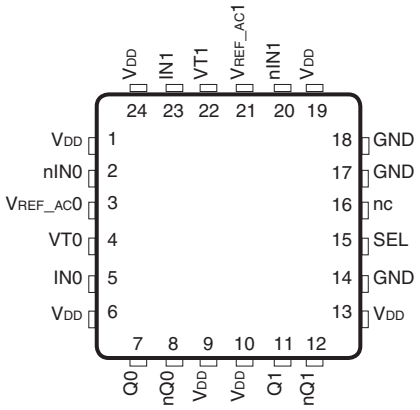
Features

- Two differential LVDS outputs
- INx, nINx pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, CML
- 50Ω internal input termination to V_T
- Maximum output frequency: 2GHz (maximum)
- Additive phase jitter, RMS: 0.06ps (typical)
- Output skew: 20ps (maximum)
- Propagation delay: 700ps (maximum)
- 2.5V operating supply
- -40°C to 85°C ambient operating temperature
- Available in lead-free RoHS-complaint package

Block Diagram



Pin Assignment



889474
24-Lead VFQFN
4mm x 4mm x 0.925mm package body
K Package
Top View

© 2019 Renesas Electronics Corporation

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 6, 9, 10, 13, 19, 24	V_{DD}	Power		Positive supply pins.
2, 20	nIN0, nIN1	Input		Inverting differential clock inputs. 50Ω internal input termination to V_T.
3, 21	V_{REF_AC0}, V_{REF_AC1}	Output		Reference voltage for AC-coupled applications.
4, 22	V_{T0}, V_{T1}	Input		Termination inputs.
5, 23	IN0, IN1	Input		Non-inverting differential clock inputs. 50Ω internal input termination to V_T.
7, 8	Q0, nQ0	Output		Differential output pair. LVDS interface levels.
11, 12	Q1, nQ1	Output		Differential output pair. LVDS interface levels.
14, 17, 18	GND	Power		Power supply ground.
15	SEL	Input	Pullup	Input select pin. LVCMOS/LVTTL interface levels.
16	nc	Unused		No connect.

NOTE: *Pullup* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
R_{PULLUP}	Input Pullup Resistor			25		kΩ

Table 3. Truth Table

Inputs					Outputs	
IN0	nIN0	IN1	nIN1	SEL	Q0:Q1	nQ0:nQ1
0	1	X	X	0	0	1
1	0	X	X	0	1	0
X	X	0	1	1	0	1
X	X	1	0	1	1	0

© 2019 Renesas Electronics Corporation

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, I_O (LVDS)	
Continuous Current	10mA
Surge Current	15mA
Input Current, INx, nINx	±50mA
V_T Current, I_{VT}	±100mA
Input Sink/Source, I_{REF_AC}	± 0.5mA
Operating Temperature Range, T_A	-40°C to +85°C
Storage Temperature, T_{STG}	-65°C to 150°C
Package Thermal Impedance, θ_{JA} (Junction-to-Ambient)	49.5°C/W (0 mps)

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, V_{DD} = 2.5V ± 5%; TA = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				80	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{DD} = 2.5V ± 5%; TA = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		0		0.7	V
I_{IH}	Input High Current	V_{DD} = V_{IN} = 2.625V			5	µA
I_{IL}	Input Low Current	V_{DD} = 2.625V, V_{IN} = 0V	-150			µA

Table 4C. Differential DC Characteristics, V_{DD} = 2.5V ± 5%; TA = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
R_{IN}	Input Resistance	IN-to-V_T	IN-to-VT	45	50	55	Ω
R_{DIFF_IN}	Differential Input Resistance	INx, nINx		90	100	110	Ω
V_{IH}	Input High Voltage	INx, nINx		1.2		V_{DD}	V
V_{IL}	Input Low Voltage	INx, nINx		0		V_{IN} – 0.1	V
V_{IN}	Input Voltage Swing	INx, nINx		0.1		V_{DD}	V
V_{DIFF_IN}	Differential Input Voltage Swing	INx, nINx		0.2			V
V_{T_IN}	IN-to-V_T	INx, nINx				1.28	V
V_{REF_AC}	Output Reference Voltage			V_{DD} – 1.4	V_{DD} – 1.3	V_{DD} – 1.2	V

© 2019 Renesas Electronics Corporation

TABLE 4D. LVDS DC CHARACTERISTICS, V_{DD} = 2.5V ± 5%; TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OUT}	Output Voltage Swing		340	400		mV
V_{DIFF_OUT}	Differential Output Voltage Swing		680	800		mV
V_{OCM}	Output Common Mode Voltage		1.10		1.35	V
ΔV_{OCM}	Change in Common Mode Voltage		-50		50	mV

TABLE 5. AC CHARACTERISTICS, V_{DD} = 2.5V ± 5%; TA = -40°C TO 85°C

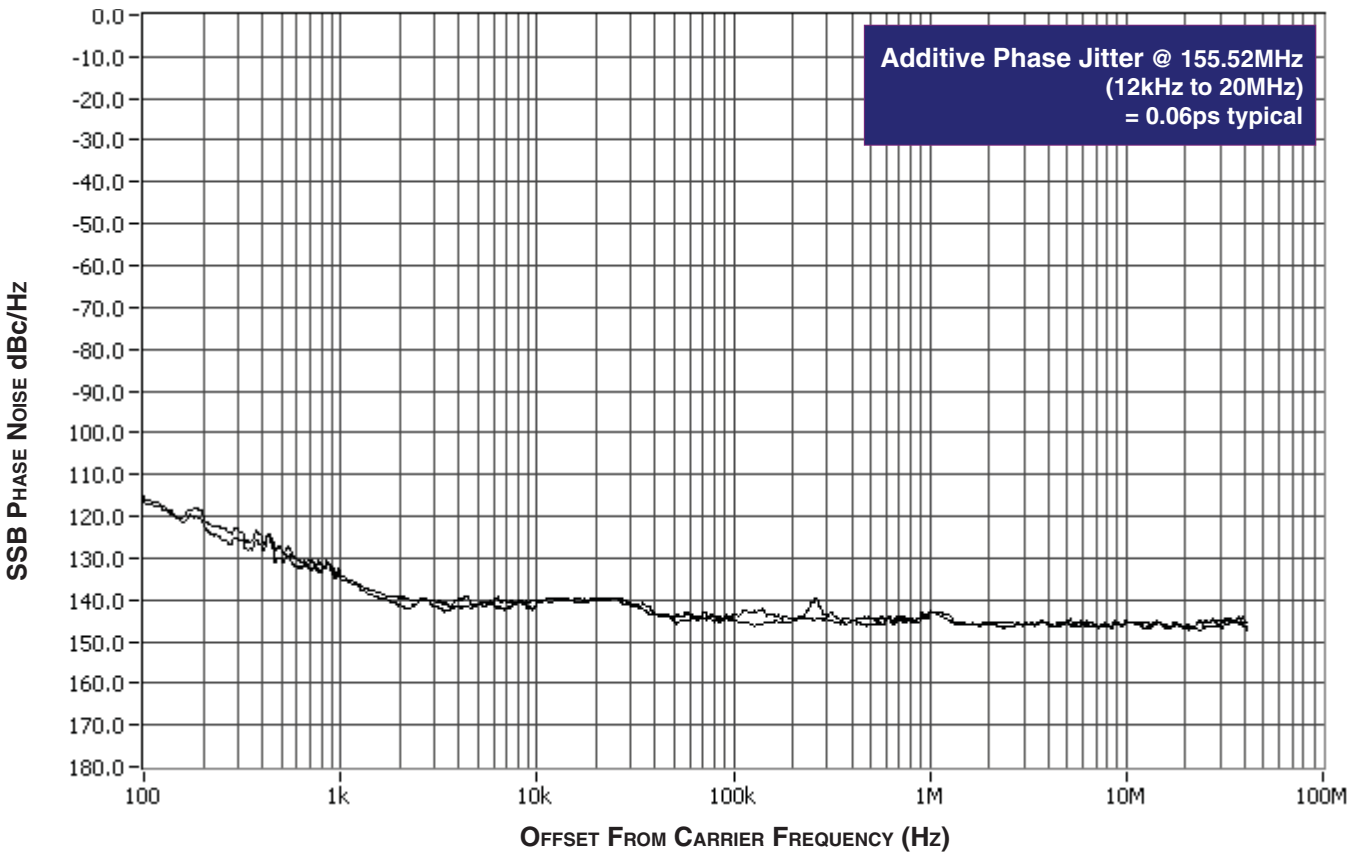
Symbol	Parameter		Condition	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency					4	Gpbs
		Q0:1/nQ0:1				2	GHz
t_{PD}	Propagation Delay, (Differential); NOTE 1	IN-to-Q		400		700	ps
		SEL-to-Q		250		600	ps
tsk(o)	Output Skew; NOTE 2, 4					20	ps
tsk(pp)	Part-to-Part Skew; NOTE 3, 4					200	ps
tjit	Buffer Additive Phase Jitter, RMS; Refer to Additive Phase Jitter Section, NOTE 5		155.52MHz, 12kHz – 20MHz		0.06		ps
$MUX\_{ISOLATION}$	Mux Isolation				55		dB
t_R/t_F	Output Rise/Fall Time		20% to 80%	70		220	ps

NOTE: All parameters are characterized at ≤ 1GHz unless otherwise noted.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 5: Driving only one input clock.

© 2019 Renesas Electronics Corporation

Additive Phase Jitter

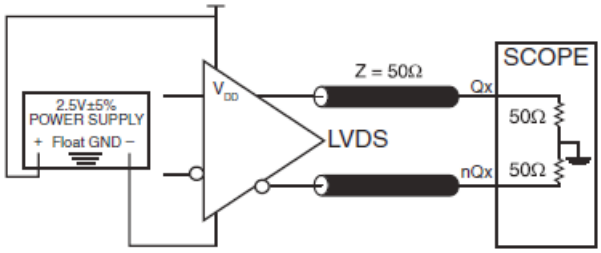
The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



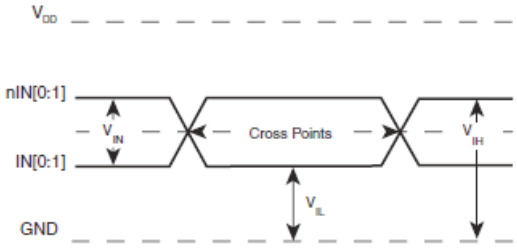
As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

© 2019 Renesas Electronics Corporation

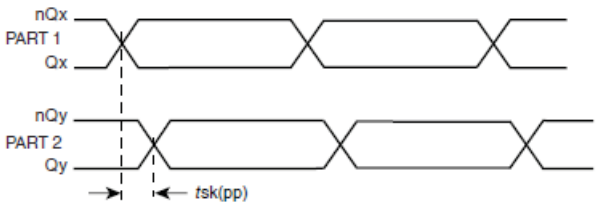
PARAMETER MEASUREMENT INFORMATION



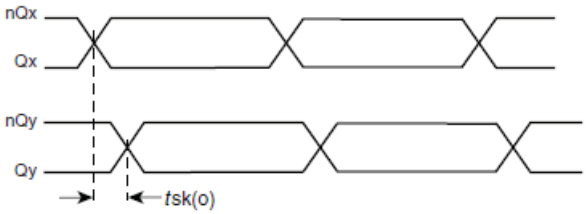
OUTPUT LOAD AC TEST CIRCUIT



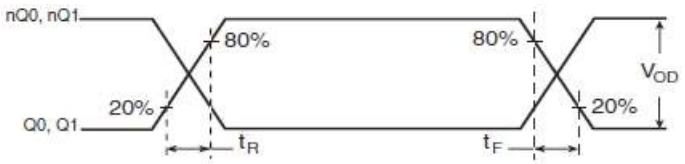
DIFFERENTIAL INPUT LEVEL



PART-TO-PART SKEW



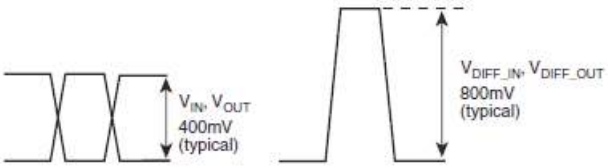
OUTPUT SKEW



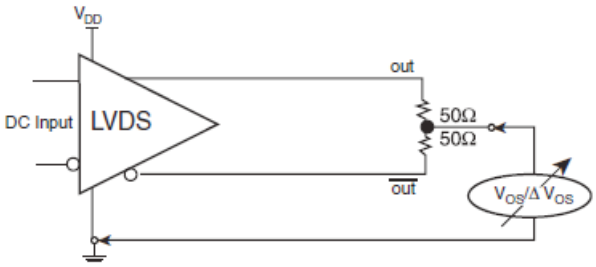
OUTPUT RISE/FALL TIME

PROPAGATION DELAY

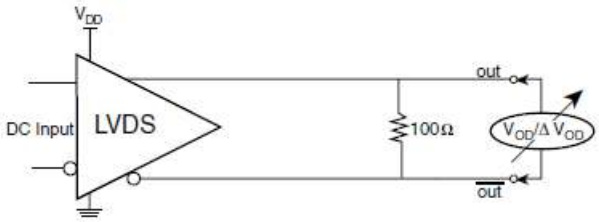
© 2019 Renesas Electronics Corporation



Single Ended & Differential Input Voltage Swing



Offset Voltage Setup



Differential Output Voltage Setup

© 2019 Renesas Electronics Corporation

Application Information

LVPECL Input with Built-In 50Ω Terminations Interface

The IN /nIN with built-in 50Ω terminations accepts LVDS, LVPECL, CML and other differential signals. The signal must meet the V_{PP} and V_{CMR} input requirements. *Figures 1A to 1E* show interface examples for the HiPerClockS IN/nIN input with built-in 50Ω terminations driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

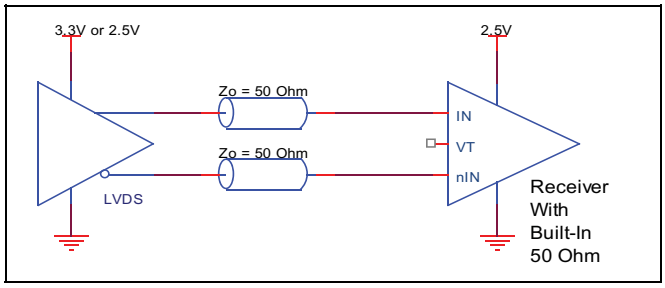


Figure 1A. HiPerClockS IN/nIN Input with Built-in 50Ω Driven by an LVDS Driver

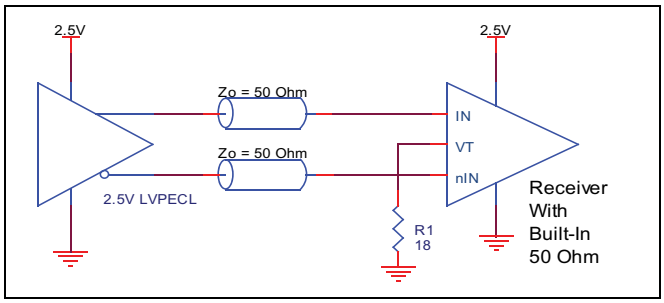


Figure 1B. HiPerClockS IN/nIN Input with Built-in 50Ω Driven by an LVPECL Driver

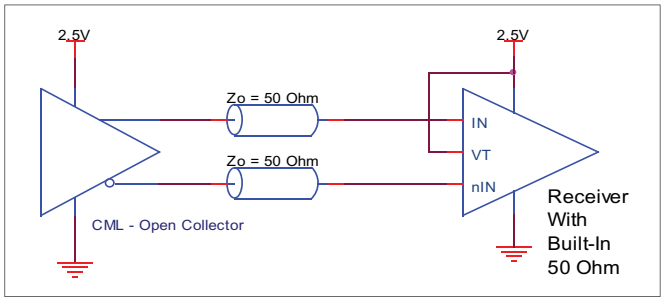


Figure 1C. HiPerClockS IN/nIN Input with Built-in 50Ω Driven by a CML Driver

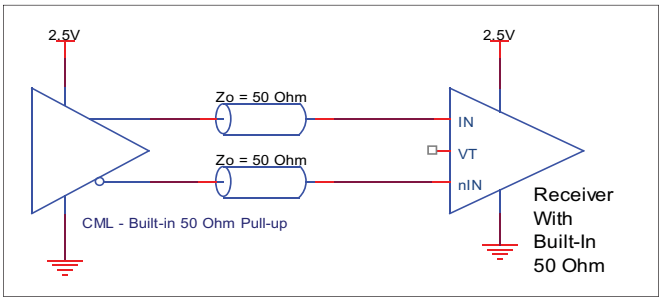


Figure 1D. HiPerClockS IN/nIN Input with Built-in 50Ω Driven by a CML Driver with Built-In 50Ω Pullup

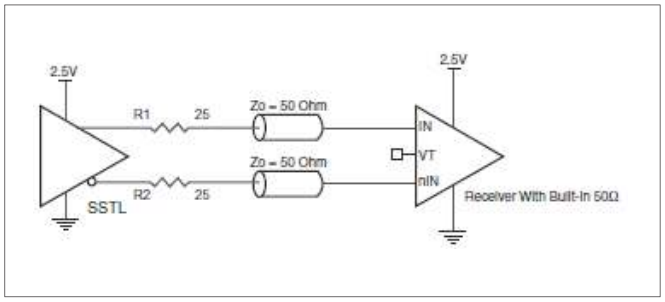


Figure 1E. HiPerClockS IN/nIN Input with Built-in 50Ω Driven by an SSTL Driver

© 2019 Renesas Electronics Corporation

Recommendations for Unused Output Pins

Inputs:

IN/nIN Inputs

For applications not requiring the use of the differential input, both IN and nIN can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from IN to ground.

Outputs:

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

2.5V LVDS Driver Termination

Figure 2 shows a typical termination for LVDS driver in characteristic impedance of 100Ω differential (50Ω single) transmission line environment. For buffer with multiple LVDS driver, it is recommended to terminate the unused outputs.

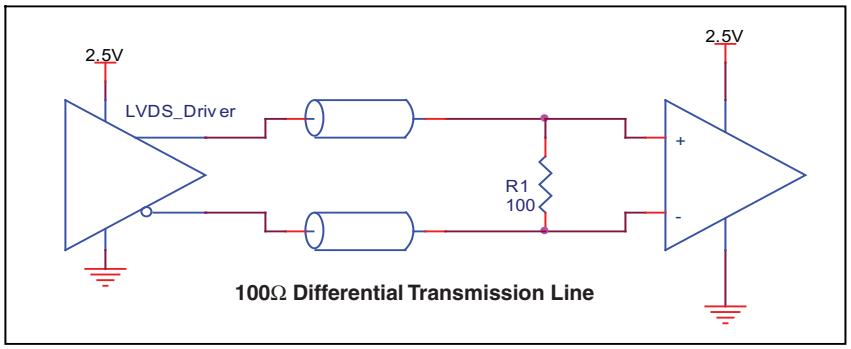


Figure 2. Typical LVDS Driver Termination

2.5V Differential Input with Built-In 50Ω Termination Unused Input Handling

To prevent oscillation and to reduce noise, it is recommended to have pull up and pull down connect to true and compliment of the unused input as shown in *Figure 3.*

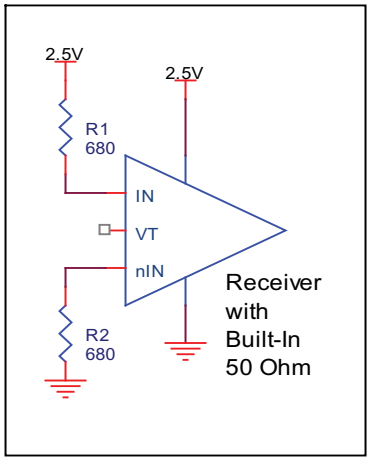


Figure 3. Unused Input Handling

© 2019 Renesas Electronics Corporation

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/ shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as "heat pipes". The number of vias (i.e. "heat pipes") are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor's Thermally/Electrically Enhance Leadfame Base Package, Amkor Technology.

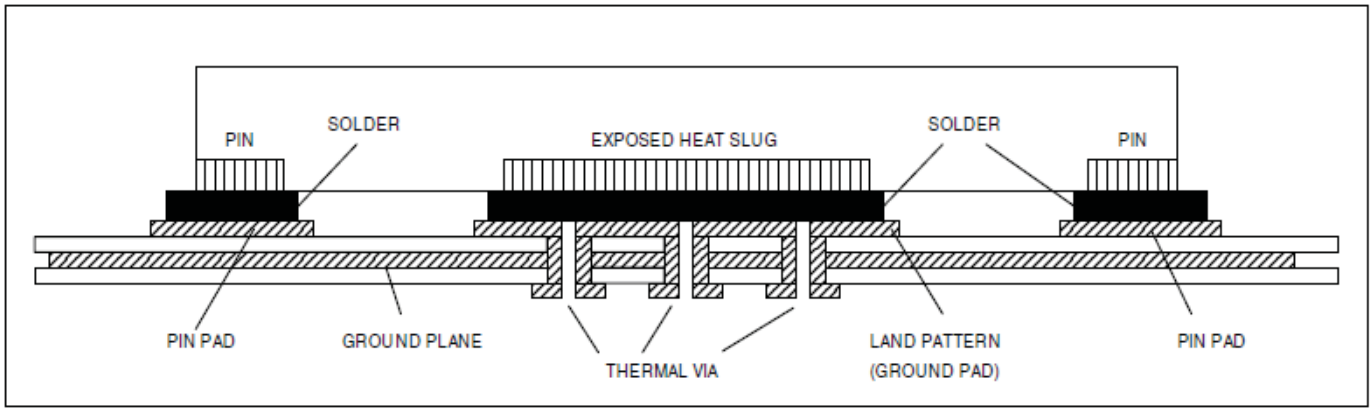


Figure 4. P.C.Assembly for Exposed Pad Thermal Release Path –Side View (Drawing not to Scale)

© 2019 Renesas Electronics Corporation

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the 889474.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the 889474 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 2.625V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{DD_MAX} * I_{DD_MAX} = 2.625V * 80mA = **210mW**
- Power Dissipation at built-in terminations: Assume the input is driven by a 2.5V SSTL driver as shown in Figure 1E and estimated approximately 1.75V drop across IN and nIN.

  Total Power Dissipation for the two 50Ω built-in terminations is: $(1.75V)^2 / (50\Omega + 50\Omega)$ = **30.6mW**
  Input pair for both inputs is 2 * 30.6mW = 61.2mW

  Total Power$_{\_MAX}$ (2.625V, with all outputs switching) = 210mW + 61.2mW = 271.2mW

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)
T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 49.5°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 0.271W * 49.5°C/W = 98.4°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 24-PIN VFQFN, FORCED CONVECTION

θ_{JA} vs. 0 Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	49.5°C/W	43.3°C/W	38.8°C/W

© 2019 Renesas Electronics Corporation

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 24 LEAD VFQFN

θ_{JA} vs. 0 Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	49.5°C/W	43.3°C/W	38.8°C/W

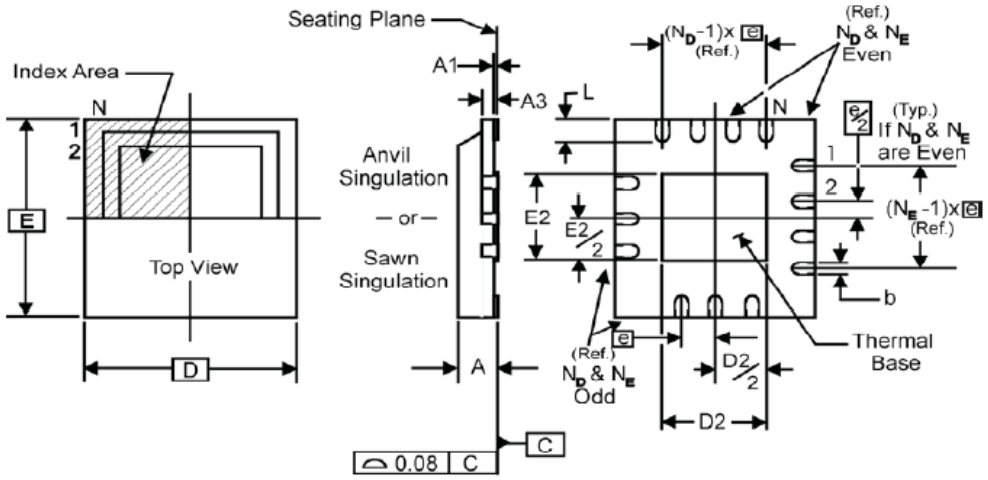
TRANSISTOR COUNT

The transistor count for 889474 is: 367

Pin compatible with SY89474U

© 2019 Renesas Electronics Corporation

Package Outline - K Suffix for 24 Lead VFQFN



NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pinout are shown on the front page. The package dimensions are in Table 8 below.

Table 8. Package Dimensions

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS		
SYMBOL	**MINIMUM**	**MAXIMUM**
N	24	
A	0.80	1.0
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.30
e	0.50 BASIC	
N_D	6	
N_E	6	
D	4	
D2	2.30	2.55
E	4	
E2	2.30	2.55
L	0.30	0.50

Reference Document: JEDEC Publication 95, MO-220

© 2019 Renesas Electronics Corporation

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
889474AKLF	9474AL	24 Lead VFQFN “Lead-Free”	tube	-40°C to 85°C
889474AKLFT	9474AL	24 Lead VFQFN “Lead-Free”	tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an “LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

© 2019 Renesas Electronics Corporation

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	T9	14	Ordering Information - removed leaded devices. Updated data sheet format.	11/11/15

© 2019 Renesas Electronics Corporation

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use o any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan

www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:

www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

© 2023 Renesas Electronics Corporation. All rights reserved.