AK2301

3.3V Single channel PCM CODEC LSI

GENERAL DESCRIPTION

The AK2301 is a single channel PCM CODEC for various applications for example, AFE.
It includes the selectable A/μ-law function, mute and power down. All of these functions are controlled by the pin. Ω Ω

It includes Band limiting filter, A/D and D/A converter, and A-law/μ-law converter. All functions are provided in small 16pin TSSOP package and it is good for reducing the mounting space.

PACKAGE

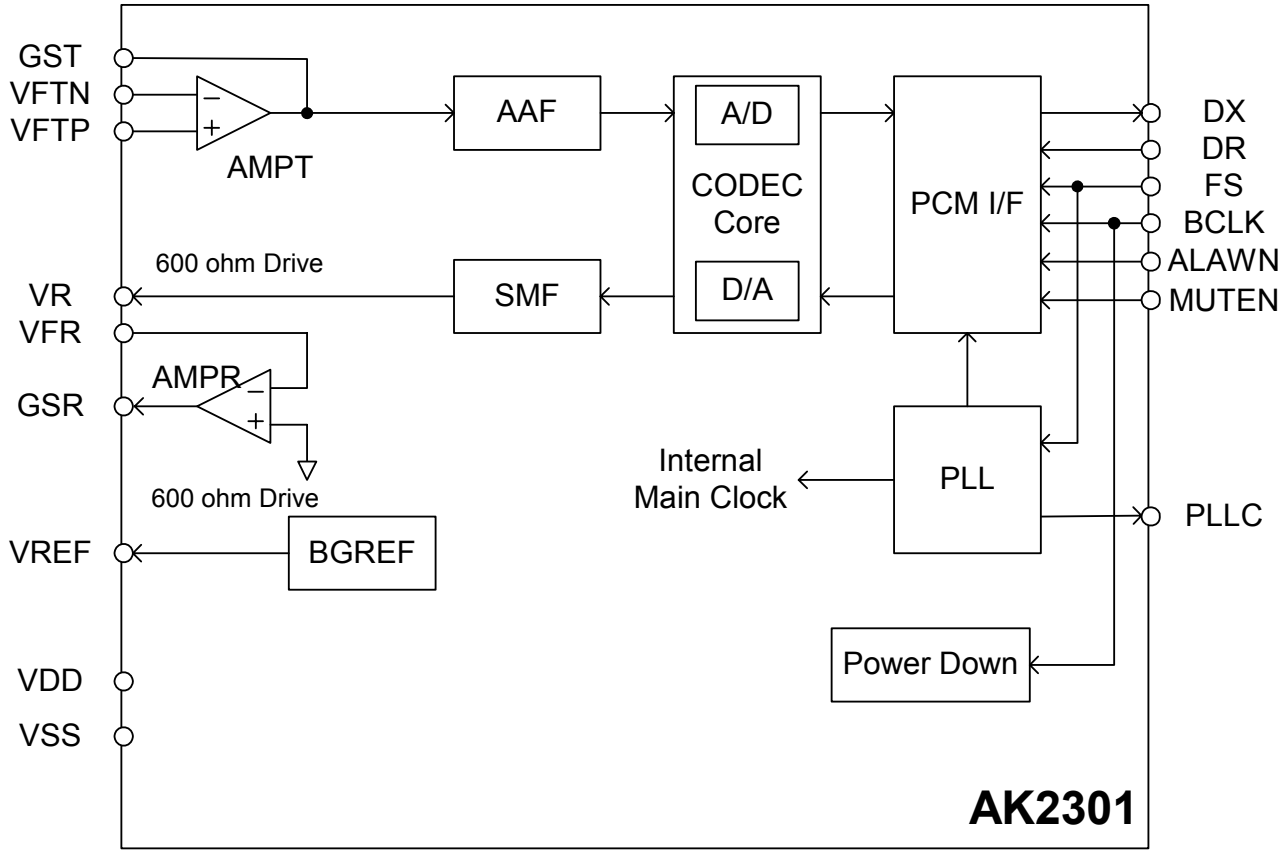
♦ 16pin TSSOP
Pin to pin 5.0*6.4mm
Pin pitch 0.65mm

FEATURE

♦Single PCM CODEC and filtering system
♦Selectable functions
- Mute
- A-law / μ-law

♦Long Frame / Short Frame are selected automatically
♦PCM data rate
(64k*N)Hz (N=1~32) (64 ~ 2048kHz)
♦ Op-amp for differential 600Ω power drives with external gain adjust
♦Power down function (BCLK="L")
♦ Single power supply voltage
+3.0~+3.6V
♦Low power consumption
- Power on : 8mA(typ)
- Power down : 5uA(typ)

BLOCK DIAGRAM



CONTENT

PIN CONDITIONS

Pin#	Name	I/O	Pin type	AC load (MAX.)	DC load (MIN.)	Output status (mute)	Power Down Output Status	Remarks
10	VFTN	I	Analog					
11	VFTP	I	Analog					
9	GST	O	Analog	50pF	AC load(*1) 10kΩ(*2)		Hi-Z	
6	GSR	O	Analog	40pF	AC load 600Ω(*2, *3)		Hi-Z	
7	VFR	I	Analog					
8	VR	O	Analog	40pF	AC load 600Ω(*2, *3)	Analog ground	Hi-Z	
5	VDD	-						
13	VSS	-						
4	FS	I	CMOS					Must not be left open
2	BCLK	I	CMOS					Must not be left open
1	DX	O	CMOS	50pF		Hi-Z	Hi-Z	
3	DR	I	CMOS					Must not be left open
16	MUTEN	I	CMOS					Must not be left open
15	ALAWN	I	CMOS					Must not be left open
12	VREF	O	Analog				VSS	- External capacitance 1.0uF or more
14	PLLC	O	Analog				VSS	- External capacitance 0.33uF±40% (Includes temperature characteristic)

*1) AC load is a load against AGND.
*2) This value includes a feedback resistance of input/output op-amps.
*3) In differential mode, this is the AC load between GSR and AC.

PIN FUNCTION

Pin types

DIN: Digital input TOUT: Tri-state output PWR: Power / Ground

AIN: Analog input AOUT: Analog output

Pin#	Name	Type	Function
10	VFTN	AIN	**Negative analog input of transmit OP amp.** Differential or single-ended input amplifier is composed with the VFTP pin and an external resistor for gain adjustment.
11	VFTP	AIN	**Positive analog input of the transmit OP amp.** Differential or single-ended input amplifier is composed with the VFTN pin and an external resistor for gain adjustment.
9	GST	AOUT	**Output of the transmit OP amp.** An inverting amplifier is composed with an external resistor for gain adjustment.
6	GSR	AOUT	**Output of the receive OP amp.** An inverting amplifier is composed with an external resistor for gain adjustment. Differential output can be composed with the VR output.
7	VFR	AIN	**Negative analog input of the receive OP amp.** An inverting amplifier is composed with an external resistor for gain adjustment. However, when the input gain op-amp is used as a differential amp, this inverting amp is used as an analog ground buffer for the differential amp. In this case, output gain adjustment or differential drive circuit composition by this inverting amp is not available.
8	VR	AOUT	**Analog output of the D/A converter** Differential output composition is possible with GSR outputs.
5	VDD	PWR	**Positive supply voltage**
13	VSS	PWR	**Ground (0V)**
4	FS	DIN	**Frame sync input** It controls In/Output timing of PCM data. FS must be 8kHz clock which synchronized with BCLK and do not stop feeding without power down mode.
2	BCLK	DIN	**Bit clock of PCM data interface** The frequency of BCLK should be 64kHz × N (N=1~32) and duty should be 40~60%. When this pin taken low, power down the device.
1	DX	TOUT	**Serial output of PCM data** A/D converted PCM data is output in synchronization with BCLK. This output remains in high impedance except for the period in which PCM data is transmitted.
3	DR	DIN	**Serial input of PCM data** The PCM data is synchronized with BCLK.
16	MUTEN	DIN	**Mute setting pin** "L" level forces both A/D and D/A outputs to mute state.
15	ALAWN	DIN	**A/u-law select pin** "L"=A-law, "H"=μ-law Please tie to H or L.
12	VREF	AOUT	**Analog ground output** External capacitance (1.0μF or more) should be connected between this pin and VSS. **Please do not connect external load to this pin.**
14	PLLC	AOUT	**PLL loop filter output** External capacitance (0.33μF±40%: Includes temperature characteristic) should be connected between this pin and VSS.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	min	max	Units
Power supply voltage Analog/Digital power supply	VDD	-0.3	4.6	V
Digital input voltage	V_{TD}	-0.3	VDD+0.3	V
Analog input voltage	V_{TA}	-0.3	VDD+0.3	V
Input current (except power supply pins)	I_{IN}	-10	10	mA
Storage temperature	Tstg	-55	125	°C

Warning: Exceeding absolute maximum ratings may cause permanent damage.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	min	typ	max	Units
Power supply voltage Analog/Digital power supply	VDD	3.0	3.3	3.6	V
Ambient operating temperature	Ta	-40		85	°C
Frame sync frequency *)	FS	-1.0%	8	+1.0%	kHz

Note) All voltages with respect to ground: VSS = 0V
*) All characteristics of the CODEC are defined in the condition that FS= 8kHz.

ELECTRICAL CHARACTERISTICS

Measurement conditions are: VDD = +3.3V±0.3V, Ta = -40~+85°C, FS=8kHz, VSS=0V, unless otherwise noted.

DC Characteristics

Parameter	Symbol	Conditions	min	typ	Max	Unit
Power Consumption All output unloaded	I_{DD1}*1)	*1) BCLK=2.048MHz		8	13	mA
	I_{DD2}	Power down (BCLK= "L")		5	100	uA
Output high voltage	V_{OH}	I_{OH} =-1.6mA	0.8VDD			V
Output low voltage	V_{OL}	I_{OL} =1.6mA			0.4	V
Input high voltage	VIH		0.7VDD			V
Input low voltage	VIL				0.3VDD	V
Input leakage current	ILL		-10		+10	uA
Analog ground output	VRG		1.4	1.5	1.6	V
Output leakage current	ILT	Tri-state mode	-10		+10	uA

*1) Measurement conditions: BCLK=2.048MHz, All output pins have no load. VFTP, VFTN (Differential)=1020Hz@0dBm0 input, DR=1020Hz@0dBm0 Code input

PCM INTERFACE **(Long Frame, Short Frame)**

Measurement conditions are: Ta=-40 to +85°C, VDD = 3.0~3.6V, VSS = 0V, FS=8kHz, unless otherwise noted. All timing parameters of the output pins are measured at VOH = 0.8VDD and VOL = 0.4V. Input pins are measured at VIH = 0.7VDD and VIL = 0.3VDD.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Ref Fig
FS Frequency	f_{PF}	-1.0%	8	+1.0%	kHz	Fig1,2
BCLK Frequency	f_{PB}	-	f_{PF}×8N (N=1~32)	-	kHz	
BCLK Duty Cycle	t_{WB}	40		60	%	
Rising/Falling Time: (BCLK,FS, DX,DR)	t_{RB} t_{FB}			40	ns	
Hold Time: BCLK Low to FS High	t_{HBF}	60			ns	
Setup Time: FS High to BCLK Low	t_{SFB}	60			ns	
Setup Time: DR to BCLK Low	t_{SDB}	60			ns	
Hold Time: BCLK Low to DR	t_{HBD}	60			ns	
Delay Time: BCLK High to DX valid Note1)	t_{DBD}	0		60	ns	
Delay Time: (A) BCLK Low to DX High-Z or (B) FS Low to DX High-Z or (C) BCLK High to DX High-Z Note1)	t_{DZC}	0		60	ns	
Long Frame						
Hold Time: 2nd period of BCLK Low to FS Low	t_{HBFL}	60			ns	Fig1
Delay Time: FS or BCLK High, whichever is later, to DX valid Note1)	t_{DZFL}			60	ns	
FS Pulse Width Low	t_{WFSL}	1			BCLK	
Short Frame						
Hold Time: BCLK Low to FS Low	t_{HBFS}	60			ns	Fig2
Setup Time: FS Low to BCLK Low	t_{SFBS}	60			ns	

Note1) Measured with 50pF load capacitance and 0.2mA drive.

Interface Timing

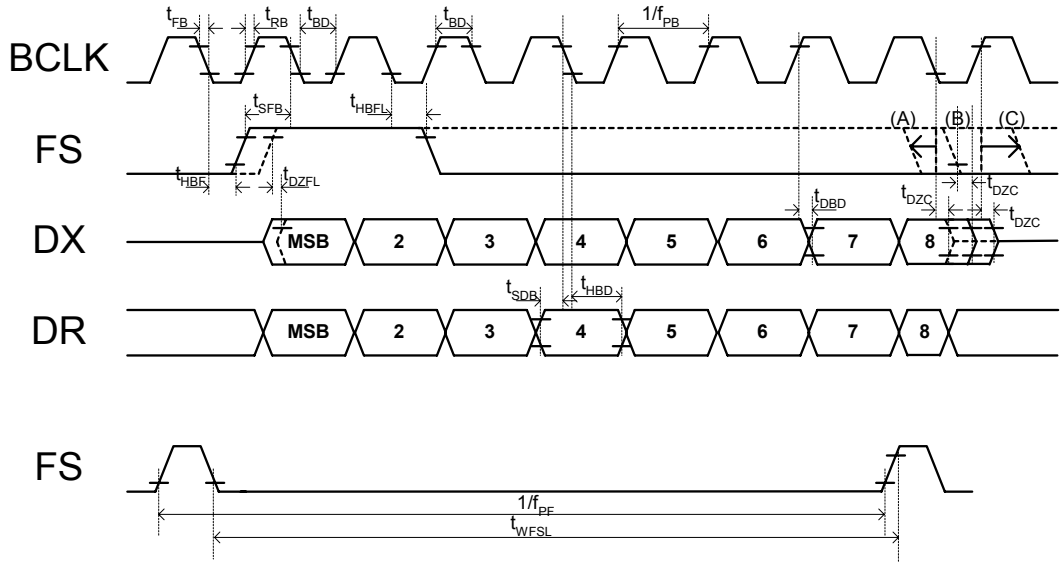


Figure 1. Long Frame

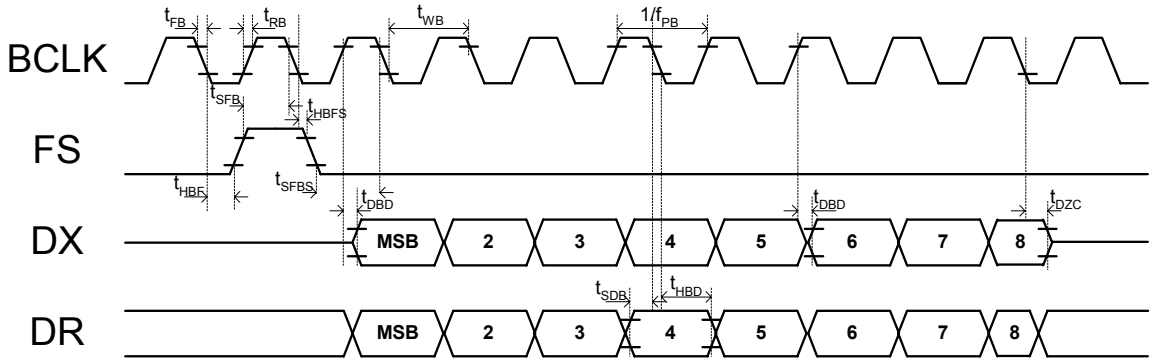


Figure 2. Short Frame

* The receive and transmit op-amp's characteristics are measured at the 0dB gain.
The frequency specifications when FS deviation from 8kHz are as follows:

$$\frac{Used\text{FS}}{8\text{k[Hz]}} \times \text{noted frequency specification} = \text{Effective frequency specification}$$

Absolute Gain

Parameter		Conditions	min	typ	max	Unit
Analog input level	VFTP,VFTN (Differential)→ DX (*1)	0dBm0@1020Hz input		0.531		Vrms
Absolute transmit gain			-0.6	–	0.6	dB
Maximum overload level		3.14dBm0		0.762		Vrms
Analog output level	DR → VR	0dBm0@1020Hz input		0.531		Vrms
Absolute receive gain			-0.6	–	0.6	dB
Maximum overload level		3.14dBm0		0.762		Vrms

(*1) In differential mode, 0dBm0= 0.531Vrms

Frequency response

Parameter	Conditions		min	typ	max	Unit
Transmit frequency response (A →D) VFTP,VFTN (Differential) →DX	Relative to: -10dBm0 1020Hz Tone	-55dBm0~ -50dBm0	-1.2	–	1.2	dB
		-50dBm0~ -40dBm0	-0.4	–	0.4	
		-40dBm0~ 3dBm0	-0.2	–	0.2	
Receive frequency response (D → A) DR → VR	Relative to: -10dBm0 1020Hz Tone	-55dBm0~ -50dBm0	-1.2	–	1.2	dB
		-50dBm0~ -40dBm0	-0.4	–	0.4	
		-40dBm0~ 3dBm0	-0.2	–	0.2	

Frequency response

Parameter	Conditions		min	typ	max	Unit
Transmit Frequency response (A → D) VFTP,VFTN (Differential) →DX	Relative to: 0dBm0@1020Hz	0.05kHz	–	–	-30	dB
		0.06kHz	–	–	-26	
		0.2kHz	-1.8	–	0	
		0.3~3.0kHz	-0.15	–	0.15	
		3.4kHz	-0.8	–	0	
		4.0kHz	–	–	-14	
Receive Frequency response (D → A) DR → VR	Relative to: 0dBm0@1020Hz	0~3.0kHz	-0.15	–	0.15	dB
		3.4kHz	-0.8	–	0	
		4.0kHz	–	–	-14	

Distortion

Parameter	Conditions		min	typ	max	Unit
Transmit signal to Distortion (A → D) VFTP,VFTN (Differential) →DX	1020Hz Tone	-40dBm0 ~ -45dBm0	25	–	–	dB
		-30dBm0 ~ -40dBm0	30	–	–	
		0dBm0 ~ -30dBm0	36	–	–	
Receive signal to Distortion (D → A) DR → VR	1020Hz Tone	-40dBm0 ~ -45dBm0	25	–	–	dB
		-30dBm0 ~ -40dBm0	30	–	–	
		0dBm0 ~ -30dBm0	36	–	–	

Note) C-message Weighted for μ-Law, Psophometric Weighted for A-Law

Noise

Parameter	Conditions	min	typ	max	Units
Idle channel noise A→D (*1)	u-law, C-message	–	8	13	dBrnC0
VFTP,VFTN (Differential) →DX	A-law, Psophometric	–	-85	-80	dBm0p
Idle channel noise D→A(*2)	u-law, C-message	–	5	10	dBrnC0
DR → VR	A-law, Psophometric	–	-85	-80	dBm0p
PSRR Transmit path	VDD=3.3V/±66mVop f=0~10kHz	–	55	–	dB
PSRR Receiver path	VDD=3.3V/±66mVop F=0~10kHz	–	55	–	dB

(*1) Analog input is set to the analog ground level
(*2) Digital input is set to the +0 CODE

Crosstalk

Parameter	Conditions	min	typ	max	Units
Transmit to receive VFTP → VR,GSR(Differential)	VFTP 0dBm0@1020Hz DR = PCM 0-Code	–	–	-75	dB
Receive to transmit DR → DX	DR=0dBm0@1020Hz code level VFTP,VFTN = 0 Vrms	–	–	-75	dB

Transmit op-amp characteristics :AMPT

Parameter	Conditions	min	typ	max	Units
Load resistance	AC load, Including feedback resistance	10	–	–	kΩ
Load capacitance		–	–	50	pF
Gain	Inverting amplifiers (Feedback capacitance = 100pF, fc= 80kHz)	-12	–	6	dB

Receive signal output characteristics: VR

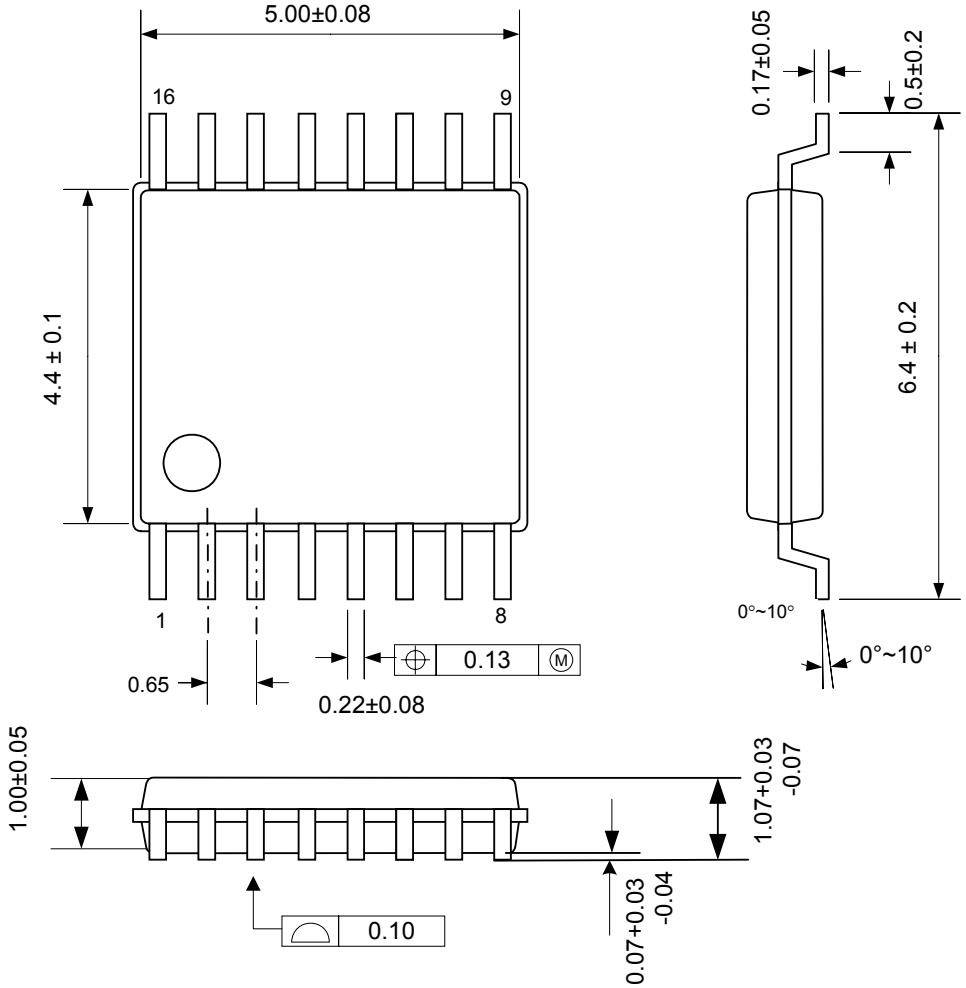
Parameter	Conditions	min	typ	max	Units
Output voltage (AGND level)	PCM +0 code input	–	1.5	–	V
Load resistance	AC load	600	–	–	Ω
Load capacitance		–	–	40	pF

Receive op-amp characteristics: AMPR

Parameter	Conditions	min	typ	max	Units
Load resistance	AC load, Including feedback resistance	600	–	–	Ω
Load capacitance		–	–	40	pF
SINAD	0dB setting, 1020Hz@0dBm0 input VR,GSR differential output (600Ω load) With C-message	50	70	–	dB
	0dB setting, 1020Hz@0dBm0 input VR,GSR differential output (5kΩ load) With C-message		80		
Gain	Inverting amplifier (Feedback capacitance = 100pF, fc= 40kHz)	-12	–	6	dB
Output voltage swing	DR = 3.14dBm0 digital code input	–	2.15	–	Vp-p

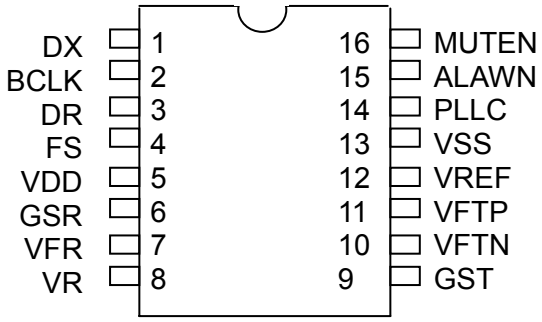
PACKAGE INFORMATION

16pin TSSOP



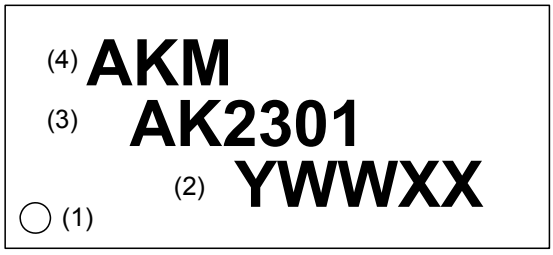
PIN ASSIGNMENT

16pin TSSOP



MARKING

(1) 1pin sign
(2) Date Code: 5digit YWWXX
Y: Date Code (year)
WW: Date Code (week)
XX: Control Code
(3) Marketing Code: AK2301
(4) AKM logo



CIRCUIT DESCRIPTION

BLOCK	FUNCTION
AMPT	Op-amp for input gain adjustment. A differential or single-ended input amplifier is composed with an external resistor. The feedback resistor should be larger than 10kΩ. Each pin definition is shown below. VFTN: Negative op-amp input. VFTP: Positive op-amp input. GST: Op-amp output.
AMPR	Op-amp for output gain adjustment. This op-amp is used as an inverting amplifier. A differential or single-ended amplifier is composed with an external resistor. Each pin definition is shown below. VFR: Negative op-amp input. GSR: Op-amp output. VR and GSR can be used as the differential output. In this case, more than 600Ω AC load should be composed with external and feedback resistors.
AAF	Integrated anti-aliasing filter (AAF) It prevents signal noise around the sampling rate from folding back into the voice band. AAF is a 2nd order RC active low-pass filter.
CODEC A/D	Converts analog signal to 8bit PCM data according to the compounding schemes of ITU recommendation G.711; A-law or u-law. Even bits are inverted in A-Law conversion. The compounding schemes is set by the ALAWN pin as follows: "H": u-Law "L": A-Law The band limiting filter is also integrated.
CODEC D/A	Expands and playbacks the 8bit PCM data from the DR pin according to the compounding schemes of ITU recommendation G.711; A-law or u-law. Even bits are inverted in A-Law converting. The compounding schemes is set by the ALAWN pin as follows: "H": u-Law "L": A-Law
SMF	Extracts the inband signal from D/A output. It also corrects the sinx/x effect of the D/A output.
BGREF	Provide the stable analog ground voltage using an on-chip band-gap reference circuit which is temperature compensated. The output voltage is typ. 1.5V. An external capacitor of 1.0uF or larger should be connected between VREF and VSS to stabilize analog ground (VREF). **Please do not connect external load to this pin.** Characteristics are not guaranteed when connecting an external load. The output should be buffered if using this voltage externally.
PCM I/F	PCM data transferring rate is dependent on BCLK. Two kinds of data format (Long Frame/Short Frame) are available. Each data format is automatically detected by the AK2301. PCM data is input to the DR pin and output from the DX pin.

FUNCTIONAL DESCRIPTIONS

PCM CODEC

- A/D
Analog input signal is converted to 8bit PCM data. The analog signal is fed to the anti-aliasing filter (AAF) before converting to PCM data to prevent signals around the sampling rate from folding back into the voice band. The converted PCM data passes through the band limiting filter which Frequency response is designated in page8, and output from the DX pin in MSB first format. It is synchronized with rising edge of the BCLK. This PCM data is A/u-law and full scale is defined as 3.14dBm0. The analog input of 0.762Vrms is converted to a digital code of 3.14dBm0.

- D/A
Input PCM data from the DR pin is through the digital filter, which Frequency response is designated in page8, and converted to analog signal. This analog signal is removed the high frequency element with SMF (fc=30kHz typ) and output from the VR pin. The input PCM data is A/u-law data and full scale is defined as 3.14dBm0. When the input signal is 3.14dBm0, the level of the analog output signal becomes 0.762Vrms.

PCM Data Interface

The AK2301 supports the following 2 PCM data formats
- Long Frame Sync (LF)
- Short Frame Sync (SF)
PCM data is interfaced through a pin. (DX, DR).
In each case, PCM data is interfaced in MSB first format.

Selection of the interface format
The AK2301 automatically selects the Long Frame/Short frame by means of detecting the length frame signal.

LONG FRAME (LF) / SHORT FRAME (SF)
-Automatic LF/SF detection
The AK2301 monitors the duration of the “H” level of FS and automatically selects LF or SF interface format.

Period of FS=”H”	Frame type
More than 2 BCLK cycles	LF
1 BCLK cycle	SF

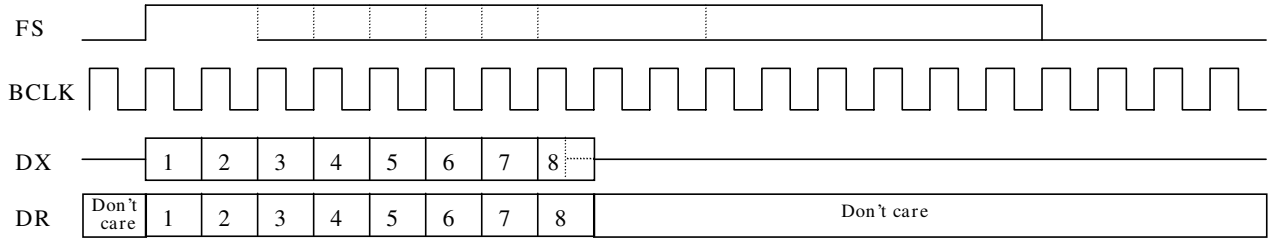
Timing of the interface
8bit PCM data is accommodated in 1 flame (125μs) defined by 8kHz frame sync signal. Although there are 32 time-slots at maximum in 8kHz frame (when BCLK = 2.048MHz), PCM data for the AK2301 occupies the first time-slot.

- Frame sync signal (FS)
8kHz reference signal. 8bit PCM data is transferred in every 1 frame (125us). This signal must be synchronized with BCLK.

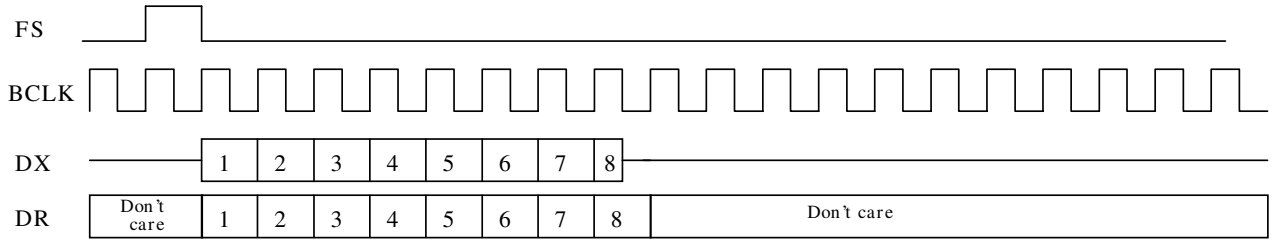
WARNING!
The AK2301 must be in power down mode by BCLK = "L" when stopping FS.

- BCLK (Bit clock)
BCLK defines the PCM data rate. BCLK rate is 64kHz × N (N=1~32).

LongFrame



ShortFrame



MUTE

The output of the PCM CODEC can be muted by a pin control.

MUTEN pin

MUTEN pin	Operation	DX pin	VR pin
L	Mute	High-Impedance	CODEC analog ground
H	Normal	PCM data output	CODEC analog output

[DX pin]
When the MUTEN pin turns to “L” during the data output, the mute function becomes available at the beginning of the next FS after all bits are output.

[VR pin]
When the MUTEN pin turns to “L”, 0 code is fed to the D/A converter and VR becomes at analog ground level.

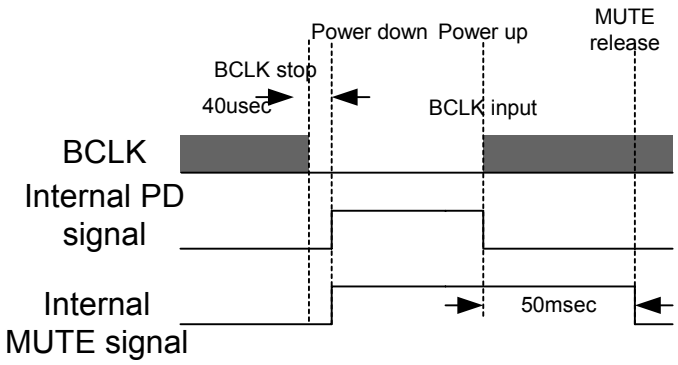
POWER DOWN MODE

To hold the BCLK pin “L”, the AK2301 is powered down.

Power up/down sequence

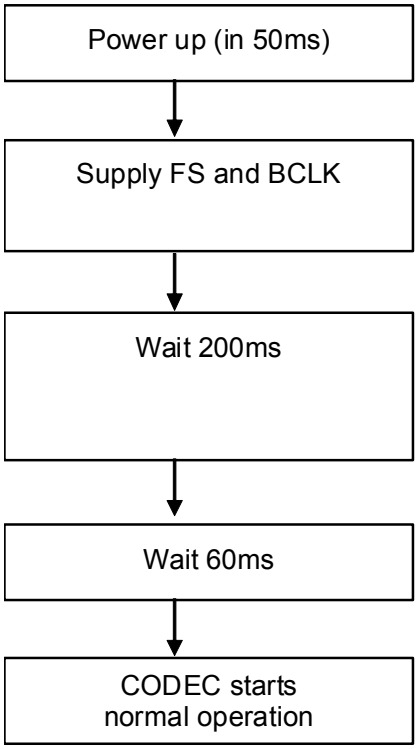
1)Power down
40usec(typ) passed after the BCLK pin hold “L”, the internal PDN signal turn to “L” and the AK2301 enters power-down mode. In power-down mode, the GST, DX, GSR and VR pins are Hi-z. The VREF and PLLC pins output VSS.

2)Power up
Power-down mode is released when FS and BCLK are input. Outputs are muted (DX=High-Z, VR=AGND) for 50msec (typ) after the power-down is released to avoid noises.



Power Up Sequence

The following start up process is recommended when power up the AK2301.



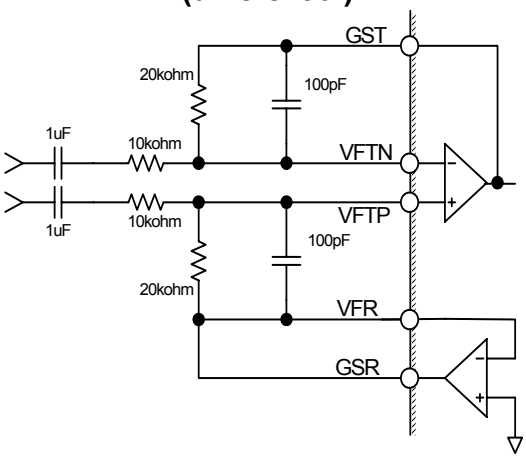
- FS="L"
- BCLK="L"
- MUTEN="L"

- CODEC Initialization starts.

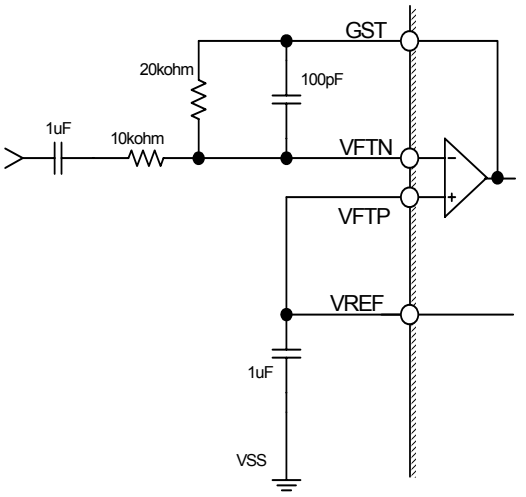
- CODEC Initialization completes.
- MUTEN="H"

APPLICATION CIRCUIT EXAMPLES

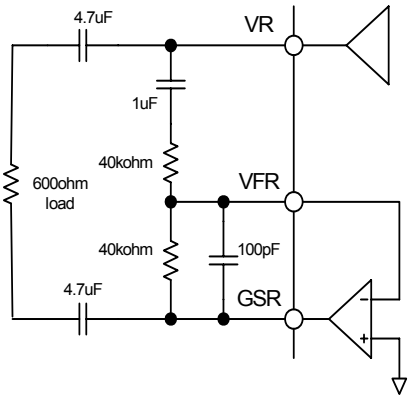
Analog input circuit (differential)



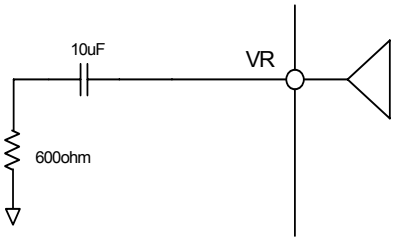
Analog input circuit (single)



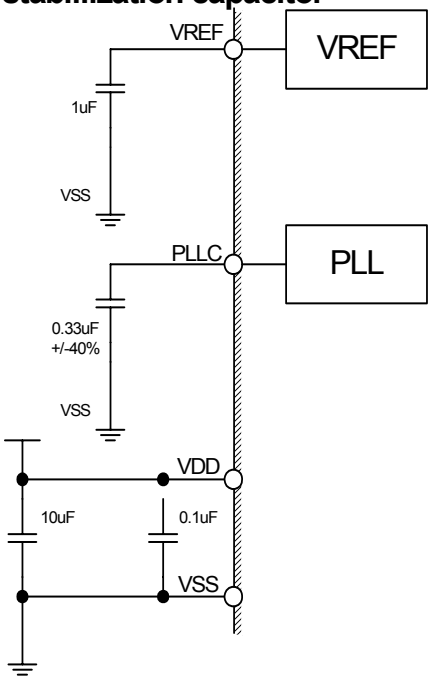
Analog output circuit (differential)



Analog Output Circuit (Single)



Power supply, PLL loop filter capacitor and analog ground stabillization capacitor



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