

Evaluation board for CoolSiC™ Easy1B half-bridge modules

Evaluation of CoolSiC™ MOSFET modules in a bidirectional buck-boost converter

About this document

Scope and purpose

SiC MOSFET-based modules are a revolutionary step towards highly efficient power electronic devices with a benchmark in terms of power density. Switching frequencies exceeding 100 kHz as well as greater than 99% power conversion efficiency are simple to implement using Infineon EasyPACK™ modules with CoolSiC™ trench-MOSFET devices.

The purpose of this board is to enable the evaluation of the FF11MR12W1M1_B11 and FF23MR12W1M1_B11 CoolSiC™ MOSFET modules. The evaluation board allows users to evaluate the device performance via double-pulse measurements and functional tests as bidirectional buck-boost converter. The board is designed on a bidirectional buck-boost converter topology.

The properties of this board are described in the design features chapter of this document. The remaining sections provide information to enable designers to copy, modify and qualify the design for production, according to the customer specific requirements.

Environmental regulations have been considered in the design of the EVAL-PS-E1BF12-SiC board. Components qualified for a lead-free, reflow soldering process have been selected. The design has been tested as described in this document, but not qualified regarding manufacturing and operation over the whole operating temperature range or lifetime.

Note: The evaluation boards provided by Infineon are only designed for functional testing, and are available in small quantities.

In view of their function, evaluation boards are not subject to the same procedures in the context of Returned Material Analysis (RMA), Process Change Notification (PCN) and Product Discontinuation (PD) as other products.

Read the legal disclaimer and warnings for further restrictions on Infineon's warranty and liability.

Warnings



Caution: The described evaluation board is dedicated for a laboratory environment only. It operates at high voltages. This board must be operated by qualified and skilled personnel familiar with all applicable safety standards.

Intended audience

This document is intended for engineers who design power converters on the basis of Infineon CoolSiC™ modules used in their applications.



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Introduction

1 Introduction

1.1 Design features

The EVAL-PS-E1BF12-SiC evaluation board has been designed as a bidirectional buck-boost converter. It enables users to make basic electrical tests such as double-pulse measurements as well as functional testing in buck and/or boost operation. Figure 1 shows a picture of the physical appearance of the board which has a dimension of 133 mm x 175 mm.

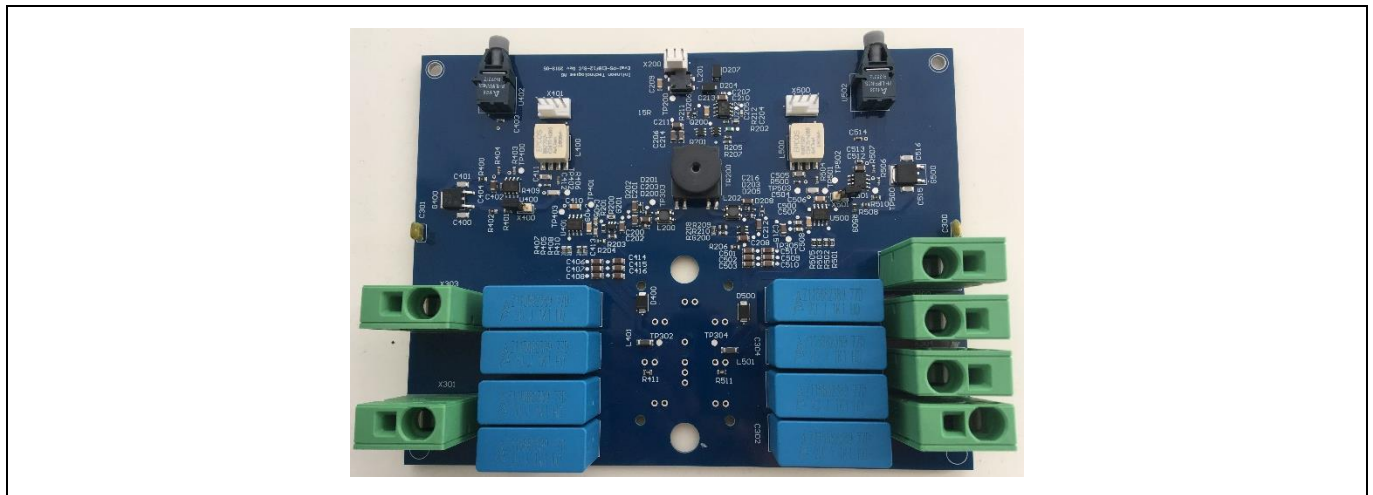


Figure 1 Evaluation board EVAL-PS-E1BF12-SiC

This section provides an overview of the evaluation board, and includes the description of its main features, key data, pin assignments and mechanical dimensions.

Figure 2 shows the circuit topology used in the described evaluation board in conventional buck-boost converter mode. The board is provided with the option of using an Easy 1B device in half-bridge configuration, and includes drivers for the top and bottom device of the power module, and high-frequency decoupling capacitors. It also has the option of providing an external gate driver signal via electrical signals or optical fibers. Any other components necessary for converter systems such as inductors, bulk capacitors and necessary protection circuits need to be added externally if required in the application.

Introduction

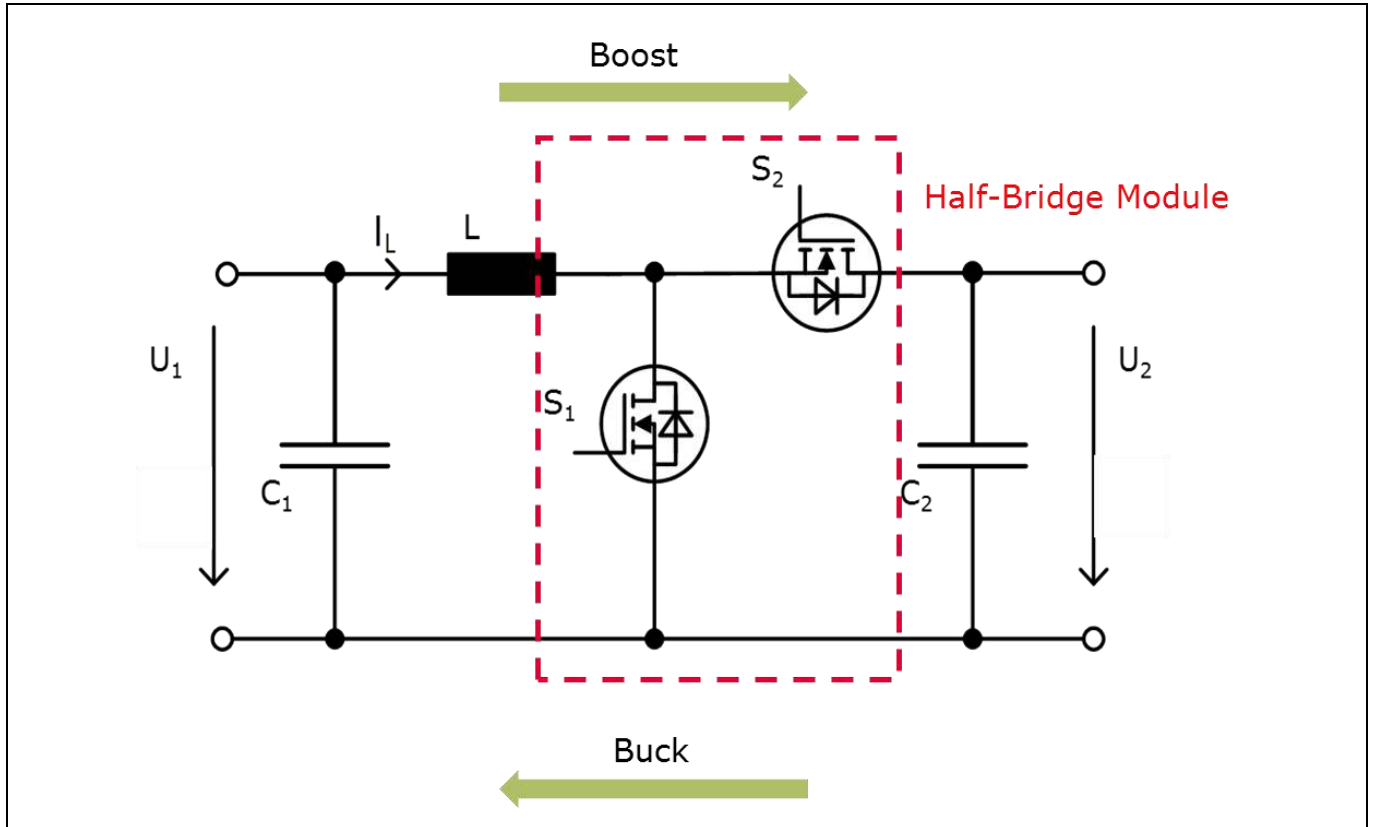


Figure 2 Bidirectional buck-boost converter using a CoolSiC™ MOSFET half bridge

The main function of this board is the evaluation of the FF11MR12W1M1_B11 and the FF23MR12W1M1_B11 in combination with the EiceDRIVER™ 1EDI60IH12AH driver.

1. A bidirectional buck-boost converter is a useful converter in today’s power electronics’ world. As an example, transformer-less chargers use it to charge and discharge high-voltage batteries. Another application for the boost mode is the maximum power point tracker (MPPtracker) for PV applications achieving high efficiency by synchronous rectification. In the boost operation mode, S1 is the active switch, while S2 is operated as the diode. The buck operation works with S2 as the active switch and S1 as the diode.
2. The evaluation board is electrically and mechanically suitable for the FF11MR12W1M1_B11 and the FF23MR12W1M1_B11 CoolSiC™ MOSFET modules. The initial configuration of the board is equipped with the required components to do:
 - Double-pulse characterization
 - Functional testing of the buck-boost operation using electrical loads at the input or output stage

Introduction

1.2 Key data

General key data and characteristic values are given in Table 1. These are typical values, measured at an ambient temperature of $T_{amb} = 25^{\circ}C$.

Table 1 Electrical parameters

Parameter	Description DC-link	Value	Unit
V_{DC}	Maximal input DC-link voltage	900	V
I_{out}	Maximal output current	25	A
C_{DC}	DC-link capacitance at the board delivery (input and output)	8	μF
T_{op}	Operation temperature (design target)	-40...+85	$^{\circ}C$
T_{stg}	Store temperature (design target)	-40...+85	$^{\circ}C$
Parameter	Description driver and SMPS	Value	Unit
V_{CC}	Driver input voltage	15	V
V_{GS}	Drive voltages at the SiC MOSFET switches	-3/18	V
I_G	Maximum and minimum gate driver current for each driver channel	6	A

1.3 Pin assignments

The evaluation board allows an optical or electrical pulsing of the two SiC MOSFET switches. The connector names are highlighted in Figure 3. The pin numbering is from left to right for the gate signals.

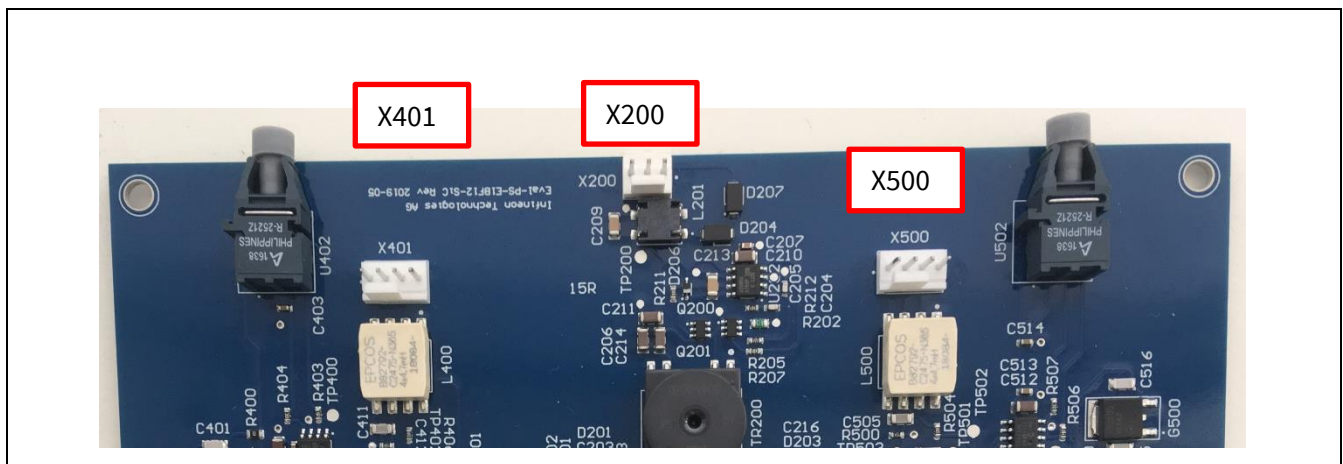


Figure 3 Connectors of the evaluation board’s driver circuit

The board is powered by the connector X3 as listed in the Table 2.

Table 2 Pin assignment of the connector X200 to power the internal DC/DC converter

Pin name	Pin
X200_1	+15 V
X200_2	No Connection
X200_3	GND

Introduction

X401 and X500 pin assignment

Each SiC MOSFET switch has a separate driver circuitry. The interfaces for external signal measurement are offered by X401 and X500 as listed in Table 3 and Table 4.

Table 3 Pin assignment of connector X401 for the driving of upper device (S2)

Pin name	Pin
X401_1	+5 V
X401_2	GND
X401_3	PWM signal
X401_4	GND

Table 4 Pin assignment of connector X500 for the driving of lower device (S1)

Pin name	Pin
X500_1	+5 V
X500_2	GND
X500_3	PWM signal
X500_4	GND

The optical pulsing of the top device is possible via U402, while the bottom device is pulsed using U502. Additionally, the corresponding jumpers X400 (for U402) and X501 (for U502) have to be activated.

The inductor of the bidirectional buck-boost converter is connected between the connectors X304 and X305 of the board. The respective DC-source and load connections depend on whether the board is used as buck or boost converter.

Functional blocks

2 Functional blocks

2.1 Power stage

The purpose of the EVAL-PS-E1BF12-SiC board is to evaluate the CoolSiC™ MOSFET half-bridge modules in the Easy1B package. The functional schematics of the board are shown in Figure 4. Electrical or optical pulses are translated in the evaluation board to signals for the 1EDI60IH12AF driver. Each driver controls one of the SiC MOSFET switches within the FF11MR12W1M1_B11 or FF23MR12W1M1_B11 modules. The driving voltages are -3 V/18 V.

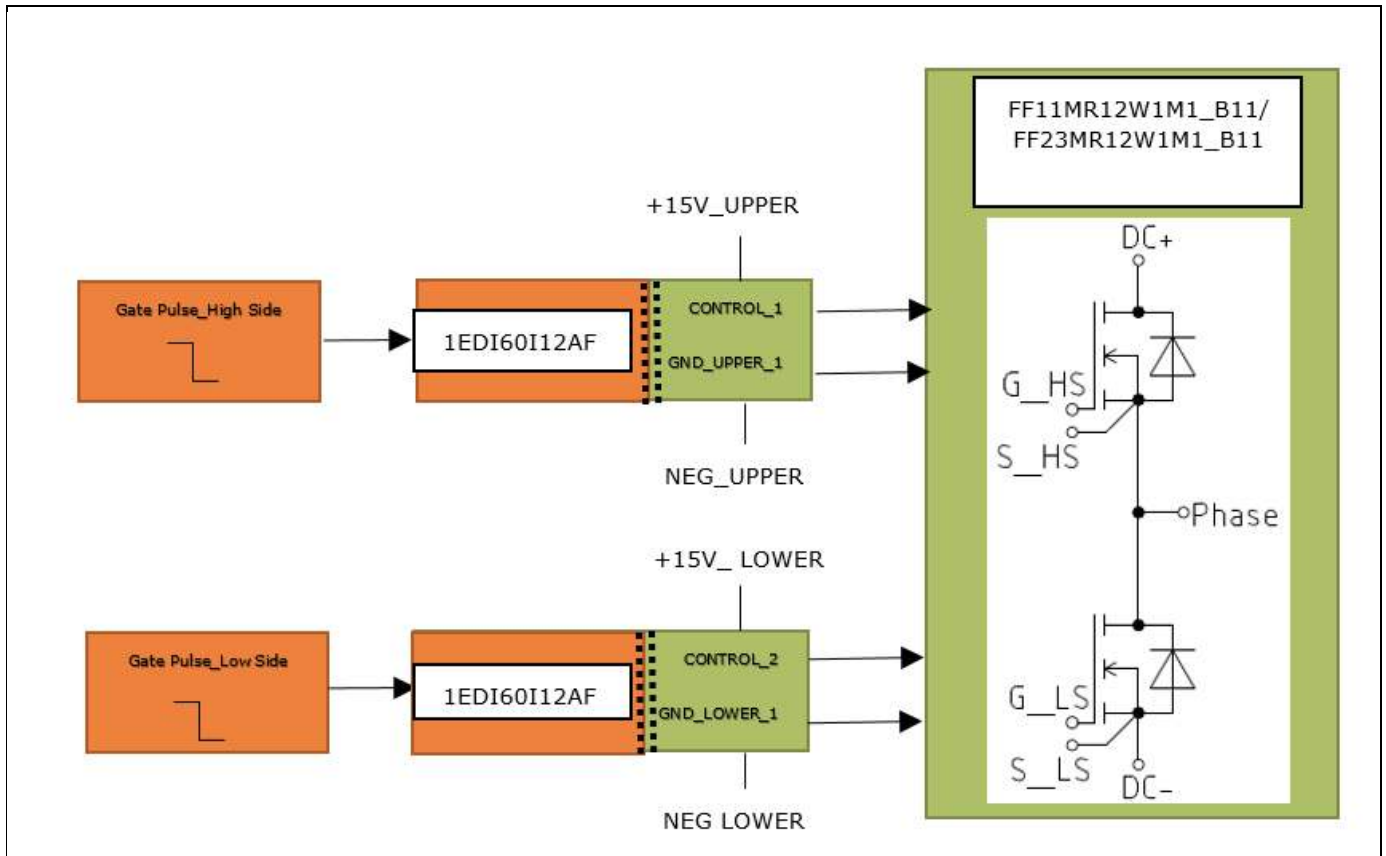


Figure 4 Functional schematic of the evaluation board

2.2 Driver power supply stage

The evaluation board is equipped with the isolated power supply required for driving the gate of the power devices. The power supply has been implemented by a half-bridge DC-bus converter. It is controlled on the primary side by AU1R2085S based self-oscillating, half-bridge driver. The schematic is shown below in Figure 5. The isolated secondary side has been equipped with a regulated adjustable linear regulator, which has been adjusted for -3 V to supply negative voltage to the gate for this board. The negative gate voltage level can be adjusted according to the application note **AN2018-09** (Guidelines for CoolSiC™ MOSFET gate-drive voltage window) depending on the device and operating conditions.

Functional blocks

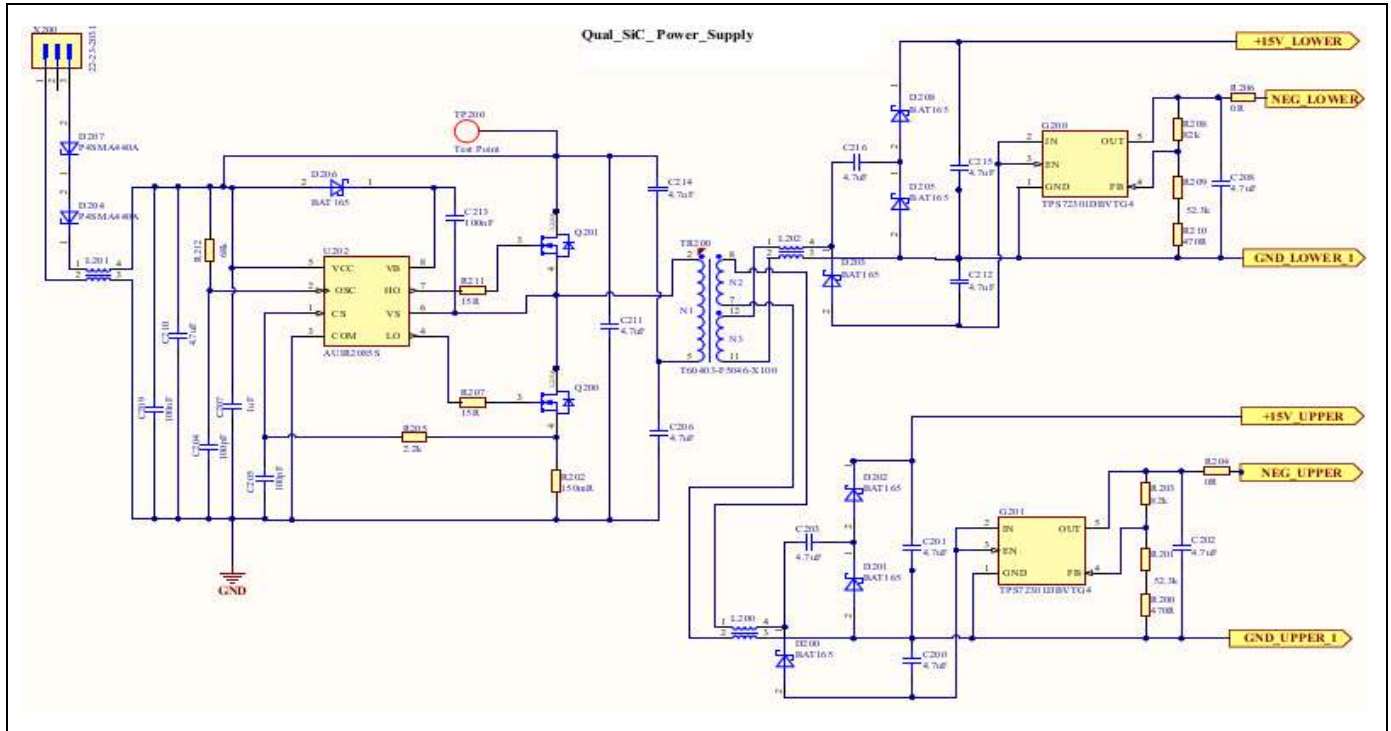


Figure 5 Gate driver power supply of lower-side device

2.3 Driver stage:

The driver stage for upper and lower device has been implemented in the board and below section.

The driver stage for the lower side device can be seen in figure 6. The upper part of the picture shows the optical driver input. U502 converts the optical signal into an electrical signal, the driver stage TC4426EOA transforms the electrical signals to an input voltage for EiceDRIVER™ Compact 1EDI60I12AF.

An optional 15 V/+5 V linear regular circuit has been implemented which can be configured for supplying 5 V for various combinations of optical and electrical input voltages. This will ensure a proper supply voltage to U502 connector (HFBR-2521Z), U501 (TC4426EOA) and U500 (1EDI60I12AF) control power supply. The table below shows the options available on the board to reconfigure it for different types of optical input and electrical voltages.

Table 1 Configuration for external 15 V supply for optical and electrical control input

Component	Status
X400, X501	Shorted for optical input gate drive signal/Open for electrical control input gate drive signal
R400, R402 , R509, R510 Open	Electrical 5 V input at connector U502, U402 available
R509, R510, R400, R402 Open	Electrical 5 V input at connector X500, X401 available
R401 and R508 Open	Electrical 15 V input at connector X500, X401 available

Functional blocks

The analog electrical driver input is illustrated on the bottom left of Figure 6. The electrical input is fed via a common mode choke (L400, L500) to the driver stage for better immunity from noise.

The driver output is shown in the bottom right section of Figure 6. The driver voltages of -3 V/18 V are decoupled from the ground by capacitors. The turn-on and turn-off resistance of the EiceDRIVER™ output is realized by a parallel connection of two SMD resistors.

Special mention should be made here of the issue of false gate turn-on, a phenomenon in a half-bridge SiC configuration that is due to ringing in the V_{gs} of the MOSFET. The higher switching speed and parasitic capacitance plays a major role in this phenomenon. Layout considerations have been made for reducing stray inductances, and provisions made in the gate drive circuitary for adjusting the dv/dt which helps to reduce the ringing of the circuit.

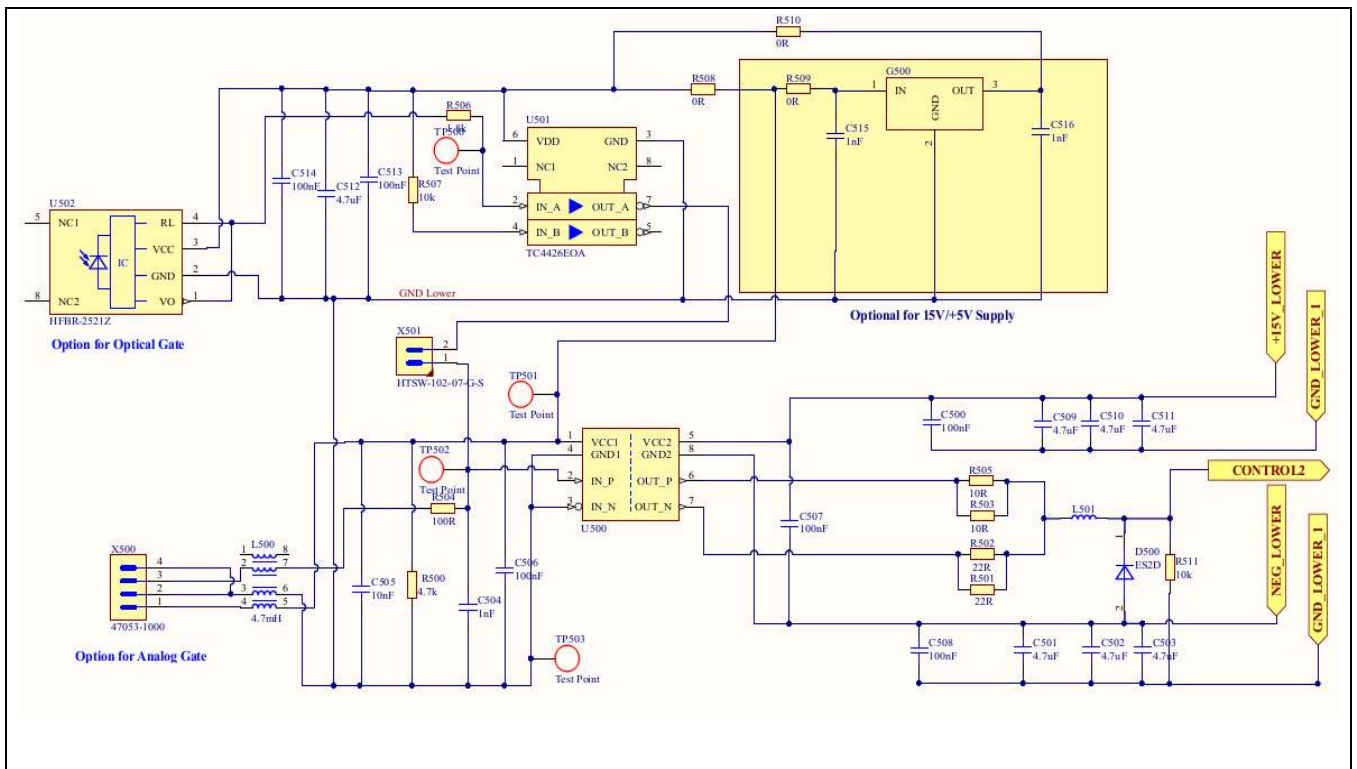


Figure 6 Schematic details of the input stage for a single MOSFET driver section

Characterization

3 Characterization

3.1 Test setup and current measurement

Figure 7 captures the test setup and voltage measurement techniques for double-pulse testing of lower devices. The first turn-on pulse of the low-side device (S2) establishes the desired current value (e.g. nominal data sheet current in this case) in the inductive load, and the turn-off pulse makes the current flow in the free-wheeling diode (e.g. body diode of the top device S1 in this case). An external inductance value of 630 μH was used in the actual test setup. The second turn-on pulse measures the low-side device turn-on characteristics, which also include the reverse recovery of the free-wheeling diode.

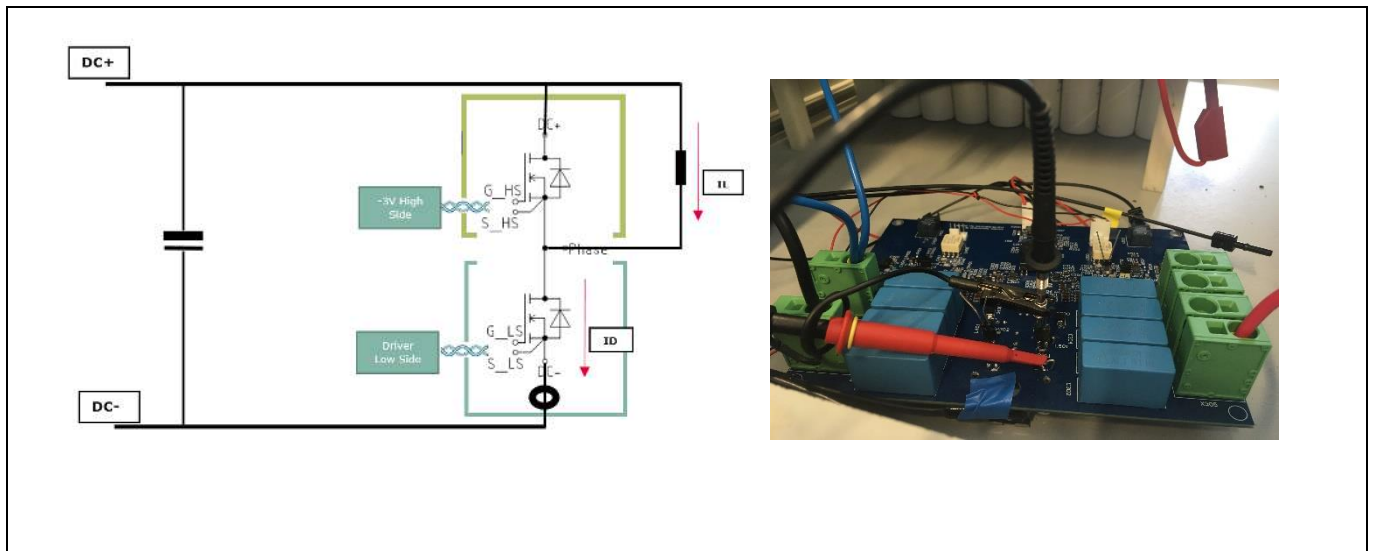


Figure 7 Test setup and voltage measurement techniques

The source-current measurement of S1 and S2 is done with the help of copper rivet adapters (Part no. Stäubli 41.0051B1) and Rogowski current sensors as shown below in Figure 8. Be aware that the use of rivet adapters leads to an increase in inductance in the main circuit as well as in the gate circuit.

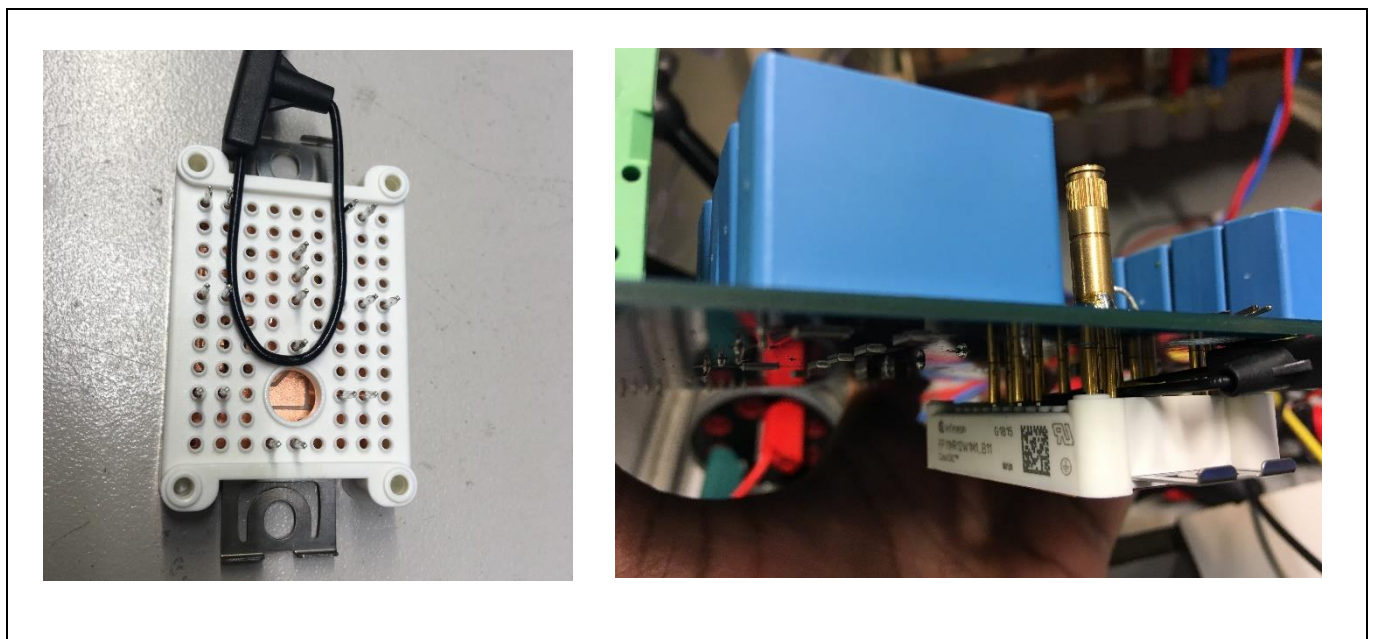


Figure 8 Current measurement with the help copper rivets and a Rogowski coil

Characterization

All current measurements shown in this application note have been performed with thin clip-around Rogowski coils of 1.2 kV, having a 1.6 mm cross section. The bandwidth of the Rogowski coil is 30 MHz with current ratings of 300 A with di/dt capabilities of 20 kA/uS.

3.2 Test results

This chapter presents some examples of extracted waveforms of the module FF11MR12W1M1_B11 Easy1B, which has been characterized with the help of the evaluation board.

One key aspect in designing half-bridge topologies with SiC MOSFET devices is to assess the risk of a parasitic turn-on of the upper device during switching of the lower device, and vice versa. This effect may be caused by a high dv/dt of a SiC MOSFET, which can exceed 50 kV/μs for a CoolSiC™ MOSFET.

To mitigate the situation, two approaches have been considered here. As a first approach, asymmetric power supplies such as +18 V/-3 V are used to drive the gate of the device. This creates a safe margin so that the ringing voltage does not touch the gate threshold limit ($V_{th}=4.5\text{ V}$). In the case of unipolar switching (15V/0 V), the dv/dt can be reduced by using larger gate resistance to mitigate the parasitic turn-on events. This is a significant advantage of the simple gate controllability of CoolSiC™ MOSFET devices. For more details on this topic, see the article referred to in [4].

As a second approach, an external capacitor ($R_{511}, R_{411} = 1.5\text{ nF}$ capacitance) is added between the gate and the source for a better ratio between C_{gs} and C_{gd} . This lowers the impedance of the gate terminal and helps to get rid of the ringing in the waveform although it sacrifices some switching speed. Figure 9 shows the turn-on behavior of the lower-side device with gate resistor of 5 ohm (2 of 10 Ohm resistors are in parallel) and external gate capacitances of 1.5 nF.

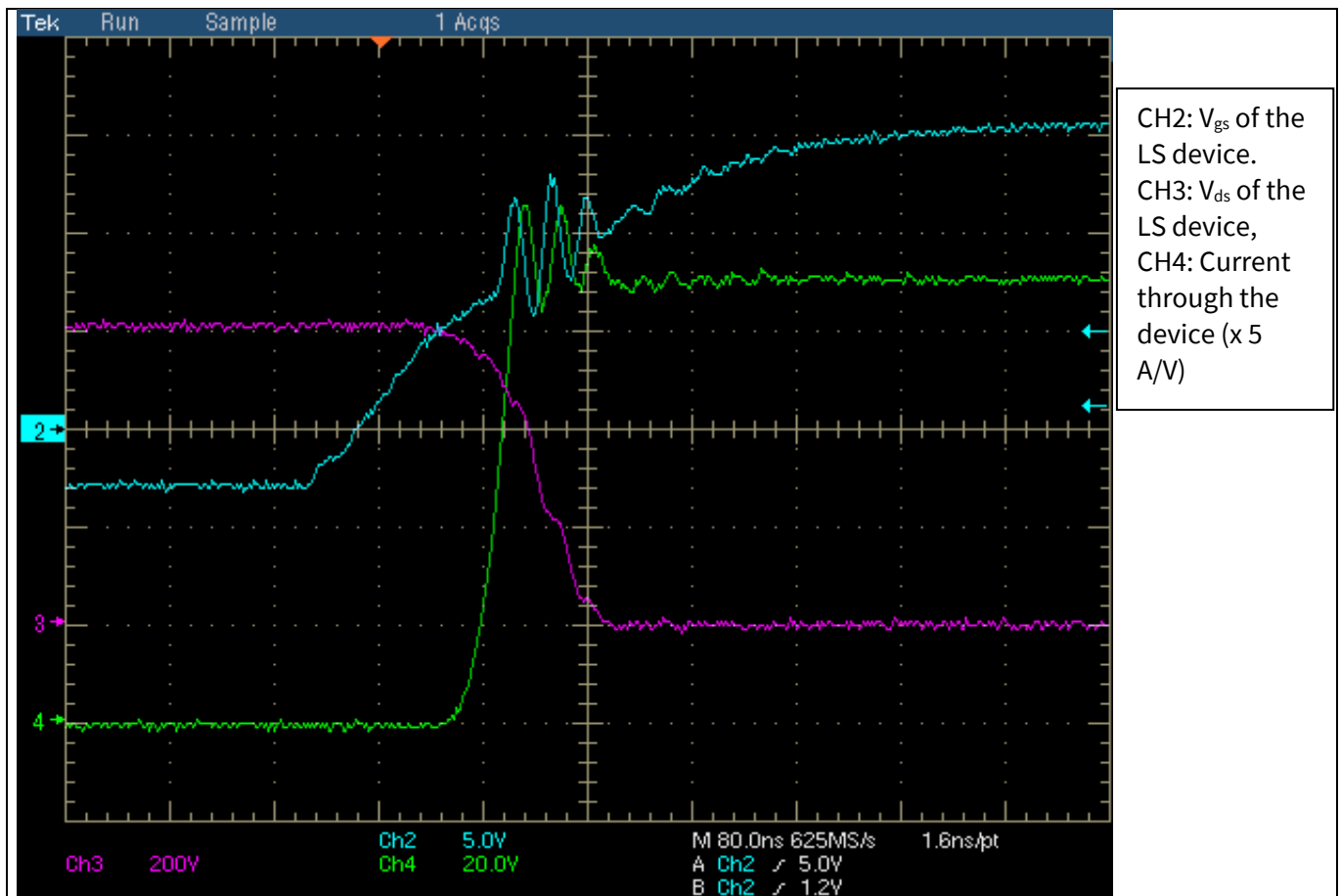


Figure 9 Turn-on of a FF11MR12W1M1_B11 device at 100 A and 600 V

Characterization

As shown, the switching waveform has less ringing, which improves the EMI performance and has been optimized by taking advantage of low board inductance and the low inductive parasitics of the Easy1B module.

Figure 10 shows the turn-off behavior of the device under test at the same operation point with a equivalent turn-off gate drive resistance of 11 Ohm (2 of 22 Ohm resistors are in parallel) . During turn-off, the overvoltage peak of V_{ds} has to be properly analyzed, as the di/dt of the FF11MR12W1_B11 is up to ten times higher than a comparable IGBT current gain leading to a high overvoltage with respect to

$$V_{DC} = V_0 + \frac{di}{dt} \times L_{\sigma}$$

The low stray inductances of the power module and the board lead to a low overvoltage below 100 V, which is reasonable for a power electronic application using CoolSiC™ MOSFET modules.

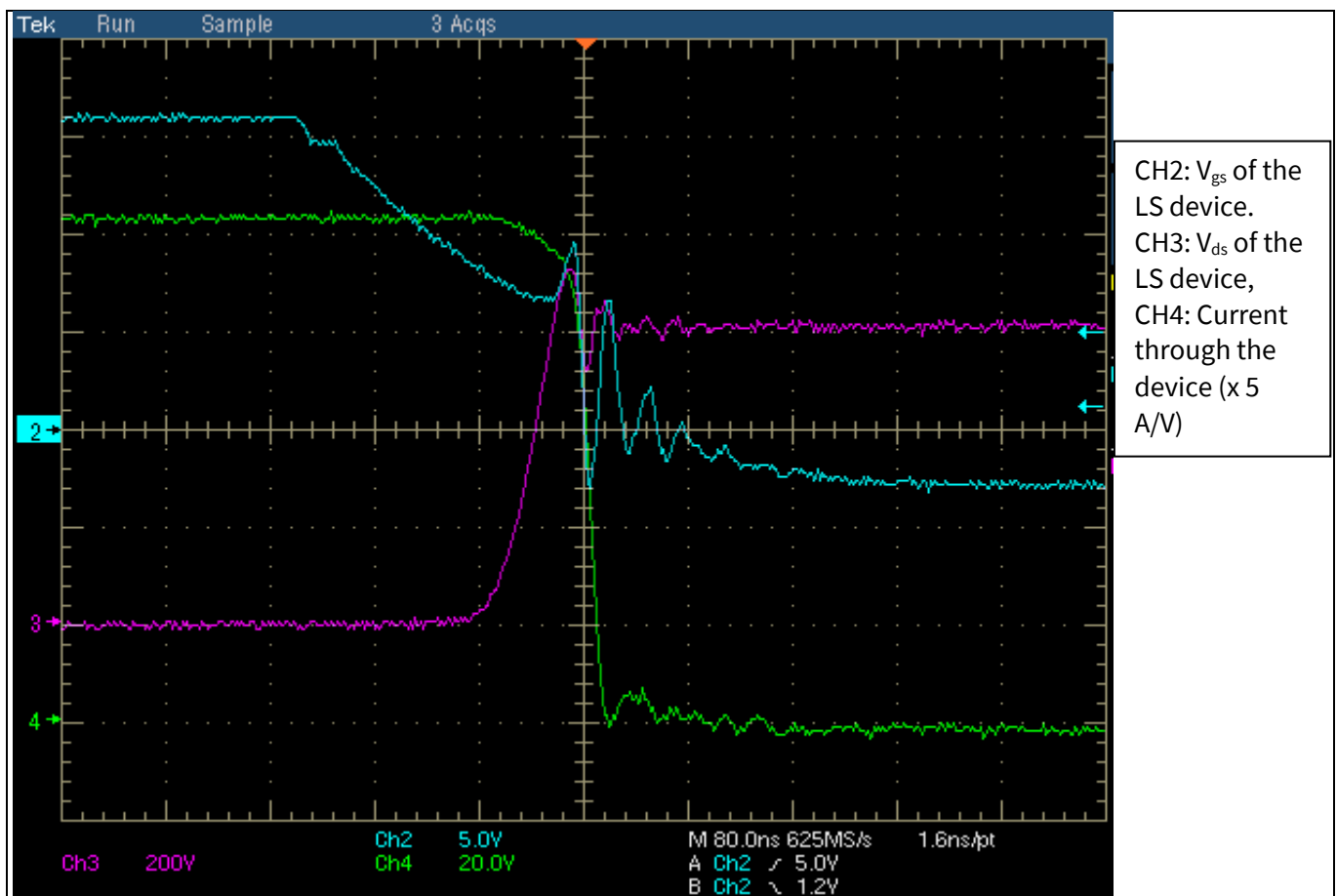


Figure 10 Turn-off of a FF11MR12W1M1_B11 device at 100 A and 600 V

3.3 Current sharing

The use of fast switching devices requires a high level of symmetry in the module as well as in the PCB design. This aspect has been taken into account during the design of the EVAL-PS-E1BF12-SiC board. Figure 11 shows the connection of the DC-link to the board input and the module. As illustrated, the PCB layer design achieves a high level of symmetry.

Figure 12 shows the results of this symmetrical design. The output current flows with nearly no current mismatch between the two groups of output pins into the board. Consequently, this approach leads to a higher level of power density, as the current mismatch does not create a bottleneck.

Characterization

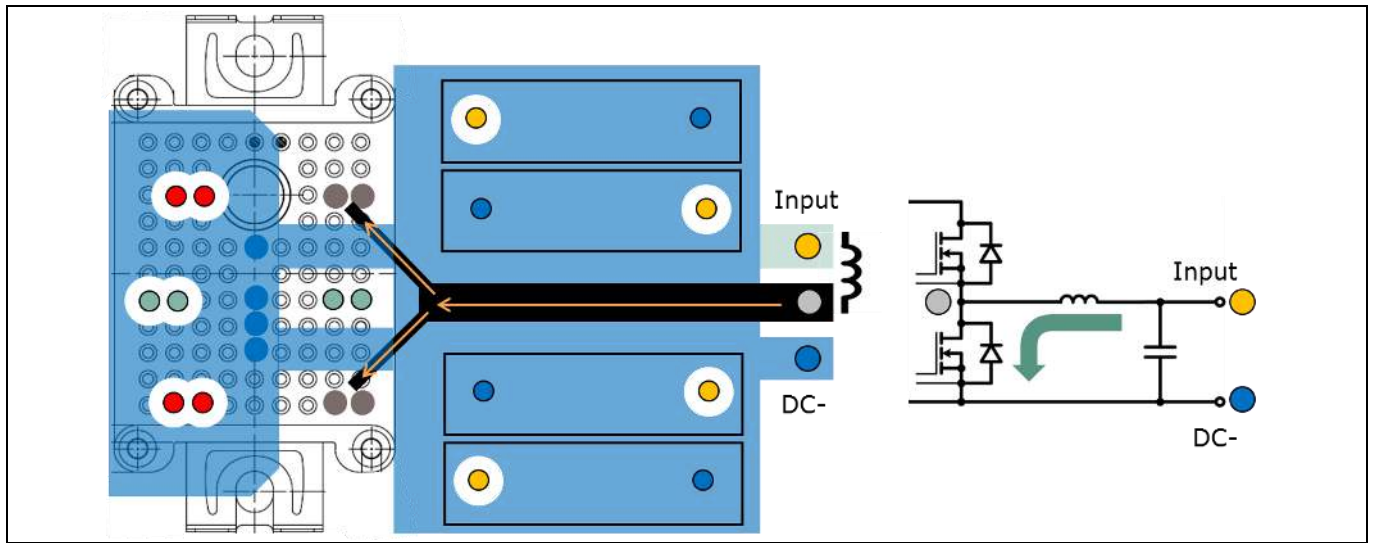


Figure 11 PCB layer design of the input DC-link

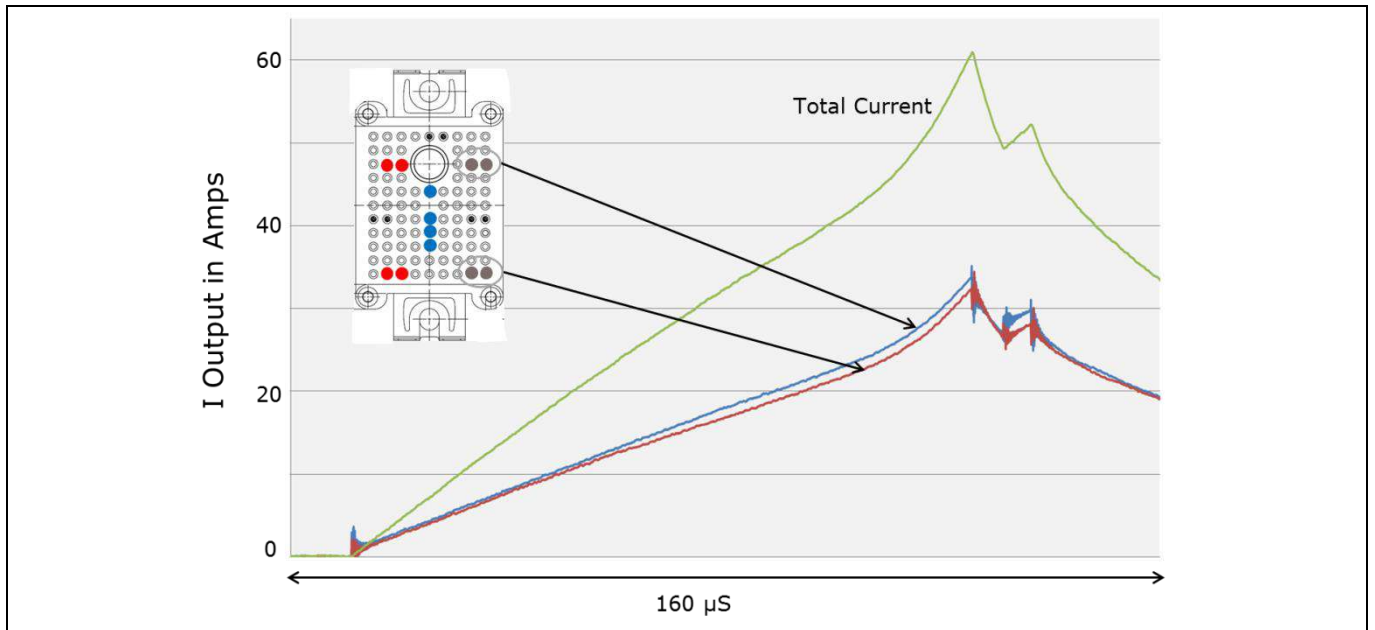


Figure 12 Current sharing of the EVAL-PS-E1BF12-SiC board toward the inductor terminals

Schematic, layout and bill of material

4 Schematic, layout and bill of material

To meet the individual customer requirements and to ease the development or modification using the evaluation driver board for the Easy module, all necessary technical data like schematic, layout and components are included in this chapter.

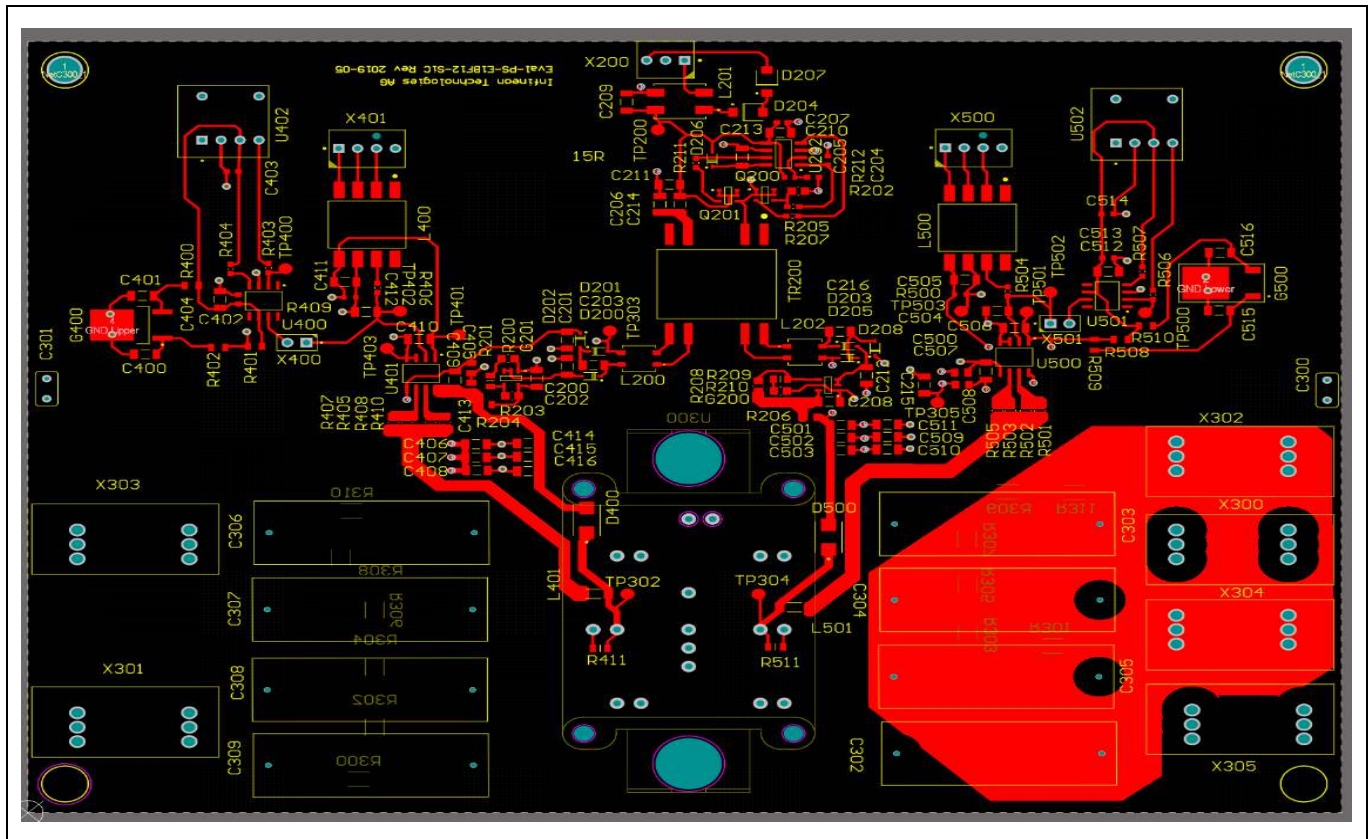
4.1 Layout

The PCB is a four-layer board made of FR4 material. The layer stack of the board is shown below in the Figure 13. The layout is provided in the subsequent drawings.

Layer Name	Type	Material	Thickness (mil)	Dielectric Material	Dielectric Constant
Top Overlay	Overlay				
Top Solder	Solder Mas...	Surface Ma...	0.4	Solder Resi...	3.5
1 L1	Signal	Copper	1.4		
Dielectric 1	Dielectric	Core	10	FR-4	4.2
2 L2	Signal	Copper	1.417		
Dielectric 3	Dielectric	Prepreg	5		4.2
3 L3	Signal	Copper	1.417		
Dielectric 2	Dielectric	Core	10		4.2
4 L4	Signal	Copper	1.4		
Bottom Sol...	Solder Mas...	Surface Ma...	0.4	Solder Resi...	3.5
Bottom Ov...	Overlay				

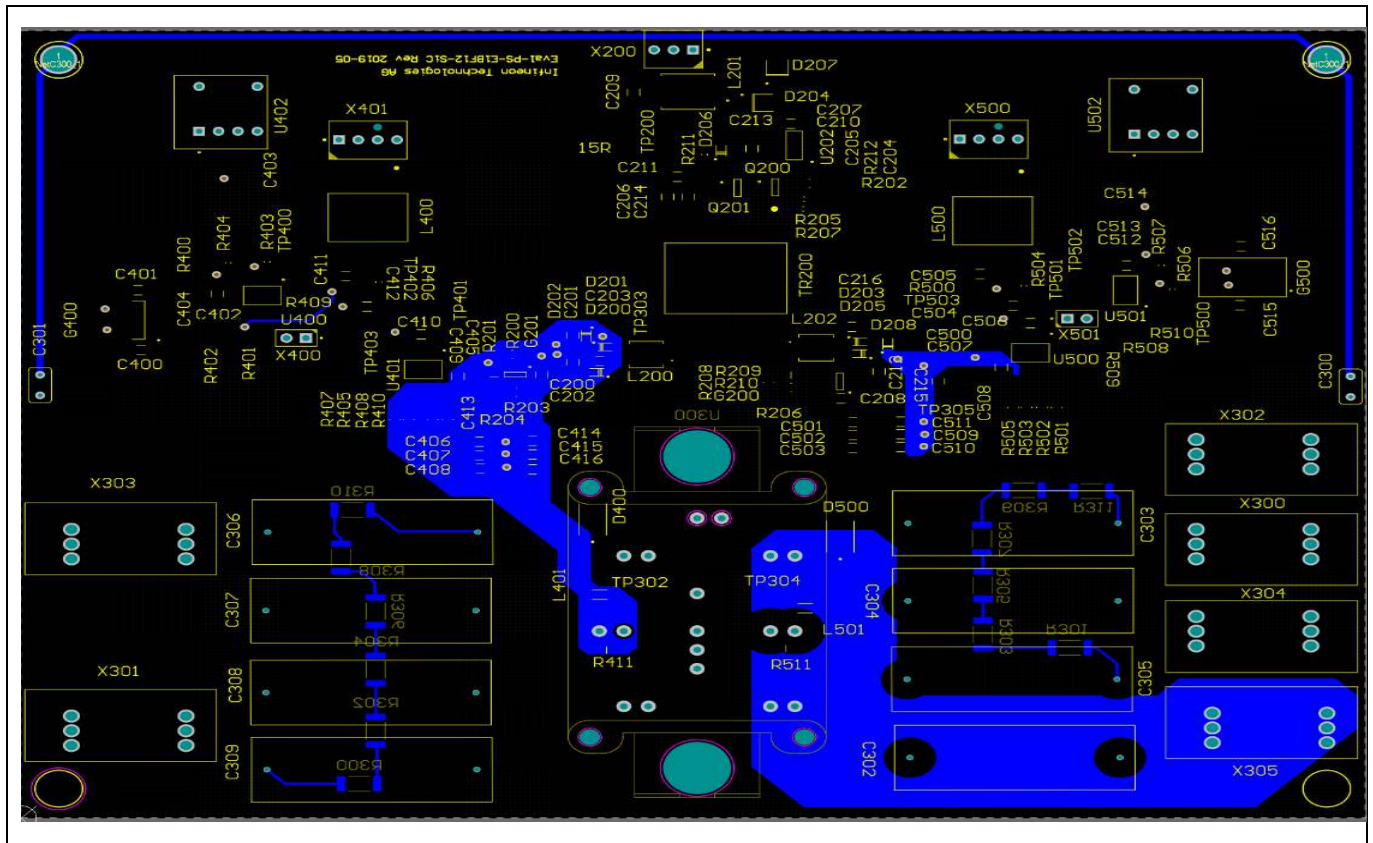
Figure 13 PCB stack of the evaluation board

Layer 1:



Schematic, layout and bill of material

Layer 4:



4.2 Bill of material

The tolerance recommendations for resistors should be less or equal to $\pm 1\%$, for the capacitors of the type COG, less or equal to $\pm 5\%$, and for capacitors of the type X7R, less or equal to $\pm 10\%$.

Type	Comment	Designator	Quantity	Package reference	Recommended manufacturer
Capacitor	4.7 uF	C200, C201, C202, C203, C206, C208, C210, C211, C212, C214, C215, C216, C404, C406, C407, C408, C414, C415, C416, C501, C502, C503, C509, C510, C511, C512	26	1206 (X7R)	NO
Capacitor	100 pF	C204	1	0603 (COG)	NO
Capacitor	100 pF	C205	1	0603 (COG)	NO
Capacitor	1 uF	C207	1	0603 (X7R)	NO
Capacitor	100 nF	C209, C213, C409, C410, C506, C507	6	1206 (X7R)	NO
Capacitor	4.7 nF	C300, C301	2	Radial Type	NO
Capacitor	2 uF	C302, C303, C304, C305, C306, C307, C308, C309	8	wire leads 27.5 mm pitch	NO
Capacitor	1 nF	C400, C401, C412, C504, C515, C516	6	1206 (COG)	NO
Capacitor	100 nF	C402, C403, C513, C514	4	0603 (X7R)	NO

Schematic, layout and bill of material

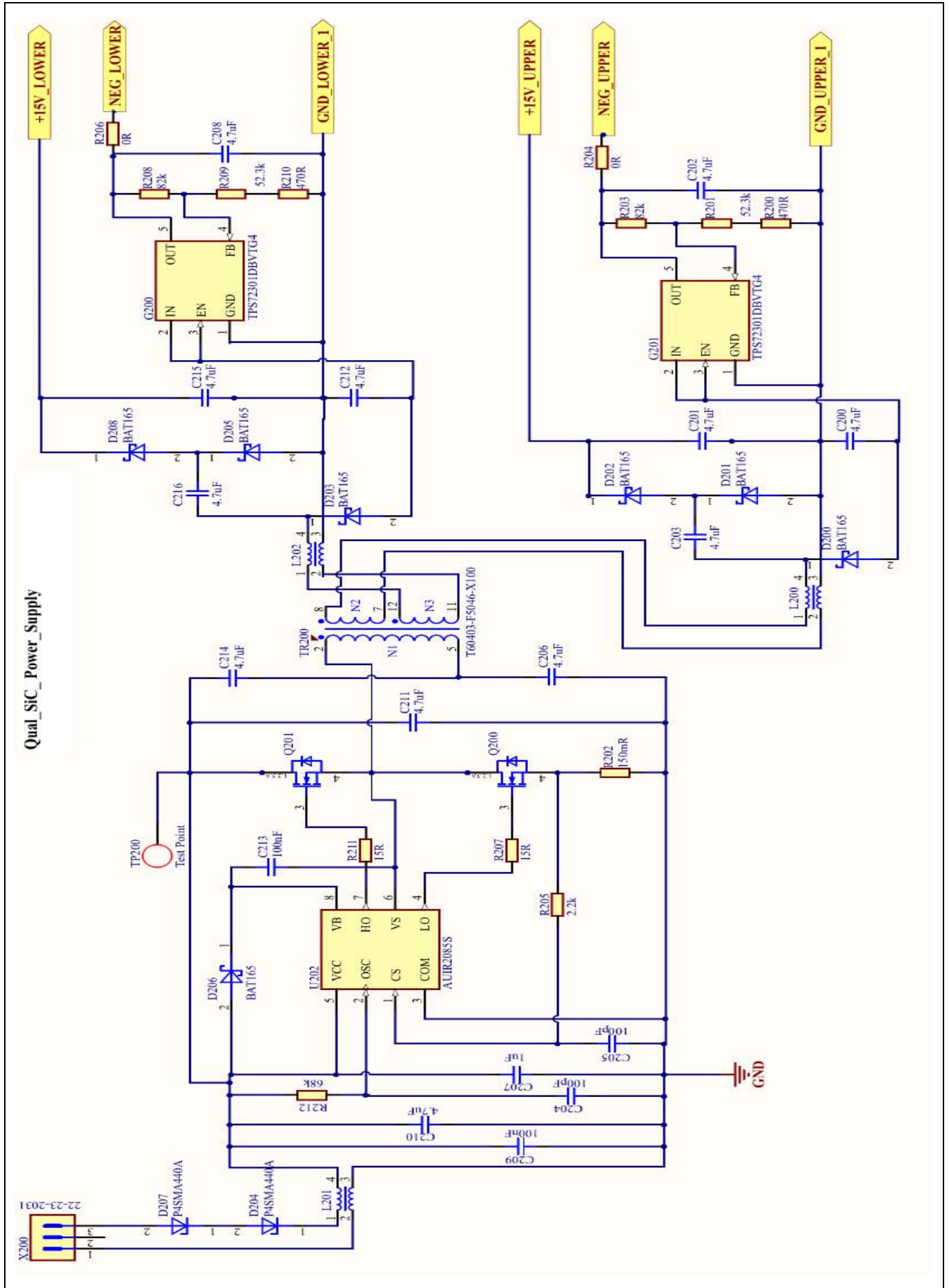
Type	Comment	Designator	Quantity	Package reference	Recommended manufacturer
Capacitor	100 nF	C405, C413, C500, C508	4	0805 (X7R)	NO
Capacitor	10 nF	C411, C505	2	1206 (C0G)	NO
Capacitor	1.5 nF	R411, R511	2	0805	NO
Resistor	470 R	R200, R210	2	0805	NO
Resistor	52.3 k	R201, R209	2	0805	NO
Resistor	150 mR	R202	1	0805	NO
Resistor	82 k	R203, R208	2	0805	NO
Resistor	0 R	R204, R206, R400, R401, R402, R508, R509, R510	8	0805	NO
Resistor	2.2 k	R205	1	0603	NO
Resistor	15 R	R207, R211	2	0603	NO
Resistor	68 k	R212	1	0603	NO
Resistor	68 k	R300, R301, R302, R303, R304, R305, R306, R307, R308, R309, R310, R311	12	2010	NO
Resistor	1.8 k	R403, R506	2	0603	NO
Resistor	10 k	R404, R507	2	0603	NO
Resistor	10 R	R405, R407, R503, R505	4	0805	NO
Resistor	100 R	R406, R504	2	0603	NO
Resistor	22 R	R408, R410, R501, R502	4	0805	NO
Resistor	4.7 k	R409, R500	2	0603	NO
Magnetics	ACM4520-142-2P-T000	L200, L202	2	SMD	TDK Corporation
Magnetics	ACM7060-301-2PL-TL01	L201	1	7X6X3.5mm	TDK Corporation
Magnetics	B82792C2475N365	L400, L500	2	SMD	TDK Corporation
Magnetics	BLM41PG600SN1	L401, L501	2	4516 (1806)	muRata
Magnetics	T60403-F5046-X100	TR200	1	Transformer, SMD; 2.54mm Pitch, 17mm L x 16mm W x 12mm H body	Vacuumschmelze
Semiconductor	P4SMA440A	D204, D207	2	DO-214AC	Diotec Semiconductor
Semiconductor	ES2D	D400, D500	2	DO-214AA	ON Semiconductor
Semiconductor	TPS72301DBVTG4	G200, G201	2	SOT23-5 (DBV)	Texas Instruments
Semiconductor	BAT165	D200, D201, D202, D203, D205, D206, D208	7	SOD323	Infineon Technologies
Semiconductor	IFX7805ABTF	G500, G400	1	PG-TO252-3-11	Infineon Technologies
Semiconductor	BSL302SN	Q200, Q201	2	PG-TSOP-6	Infineon Technologies
Semiconductor	AUIR2085S	U202	1	SOIC8-N	Infineon Technologies
Semiconductor	FF11MR12W1M1_B11	U300	1	AG-EASY1B-2	Infineon Technologies
Semiconductor	1EDI60I12AF	U401, U500	2	PG-DSO-8-51	Infineon Technologies



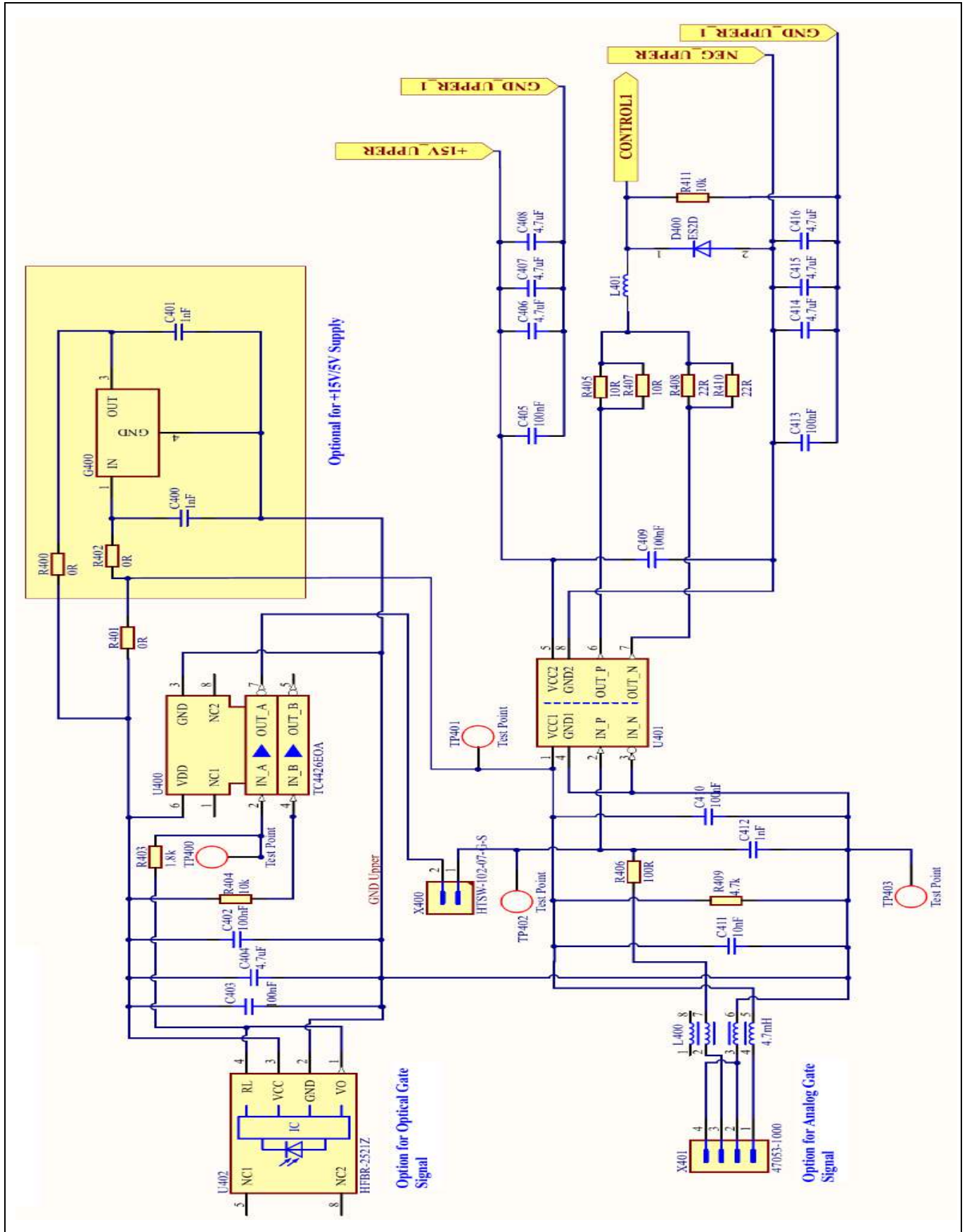
Schematic, layout and bill of material

Type	Comment	Designator	Quantity	Package reference	Recommended manufacturer
Semiconductor	TC4426EOA	U400, U501	2	SOIC	Microchip Technology
Semiconductor	HFBR-2521Z	U402, U502	2	THT	Broadcom
Connector	22-23-2031	X200	1		MOLEX Incorporated
Connector	1735862	X300, X301, X302, X303, X304, X305	6		Phoenix Contact
Connector	HTSW-102-07-G-S	X400, X501	2		Samtec
Connector	47053-1000	X401, X500	2		MOLEX Incorporated

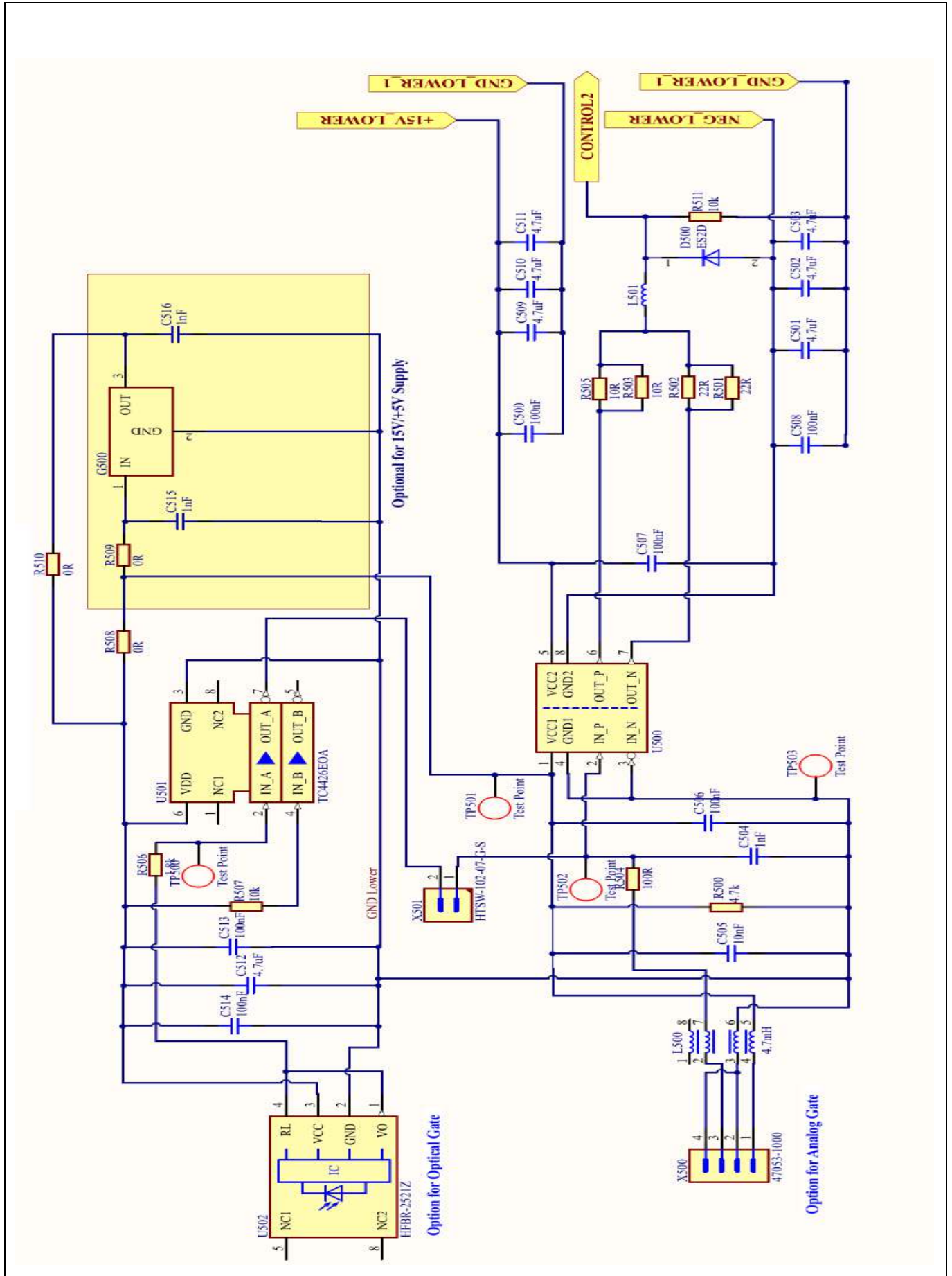
Schematic, layout and bill of material



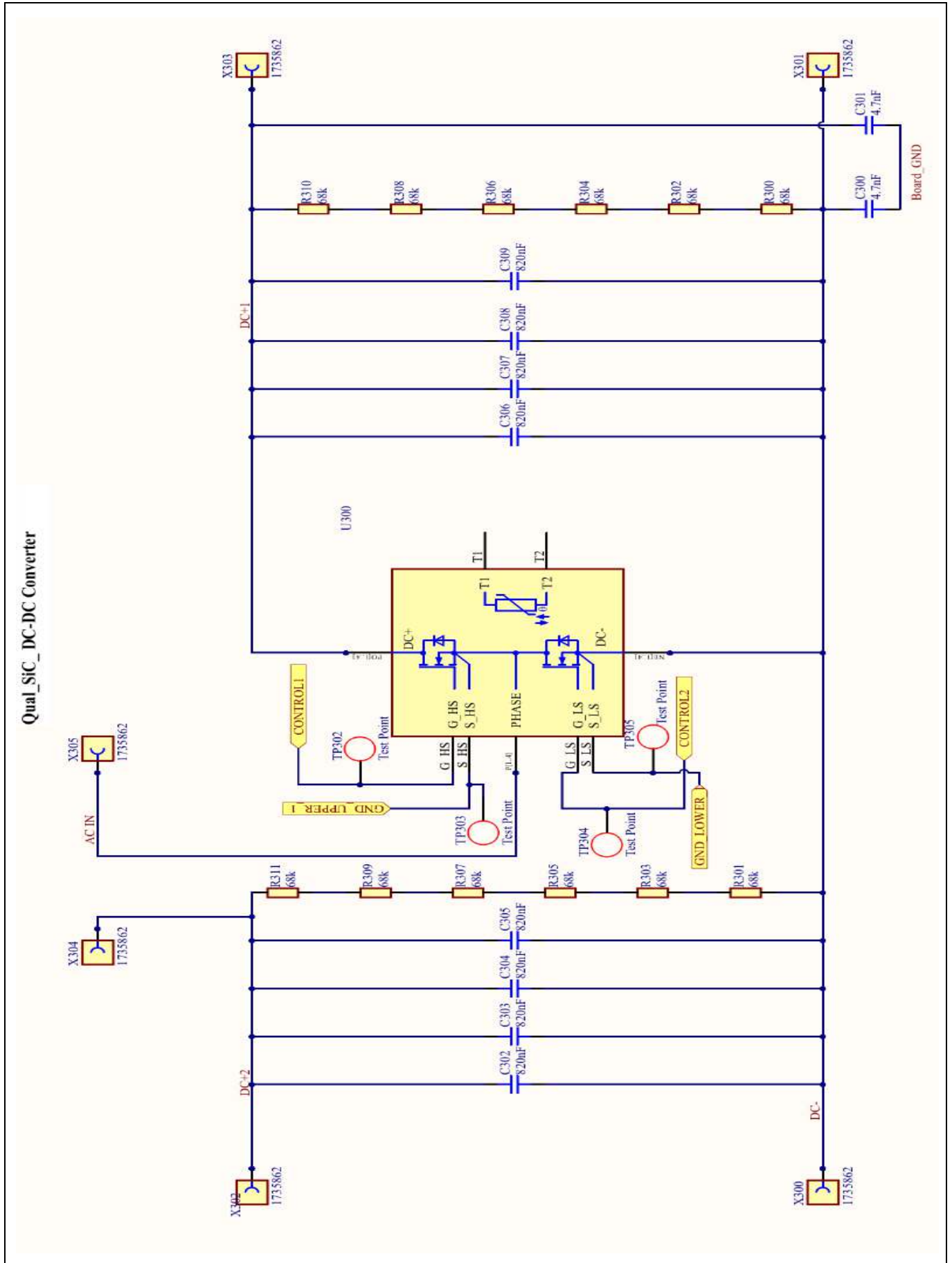
Schematic, layout and bill of material



Schematic, layout and bill of material



Schematic, layout and bill of material



Conclusion

5 Conclusion

The evaluation board EVAL-PS-E1BF12-SiC demonstrates the design of a symmetrical and low inductive board to fully exploit the superior properties of CoolSiC™ MOSFET Easy power modules. The low board inductance has been achieved by applying strip line concepts in the board design.

Furthermore, the PCB layout has been a main focus during the board development. The symmetric board layout leads to a very low current mismatch, which allows the maximum achievable power density with CoolSiC™ MOSFET modules.

The board allows for an extensive evaluation of the FF11MR12W1M1_B11 and FF23MR12W1M1_B11 properties. In this application note, the general turn-on and turn-off behavior as well as the robustness against parasitic turn-on has been shown.

Further investigations are possible with the EVAL-PS-E1BF12-SiC board such as determining the power conversion efficiency during buck or boost operation, the behavior at different R_g values, and temperature-dependent measurements, etc.

How to order

6 How to order

Each evaluation driver board has its own IFX order number and can be ordered via your Infineon sales partner.

Information can also be found at the Infineon Web Page: www.infineon.com

CAD data for the board described here is available on request. The use of this data is subjected to the disclaimer given in this AN. Please contact: WAR-IGBT-Application@infineon.com

IFX order number for **EVAL-PS-E1BF12-SiC**: **SP001798382**

Reference

7 Reference

The following literature might be helpful:

- [1] Slawinski, M., Villbusch, T., Heer, D., & Buschkuehle, M. (2016, May). Demonstration of superior SiC MOSFET Module performance within a Buck-Boost Conversion System. In *PCIM Europe 2016; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management; Proceedings of* (pp. 1-8). VDE.
- [2] Infineon Technologies AG, AN2017-04 Advanced Gate Drive Options for Silicon-Carbide (SiC) MOSFET using EiceDRIVER™, April 2017, www.infineon.com
- [3] Heer, D., Domes, D., & Peters, D. (2016, May). Switching performance of a 1200 V SiC-Trench-MOSFET in a low-power module. In *PCIM Europe 2016; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management; Proceedings of* (pp. 1-7). VDE.
- [4] Klaus Sobe, Thomas Basler, Blaz Klobucar .Characterization of the parasitic turn-on behavior of discrete CoolSiC™ MOSFETs, PCIM Europe 2019, 7 – 9 May 2019, Nuremberg, Germany.
- [5] Infineon Technologies AG , AN 2018-09 : Guidelines for CoolSiC MOSFET gate drive voltage window, May 2019, www.infineon.com



8 Revision history

Document version	Date of release	Description of changes
1.0	23/10/2017	Initial version
2.0	08/10/2019	Board layout has been updated, and negative voltage regulator added

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